查询TC74VHC4040F供应商 捷多邦，专业PCB打样工厂，24小时加急出货

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74VHC4040F, TC74VHC4040FN, TC74VHC4040FT

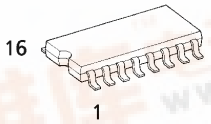
12 - STAGE RIPPLE - CARRY BINARY COUNTER

(Note) The JEDEC SOP (FN) is not available in Japan.

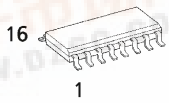
The TC74VHC4040 is an advanced high speed CMOS 12 - STAGE BINARY COUNTER / DIVIDER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.
Setting CLR to high resets the counter to low.
A negative transition on the $\overline{CK}$ input brings one increment into the counter.
This counter provides all divided output stages, and at Q12, a 1 / 4096 divided frequency will be output.
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES :

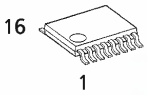
- High Speed····· f_{MAX} = 210MHz (typ.) at V_{CC} = 5V
- Low Power Dissipation····· I_{CC} = 4μA (Max.) at Ta = 25°C
- High Noise Immunity····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays···· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range··· V_{CC} (opr) = 2V ~ 5.5V
- Low Noise ····· V_{OLP} = 1.5V (Max.)
- Pin and Function Compatible with 74HC4040



F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

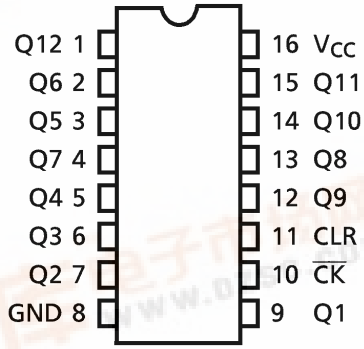


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)



FT (TSSOP16-P-0044-0.65)
Weight : 0.06g (Typ.)

PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

$\overline{CK}$	CLR	OUTPUT STATE
X	H	ALL OUTPUTS = "L"
↓	L	NO CHANGE
↑	L	ADOVANCE TO NEXT STATE

X : Don't Care

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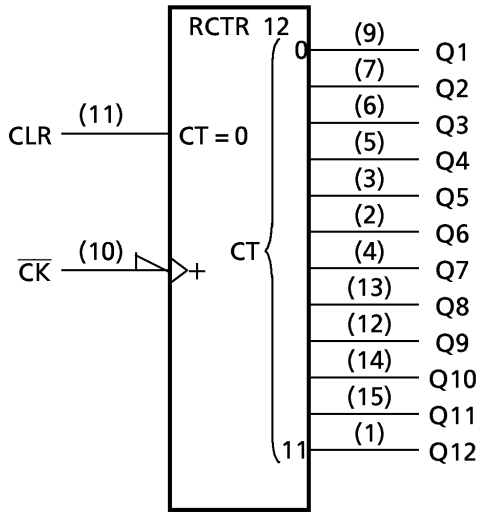
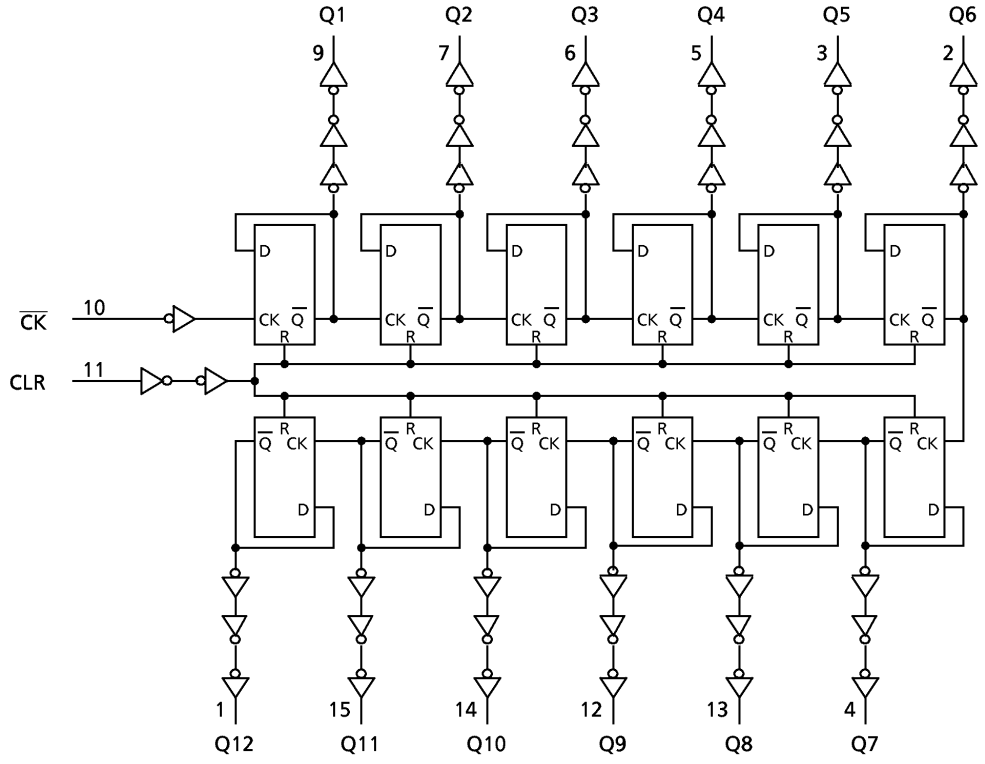
IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±100	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2.0~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt/dv	0~100 (V_{CC} = 3.3 ± 0.3V) 0~20 (V_{CC} = 5 ± 0.5V)	ns/V

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0	1.50	—	—	1.50	—	V
				3.0~5.5	V_{CC}×0.7	—	—	V_{CC}×0.7	—	
Low - Level Input Voltage	V_{IL}			2.0	—	—	0.50	—	0.50	V
				3.0~5.5	—	—	V_{CC}×0.3	—	V_{CC}×0.3	
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
			I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
			I_{OH} = −8mA	4.5	3.94	—	—	3.80	—	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
			I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
			I_{OL} = 8mA	4.5	—	—	0.36	—	0.44	
Input Leakage Current	I_{IN}	V_{IN} = 5.5V or GND		0~5.5	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		5.5	—	—	4.0	—	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP .	LIMIT	LIMIT	
Minimum Pulse Width ($\overline{CK}$)	$t_{W(L)}$ $t_{W(H)}$		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	ns
Minimum Pulse Width (CLR)	$t_{W(H)}$		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	
Minimum Removal Time	t_{rem}		3.3 ± 0.3 5.0 ± 0.5	— —	5.0 5.0	5.0 5.0	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	CL (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time ($\overline{CK}$-Q)	t_{pLH} t_{pHL}		3.3 ± 0.3	15	—	7.5	11.9	1.0	14.0	ns
				50	—	10.0	15.4	1.0	17.5	
			5.0 ± 0.5	15	—	4.8	7.3	1.0	8.5	
				50	—	6.3	9.3	1.0	10.5	
Propagation Delay Time (Qn-Qn + 1)	Δt_{pd}		3.3 ± 0.3	50	—	2.4	4.4	1.0	5.0	
			5.0 ± 0.5	50	—	1.6	3.1	1.0	3.5	
Propagation Delay Time (CLR-Q)	t_{pHL}		3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
				50	—	7.1	10.6	1.0	12.0	
Maximum Clock Frequency	f_{MAX}		3.3 ± 0.3	15	75	140	—	75	—	MHZ
				50	55	80	—	50	—	
			5.0 ± 0.5	15	150	210	—	125	—	
				50	95	125	—	80	—	
Input Capacitance	C_{IN}				—	4	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(Note 1)			—	21	—	—	—	

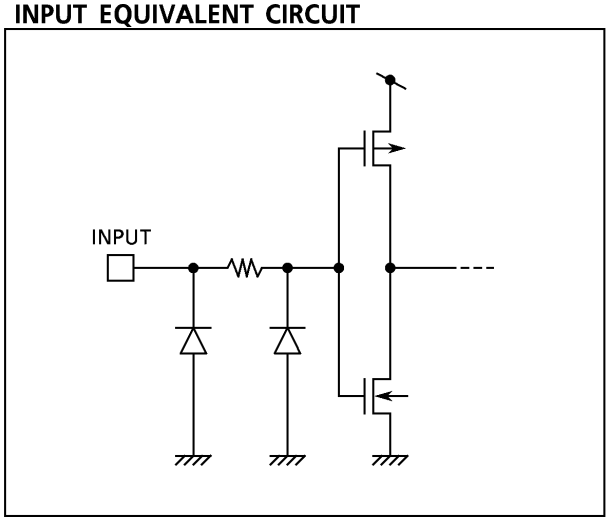
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

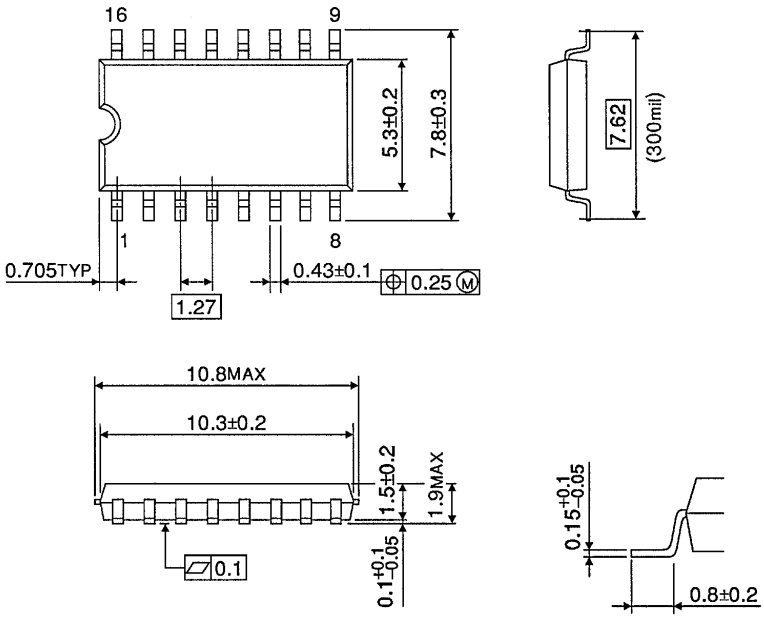
NOISE CHARACTERISTICS (Input $t_r = t_f = 3ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		UNIT
			V_{CC} (V)	TYP.	LIMIT	
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}	C_L = 50pF	5.0	1.2	1.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}	C_L = 50pF	5.0	− 1.2	− 1.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}	C_L = 50pF	5.0	−	3.5	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}	C_L = 50pF	5.0	−	1.5	V

INPUT EQUIVALENT CIRCUIT



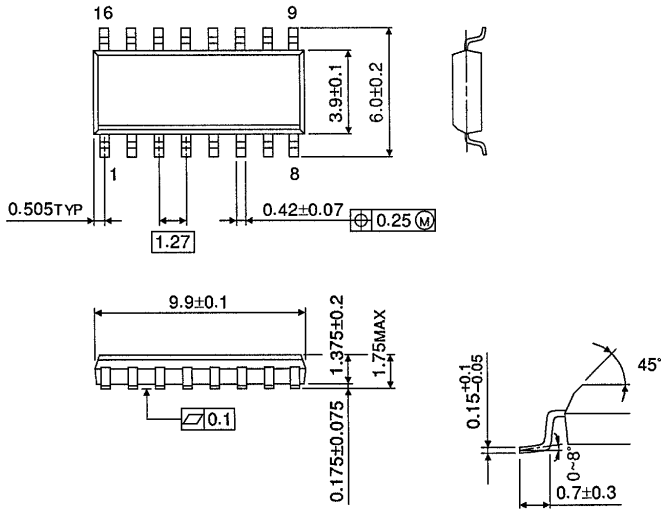
SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

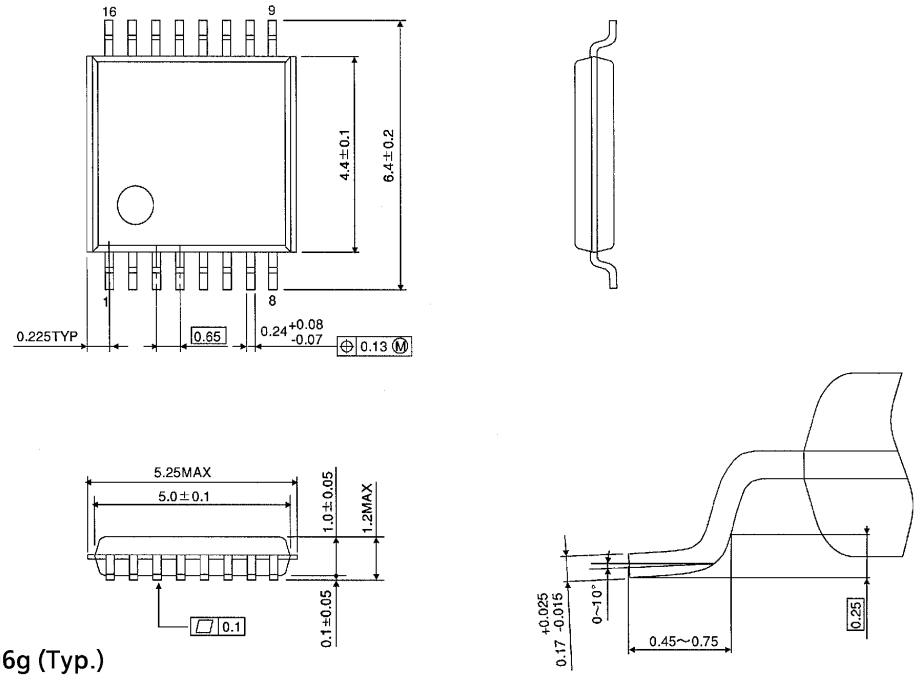
SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150-1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65) Unit in mm



Weight : 0.06g (Typ.)