

**TOSHIBA****TC74VHC74F/FN/FT**

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

**TC74VHC74F, TC74VHC74FN, TC74VHC74FT****DUAL D - TYPE FLIP - FLOP WITH PRESET AND CLEAR**

(Note) The JEDEC SOP (FN) is not available in Japan.

The TC74VHC74 is an advanced high speed CMOS D - FLIP FLOP fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

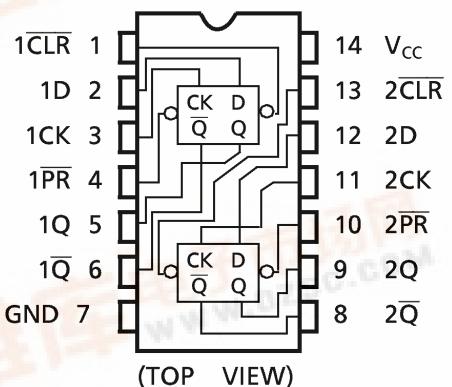
The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CK pulse.

CLR and PR are independent of the CK and are accomplished by setting the appropriate input low.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

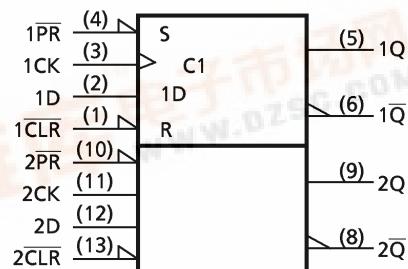
**FEATURES :**

- High Speed ..... f<sub>MAX</sub> = 170MHz(typ.) at V<sub>CC</sub> = 5V
- Low Power Dissipation ..... I<sub>CC</sub> = 2μA(Max.) at Ta = 25°C
- High Noise Immunity ..... V<sub>NH</sub> = V<sub>NL</sub> = 28% V<sub>CC</sub> (Min.)
- Power Down Protection is provided on all inputs.
- Balanced Propagation Delays ... t<sub>pLH</sub> ≈ t<sub>pHL</sub>
- Wide Operating Voltage Range....V<sub>CC</sub> (opr) = 2V~5.5V
- Pin and Function Compatible with 74ALS74

**PIN ASSIGNMENT****TRUTH TABLE**

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	↑	L	H	—
H	H	H	↑	H	L	—
H	H	X	↓	Q <sub>n</sub>	Q̄ <sub>n</sub>	NO CHANGE

X : Don't Care

**IEC LOGIC SYMBOL**

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## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	$V_{CC}$	-0.5~7.0	V
DC Input Voltage	$V_{IN}$	-0.5~7.0	V
DC Output Voltage	$V_{OUT}$	-0.5~ $V_{CC}$ +0.5	V
Input Diode Current	$I_{IK}$	-20	mA
Output Diode Current	$I_{OK}$	$\pm 20$	mA
DC Output Current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /Ground Current	$I_{CC}$	$\pm 50$	mA
Power Dissipation	$P_D$	180	mW
Storage Temperature	$T_{STG}$	-65~150	°C

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	$V_{CC}$	2.0~5.5	V
Input Voltage	$V_{IN}$	0~5.5	V
Output Voltage	$V_{OUT}$	0~ $V_{CC}$	V
Operating Temperature	$T_{OPR}$	-40~85	°C
Input Rise and Fall Time	$dt/dv$	0~100 ( $V_{CC} = 3.3 \pm 0.3$ V) 0~20 ( $V_{CC} = 5 \pm 0.5$ V)	ns/V

## DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	$V_{CC}$ (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Input Voltage	$V_{IH}$		2.0 3.0~ 5.5	1.50 $V_{CC} \times 0.7$	—	—	1.50 $V_{CC} \times 0.7$	—	V
Low - Level Input Voltage	$V_{IL}$		2.0 3.0~ 5.5	—	—	0.50 $V_{CC} \times 0.3$	—	0.50 $V_{CC} \times 0.3$	V
High - Level Output Voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu A$	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	— — —	1.9 2.9 4.4	— — —
			$I_{OH} = -4mA$ $I_{OH} = -8mA$	3.0 4.5	2.58 3.94	— —	— —	2.48 3.80	— —
		$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu A$	2.0 3.0 4.5	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1
			$I_{OL} = 4mA$ $I_{OL} = 8mA$	3.0 4.5	— —	— —	0.36 0.36	— —	0.44 0.44
Input Leakage Current	$I_{IN}$	$V_{IN} = 5.5V$ or GND	0~5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu A$
Quiescent Supply Current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0	

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TIMING REQUIREMENTS (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	V <sub>CC</sub> (V)	T <sub>a</sub> = 25°C	T <sub>a</sub> = -40~85°C	UNIT
				LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_W(L)$		3.3 ± 0.3	6.0	7.0	ns
			5.0 ± 0.5	5.0	5.0	
	$t_W(L)$		3.3 ± 0.3	6.0	7.0	
			5.0 ± 0.5	5.0	5.0	
	$t_s$		3.3 ± 0.3	6.0	7.0	
Minimum Set-up Time			5.0 ± 0.5	5.0	5.0	ns
			3.3 ± 0.3	0.5	0.5	
			5.0 ± 0.5	0.5	0.5	
			3.3 ± 0.3	5.0	5.0	
			5.0 ± 0.5	3.0	3.0	

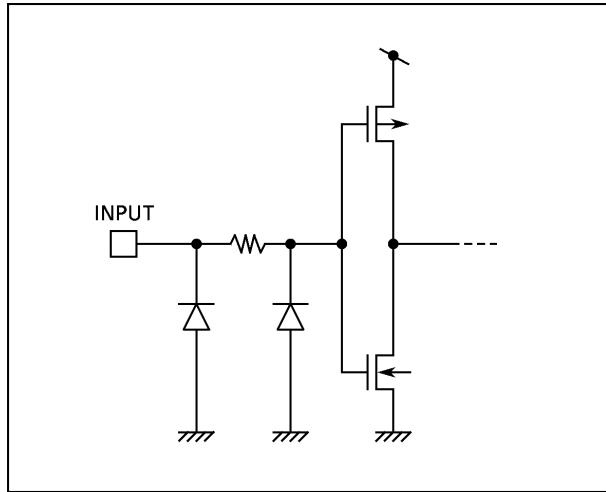
AC ELECTRICAL CHARACTERISTICS (Input  $t_r = t_f = 3\text{ns}$ )

PARAMETER	SYMBOL	TEST CONDITION	T <sub>a</sub> = 25°C			T <sub>a</sub> = -40~85°C		UNIT	
			V <sub>CC</sub> (V)	CL (pF)	MIN.	TYP.	MAX.		
Propagation Delay Time (CK - Q, $\bar{Q}$ )	$t_{PLH}$		3.3 ± 0.3	15	—	6.7	11.9	1.0	14.0
				50	—	9.2	15.4	1.0	17.5
			5.0 ± 0.5	15	—	4.6	7.3	1.0	8.5
				50	—	6.1	9.3	1.0	10.5
	$t_{PHL}$		3.3 ± 0.3	15	—	7.6	12.3	1.0	14.5
				50	—	10.1	15.8	1.0	18.0
			5.0 ± 0.5	15	—	4.8	7.7	1.0	9.0
				50	—	6.3	9.7	1.0	11.0
Maximum Clock Frequency	$f_{MAX}$		3.3 ± 0.3	15	80	125	—	70	MHz
				50	50	75	—	45	
			5.0 ± 0.5	15	130	170	—	110	
				50	90	115	—	75	
			—	—	4	10	—	10	
Input Capacitance	$C_{IN}$		—	—	—	—	—	—	pF
Power Dissipation Capacitance	$C_{PD}$	(Note 1)	—	—	25	—	—	—	

Note (1)  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

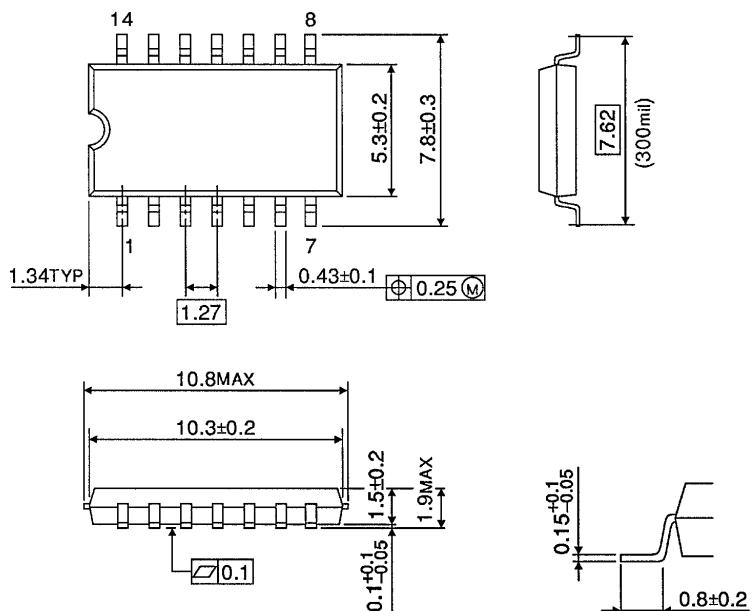
Average operating current can be obtained by the equation :

$$I_{CC(\text{opr.})} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

**INPUT EQUIVALENT CIRCUIT**

## SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

Unit in mm

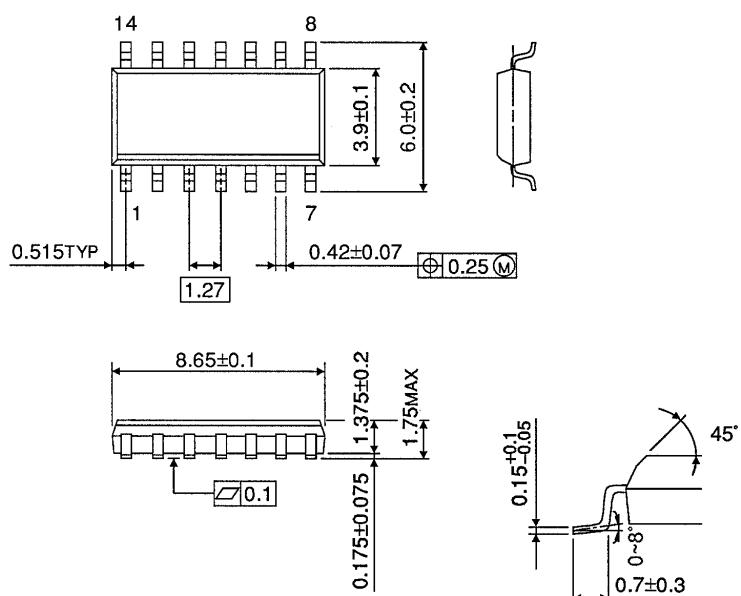


Weight : 0.18g (Typ.)

## SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150-1.27)

Unit in mm

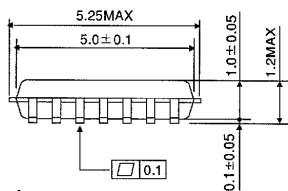
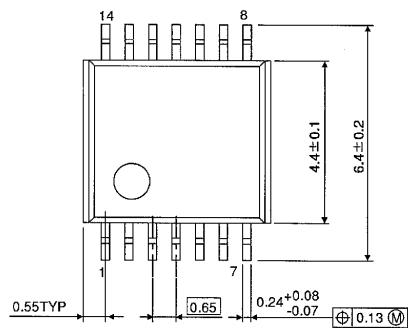
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

**TSSOP 14PIN OUTLINE DRAWING (TSSOP14-P-0044-0.65)**

Unit in mm



Weight : 0.06g (Typ.)

