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M5M5256DFP,VP,RV -70VLL-W,-85VLL-W, -70VXL-W,-85VXL-W

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5256DFP,VP,RV is 262,144-bit CMOS static RAMs organized as 32,768-words by 8-bits which is fabricated using high-performance 3 polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery results in a high density and low power static RAM. Stand-by current is small enough for battery back-up application. It is ideal for the memory systems which require simple interface.

Especially the M5M5256DVP,RV are packaged in a 28-pin thin small outline package.Two types of devices are available, M5M5256DVP(normal lead bend type package), M5M5256DRV(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5256DFP,VP,RV-70VLL	70ns	25mA (Vcc=3.6V)	12µA (Vcc=3.6V)
M5M5256DFP,VP,RV-85VLL	85ns		
M5M5256DFP,VP,RV-70VXL	70ns		2.4µA (Vcc=3.6V)
M5M5256DFP,VP,RV-85VXL	85ns		0.05µA (Vcc=3.0V, Typical)

- Single +3.3±0.3V power supply
- No clocks, no refresh
- Data-Hold on +2.0V power supply
- Directly TTL compatible : all inputs and outputs
- Three-state outputs : OR-tie capability
- /OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Low stand-by current·····0.05µA(typ.)

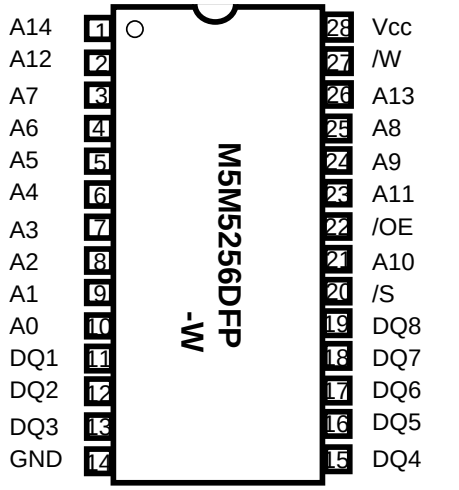
PACKAGE

M5M5256DFP : 28 pin 450 mil SOP
M5M5256DVP,RV : 28pin 8 X 13.4 mm² TSOP

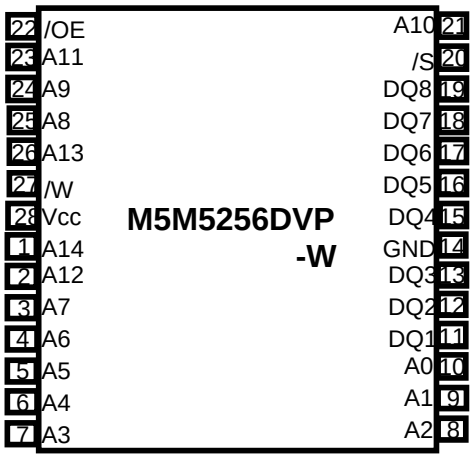
APPLICATION

Small capacity memory units

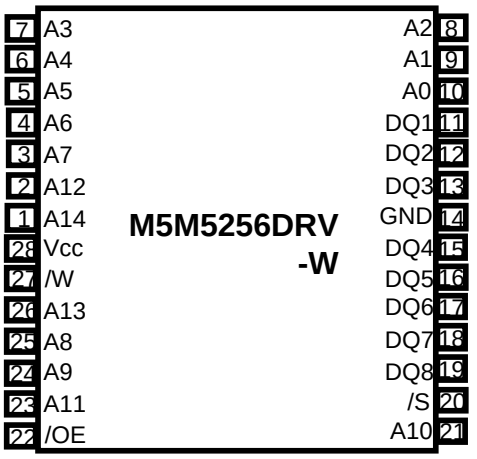
PIN CONFIGURATION (TOP VIEW)



Outline 28P2W-C (DFP)



Outline 28P2C-A (DVP)



Outline 28P2C-B (DRV)

M5M5256DFP,VP,RV -70VLL-W,-85VLL-W, -70VXL-W,-85VXL-W

262144-BIT (32768-WORD BY 8-BIT) CMOS STATIC RAM

FUNCTION

The operation mode of the M5M5256DP,KP,FP,VP,RV is determined by a combination of the device control inputs /S, /W and /OE. Each mode is summarized in the function table.

A write cycle is executed whenever the low level /W overlaps with the low level /S. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of /W, /S, whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable /OE directly controls the output stage. Setting the /OE at a high level,the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

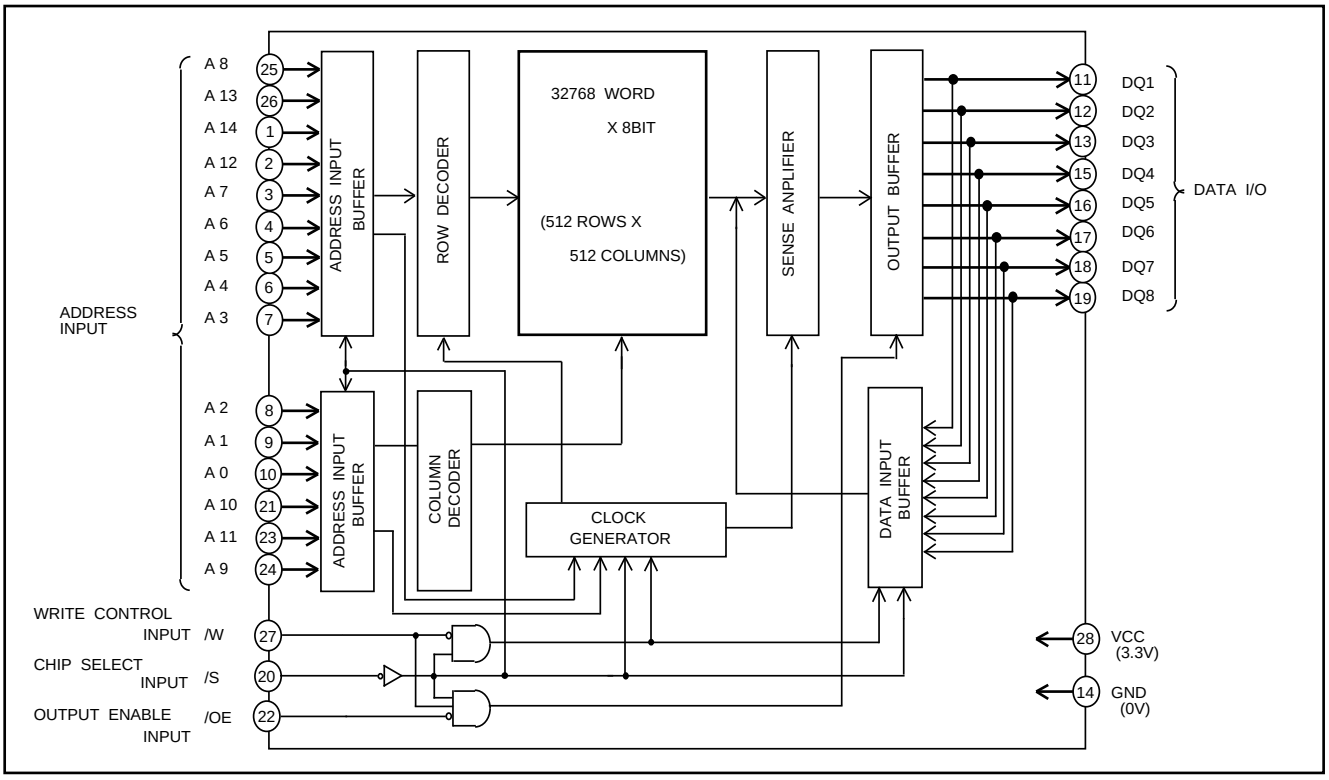
A read cycle is executed by setting /W at a high level and /OE at a low level while /S are in an active state.

When setting /S at a high level, the chip is in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by /S. The power supply current is reduced as low as the stand-by current which is specified as Icc3 or Icc4, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

/S	/W	/OE	Mode	DQ	Icc
H	X	X	Non selection	High-impedance	Stand-by
L	L	X	Write	D_{IN}	Active
L	H	L	Read	D_{OUT}	Active
L	H	H		High-impedance	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	-0.3*~4.6	V
V_I	Input voltage		-0.3*~Vcc+0.3 (Max 4.6)	V
V_O	Output voltage		0~Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		-20~70	°C
T_{stg}	Storage temperature		-65~150	°C

* -3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=-20~70°C, Vcc=3.3±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{IH}	High-level input voltage			2.0		Vcc +0.3	V
V_{IL}	Low-level input voltage			-0.3*		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH}=-0.5mA		2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}=-0.05mA		Vcc -0.5			V
V_{OL}	Low-level output voltage	I_{OL}=1mA				0.4	V
I_I	Input current	V_I=0~Vcc				±1	uA
I_O	Output current in off-state	/S=V_{IH} or or /OE=V_{IH}, $V_{I/O}$=0~Vcc				±1	uA
Icc1	Active supply current (AC, MOS level)	/S≤0.2V, Other inputs<0.2V or >Vcc-0.2V Output-open Min. cycle	Min. cycle		13	25	mA
			1MHz		1.5	3	
Icc2	Active supply current (AC, TTL level)	/S=V_{IL}, other inputs=V_{IH} or V_{IL} Output-open Min. cycle	Min. cycle		14	25	mA
			1MHz		1.5	3	
Icc3	Stand-by current	/S≥Vcc-0.2V, other inputs=0~Vcc	-VLL			12	uA
			-VXL		0.05	2.4	
Icc4	Stand-by current	/S=V_{IH},other inputs=0~Vcc				0.33	mA

* -3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (Ta=-20~70°C, Vcc=3.3±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 0: Direction for current flowing into an IC is positive (no mark).
1: Typical value is one at Ta = 25°C.
2: C_I, C_O are periodically sampled and are not 100% tested.

AC ELECTRICAL CHARACTERISTICS (Ta = -20~70°C, Vcc=3.3±0.3V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level·····V_{IH}=2.2V,V_{IL}=0.4V

Input rise and fall time·····5ns

Reference level·····V_{OH}=V_{OL}=1.5V

Output loads·····Fig.1,CL=30pF (-70VLL,-70VXL)

CL=50pF (-85VLL,-85VXL)

CL=5pF (for ten,tdis)

Transition is measured ±500mV from steady state voltage. (for ten,tdis)

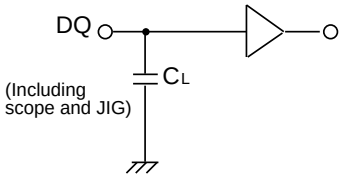


Fig.1 Output load

(2) READ CYCLE

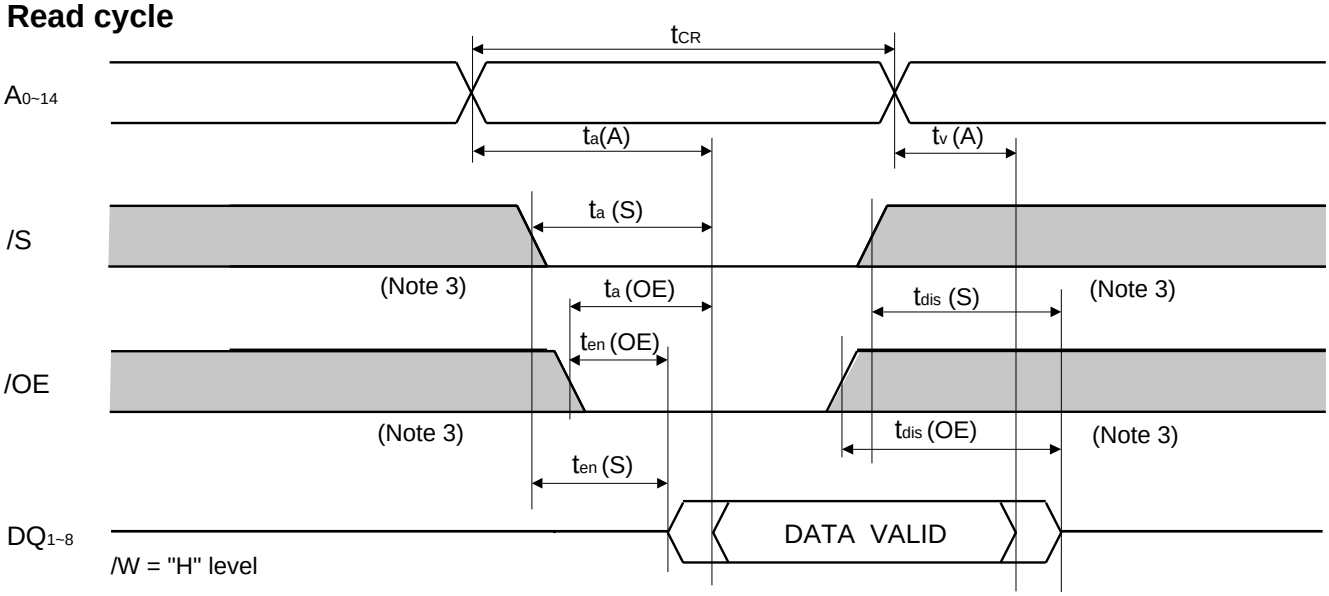
Symbol	Parameter	Limits				Unit
		-70VLL, VXL		-85VLL, VXL		
		Min	Max	Min	Max	
t_{CR}	Read cycle time	70		85		ns
t_a(A)	Address access time		70		85	ns
t_a(S)	Chip select access time		70		85	ns
t_a(OE)	Output enable access time		35		45	ns
t_{dis}(S)	Output disable time after /S high		25		25	ns
t_{dis}(OE)	Output disable time after /OE high		25		25	ns
t_{en}(S)	Output enable time after /S low	5		10		ns
t_{en}(OE)	Output enable time after /OE low	5		10		ns
t_v(A)	Data valid time after address	10		10		ns

(3) WRITE CYCLE

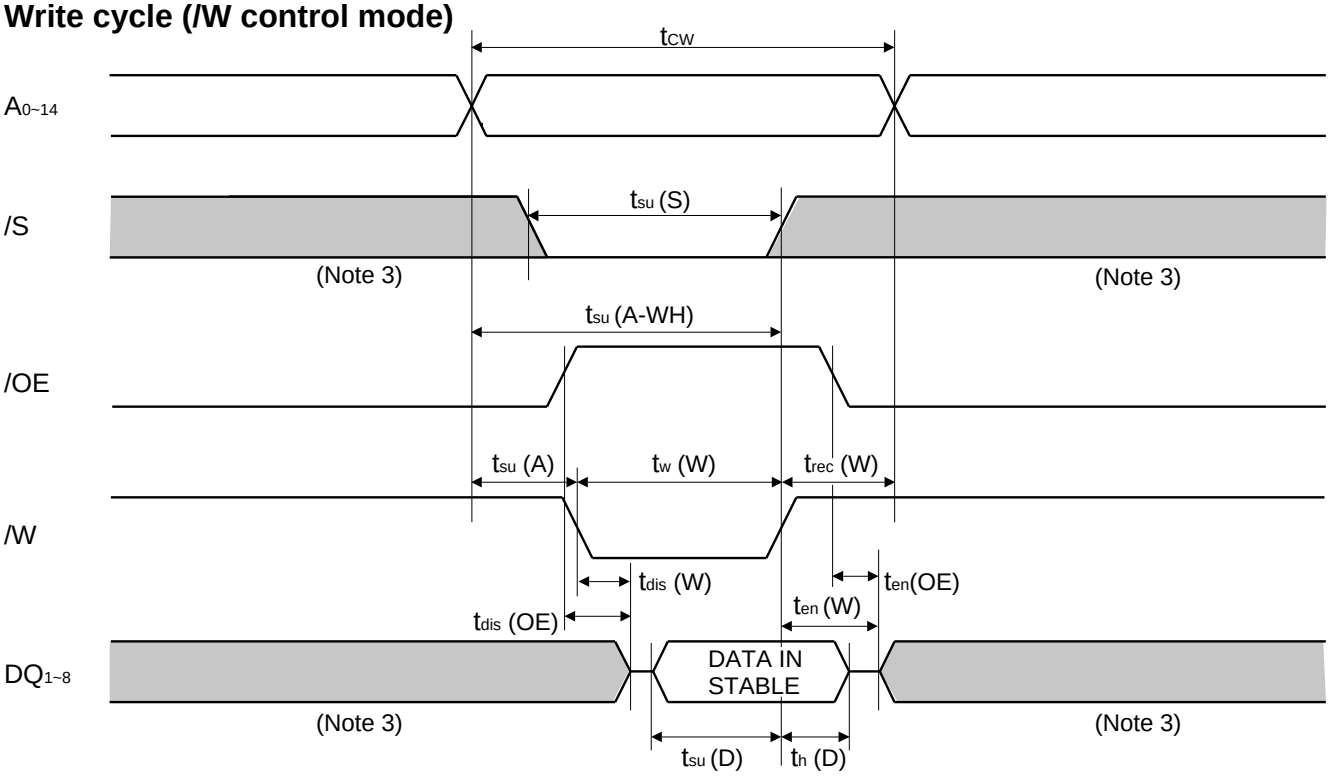
Symbol	Parameter	Limits				Unit
		-70VLL, VXL		-85VLL, VXL		
		Min	Max	Min	Max	
t_{CW}	Write cycle time	70		85		ns
t_w(W)	Write pulse width	55		60		ns
t_{su}(A)	Address setup time	0		0		ns
t_{su}(A-WH)	Address setup time with respect to /W high	65		70		ns
t_{su}(S)	Chip select setup time	65		70		ns
t_{su}(D)	Data setup time	30		35		ns
t_h(D)	Data hold time	0		0		ns
t_{rec}(W)	Write recovery time	0		0		ns
t_{dis}(W)	Output disable time from /W low		25		25	ns
t_{dis}(OE)	Output disable time from /OE high		25		25	ns
t_{en}(W)	Output enable time from /W high	5		10		ns
t_{en}(OE)	Output enable time from /OE low	5		10		ns

(4) TIMING DIAGRAMS

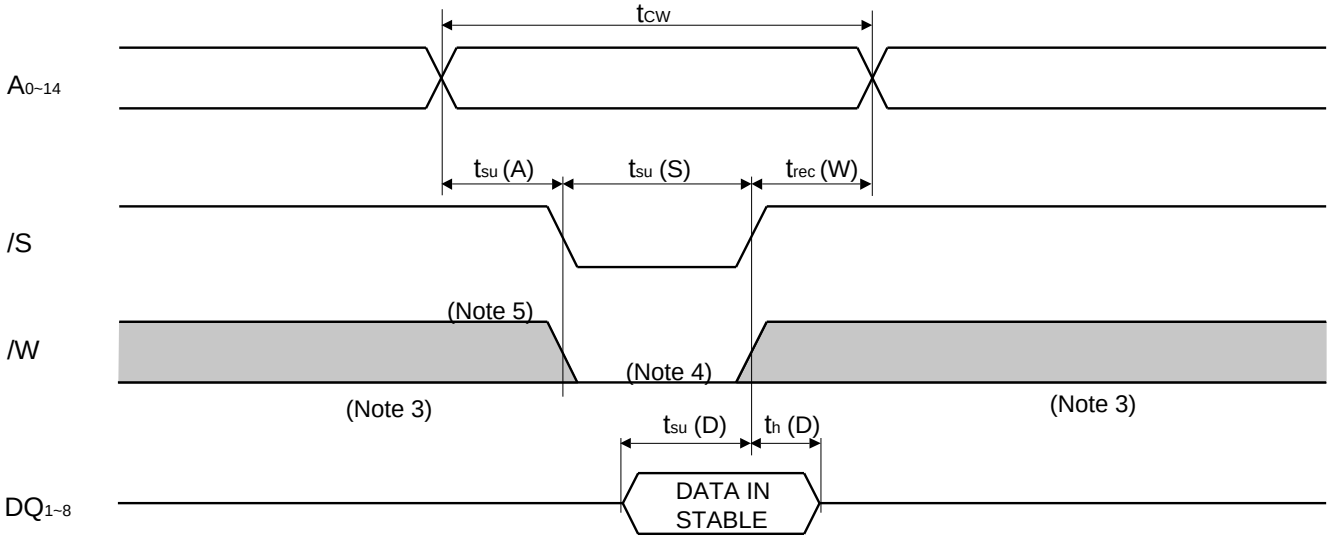
Read cycle



Write cycle (/W control mode)



Write cycle (/S control mode)



Note 3 : Hatching indicates the state is "don't care".
4 : Writing is executed in overlap of /S and /W low.
5 : If /W goes low simultaneously with or prior to /S, the outputs remain in the high impedance state.
6 : Don't apply inverted phase signal externally when DQ pin is output mode.
7 : ten, tdis are periodically sampled and are not 100% tested.

POWER DOWN CHARACTERISTICS

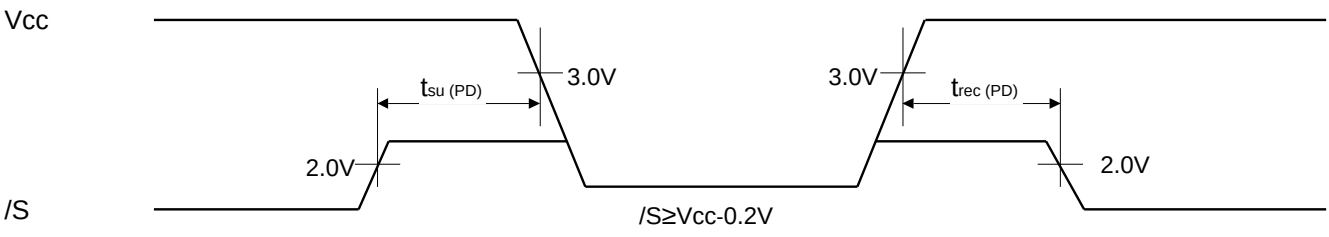
(1) ELECTRICAL CHARACTERISTICS (Ta = -20~70°C, Vcc=3.3±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{CC\ (PD)}$	Power down supply voltage			2			V
$V_{I\ (/S)}$	Chip select input /S			2			V
$I_{CC\ (PD)}$	Power down supply current	Vcc = 3V,/S≥Vcc-0.2V, Other inputs=0~Vcc	-VLL			10 (Note 7)	uA
			-VXL		0.05	2 (Note 8)	

Note7: ICC (PD) = 1uA in case of Ta = 25°C
Note8: ICC (PD) = 0.2uA in case of Ta = 25°C

(2) TIMING REQUIREMENTS (Ta = -20~70°C, Vcc=3.3±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su\ (PD)}$	Power down set up time		0			ns
$t_{rec\ (PD)}$	Power down recovery time		t_{CR}			ns

(3) POWER DOWN CHARACTERISTICS

/S control mode