Supertex inc.

VN2106
VN2110

N-Channel Enhancement-Mode Vertical DMOS FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	Order Number / Package		
		TO-92	TO-236AB*	Die†
60V	4.0Ω	VN2106N3	–	—
100V	4.0Ω	—	VN2110K1	VN2110ND

†MIL visual screening available

*Same as SOT-23. All units shipped on 3,000 piece carrier tape reels.

Product marking for SOT-23:

N1A❋

where ❋ = 2-week alpha date code

Features

- ❏ Commercial and Military versions available
- ❏ Free from secondary breakdown
- ❏ Low power drive requirement
- ❏ Ease of paralleling
- ❏ Low C_{ISS} and fast switching speeds
- ❏ High input impedance and high gain

Applications

- ❏ Motor controls
- ❏ Amplifiers
- ❏ Power supply circuits
- ❏ Converters
- ❏ Switches
- ❏ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options

TO-236AB (SOT-23) top view

TO-92

Note: See Package Outline section for dimensions.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)†	I_D (pulsed)	Power Dissipation* @ $T_C = 25°C$	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}†	I_{DRM}
TO-92	0.3A	1.0A	1.0W	125	170	0.3A	1.0A
TO-236AB	0.2A	0.8A	0.36W ($T_A = 25°C$)	200	350	0.2A	0.8A

† I_D (continuous) is limited by max rated T_j.
* Total for package.

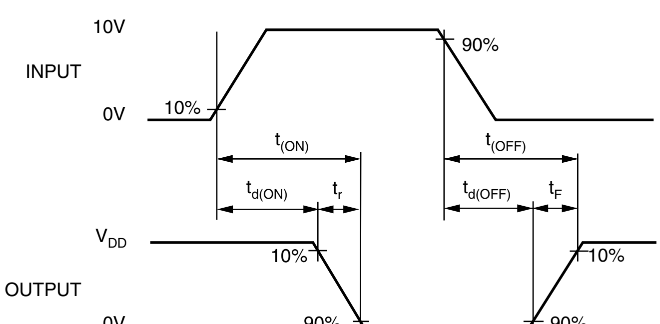
Electrical Characteristics (@ 25°C unless otherwise specified)

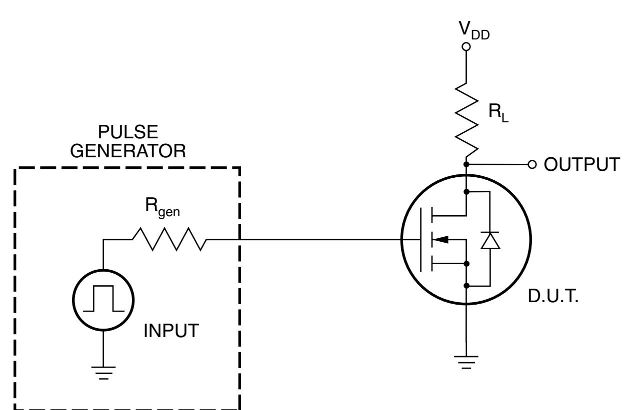
Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN2110	100			V	$I_D = 1mA$, $V_{GS} = 0V$
		VN2106	60				
$V_{GS(th)}$	Gate Threshold Voltage		0.8		2.4	V	$V_{GS} = V_{DS}$, $I_D = 1mA$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature			-3.8	-5.5	mV/°C	$V_{GS} = V_{DS}$, $I_D = 1mA$
I_{GSS}	Gate Body Leakage			0.1	100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
I_{DSS}	Zero Gate Voltage Drain Current				1	µA	$V_{GS} = 0V$, V_{DS} = Max Rating
					100	µA	$V_{GS} = 0V$, V_{DS} = 0.8 Max Rating $T_A = 125°C$
$I_{D(ON)}$	ON-State Drain Current		0.6			A	$V_{GS} = 10V$, $V_{DS} = 25V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			4.5	6.0	Ω	$V_{GS} = 5V$, $I_D = 75mA$
				3.0	4.0	Ω	$V_{GS} = 10V$, $I_D = 500mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			0.70	1.0	%/°C	$V_{GS} = 10V$, $I_D = 500mA$
G_{FS}	Forward Transconductance		150	400		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
C_{ISS}	Input Capacitance			35	50	pF	$V_{GS} = 0V$, $V_{DS} = 25V$, f = 1MHz
C_{OSS}	Common Source Output Capacitance			13	25		
C_{RSS}	Reverse Transfer Capacitance			4	5		
$t_{d(ON)}$	Turn-ON Delay Time			3	5	ns	$V_{DD} = 25V$ $I_D = 0.6A$ $R_{GEN} = 25\Omega$
t_r	Rise Time			5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time			6	9		
t_f	Fall Time			5	8		
V_{SD}	Diode Forward Voltage Drop			1.2	1.8	V	$I_{SD} = 0.6A$, $V_{GS} = 0V$
t_{rr}	Reverse Recovery Time			400		ns	$I_{SD} = 0.6A$, $V_{GS} = 0V$

Notes:

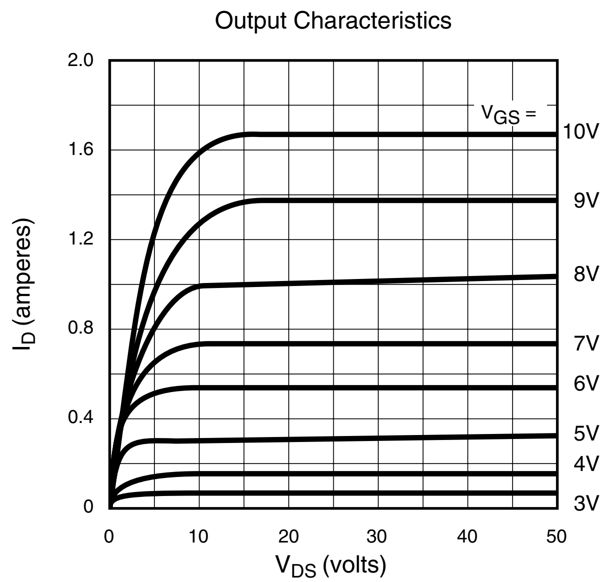
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

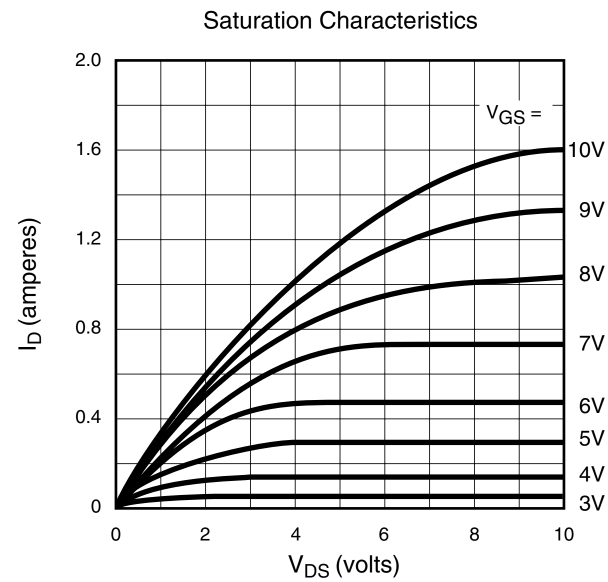
Switching Waveforms and Test Circuit

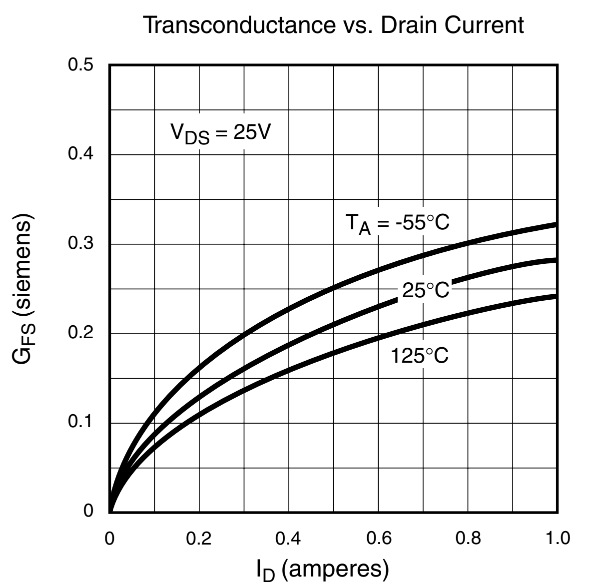


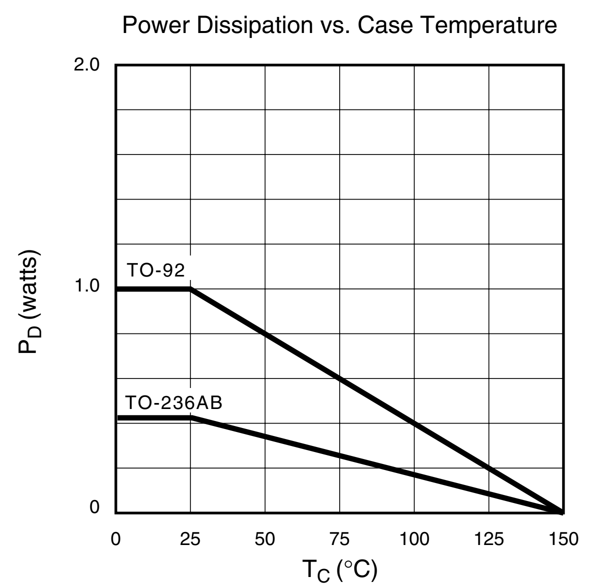


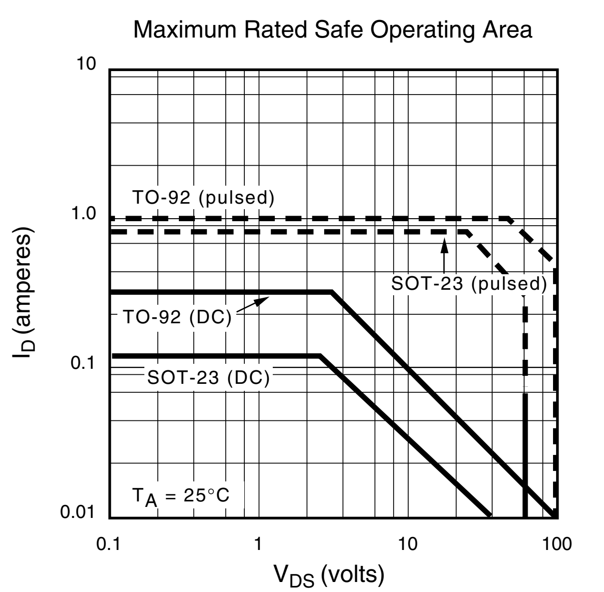
Typical Performance Curves

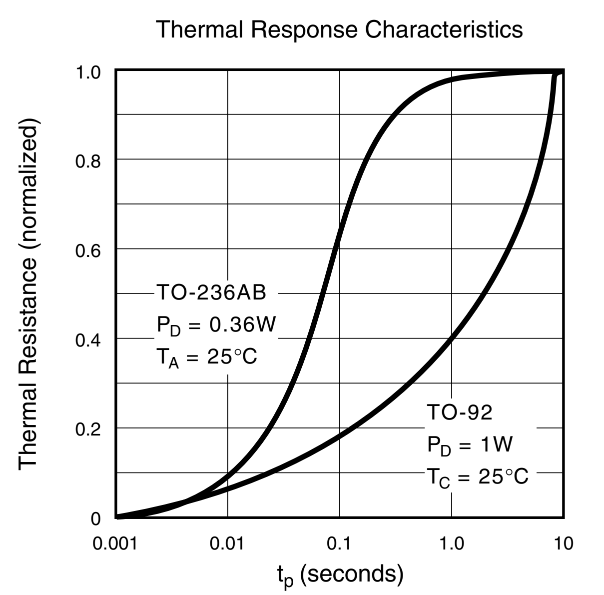






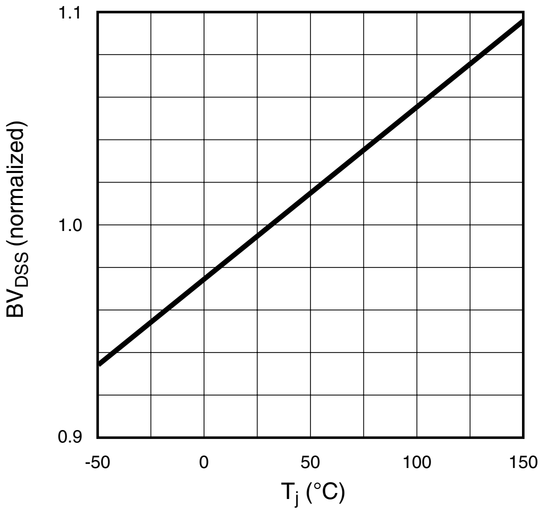




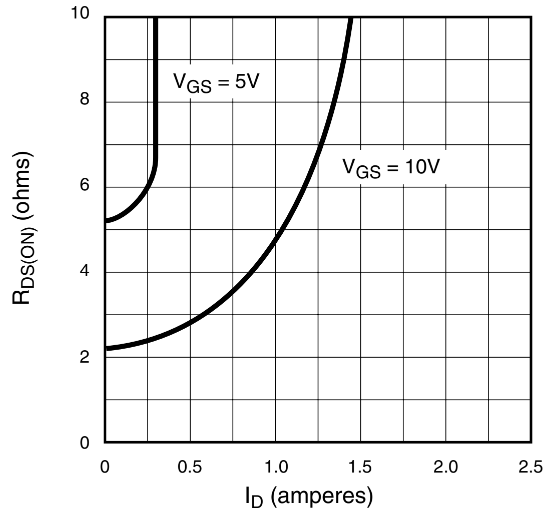


Typical Performance Curves

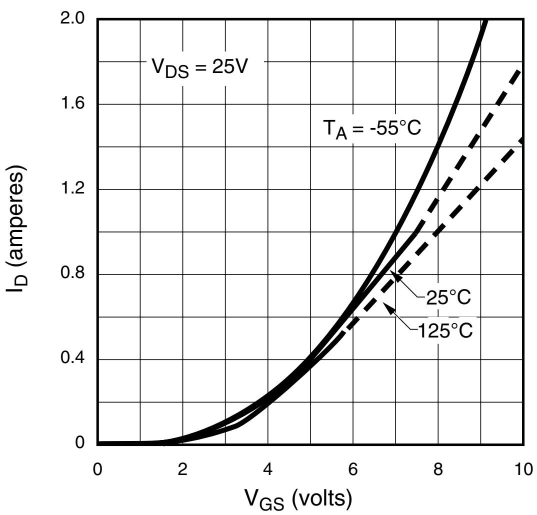
BV$_{DSS}$ Variation with Temperature



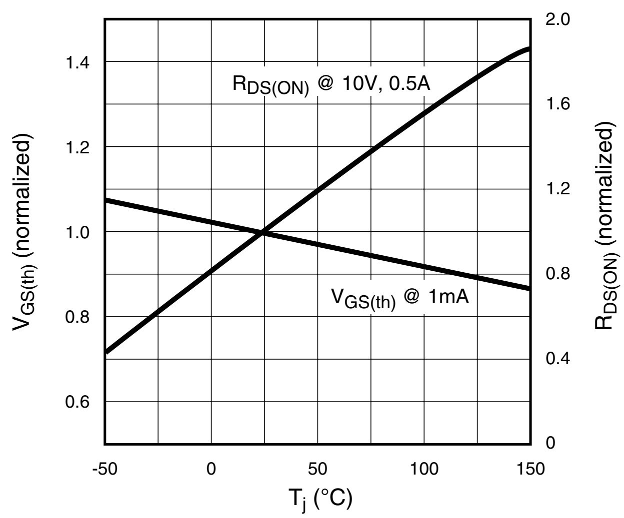
On-Resistance vs. Drain Current



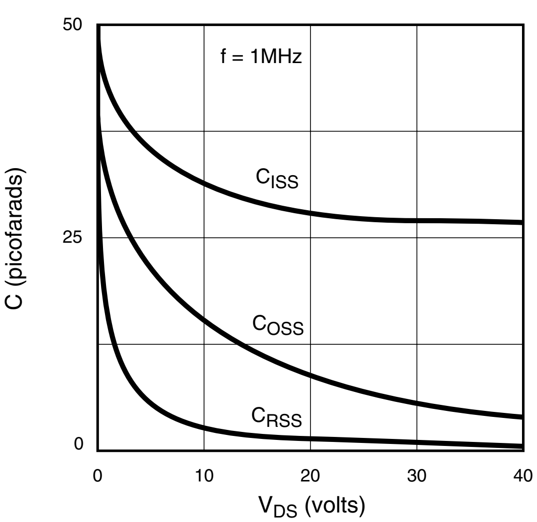
Transfer Characteristics



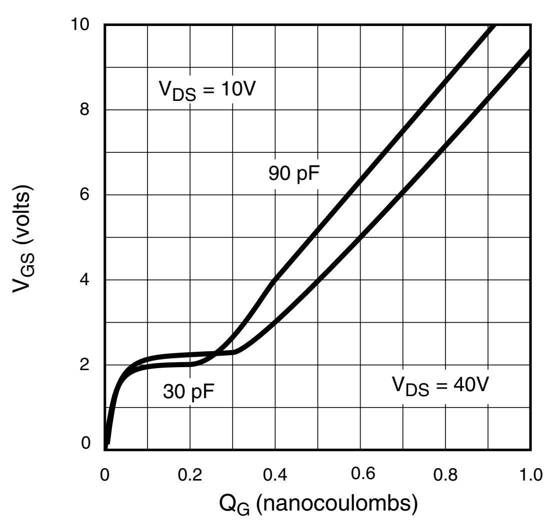
V$_{GS(th)}$ and R$_{DS(ON)}$ Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics



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