



# VNP35N07FI VNB35N07/VNV35N07

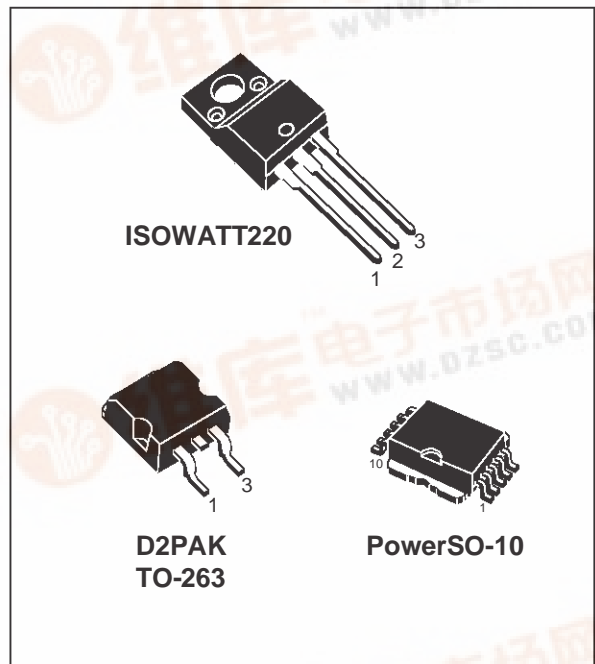
## "OMNIFET": FULLY AUTOPROTECTED POWER MOSFET

TYPE	V <sub>clamp</sub>	R <sub>DS(on)</sub>	I <sub>lim</sub>
VNP35N07FI	70 V	0.028 Ω	35 A
VNB35N07	70 V	0.028 Ω	35 A
VNV35N07	70 V	0.028 Ω	35 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET

### DESCRIPTION

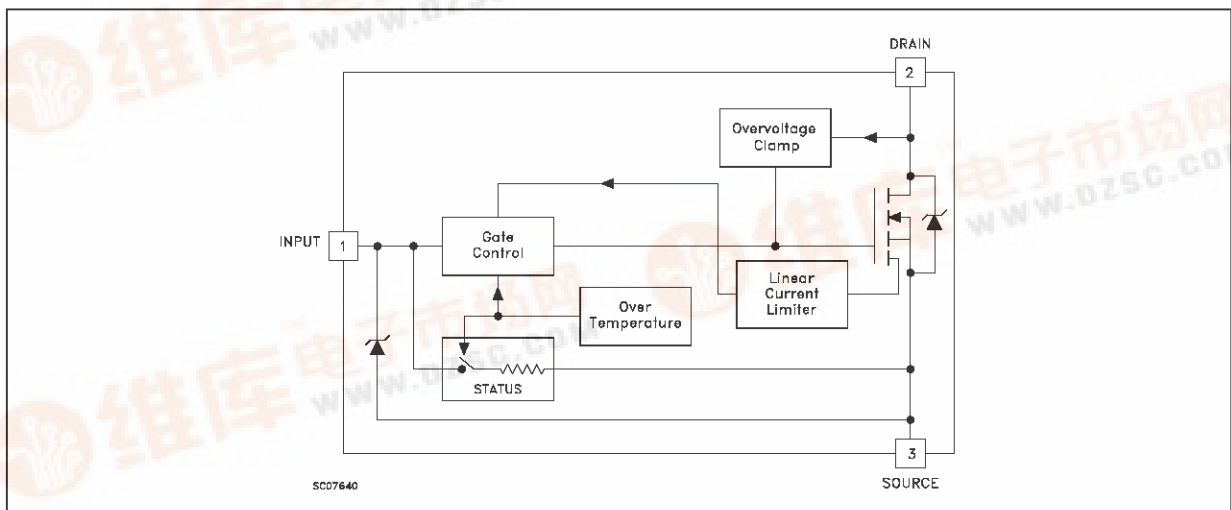
The VNP35N07FI, VNB35N07 and VNV35N07 are monolithic devices made using STMicroelectronics VIPower M0 Technology, intended for replacement of standard power MOSFETS in DC to 50 KHz applications. Built-in thermal shut-down, linear current limitation and overvoltage clamp protect the chip in harsh



environments.

Fault feedback can be detected by monitoring the voltage at the input pin.

### BLOCK DIAGRAM (\*)



(\*) PowerSO-10 Pin Configuration : INPUT = 6,7,8,9,10; SOURCE = 1,2,4,5; DRAIN = TAB

## VNP35N07FI-VNB35N07-VNV35N07

### ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value		Unit
		PowerSO-10 D2PAK	ISOWATT220	
V <sub>DS</sub>	Drain-source Voltage (V <sub>in</sub> = 0)	Internally Clamped		V
V <sub>in</sub>	Input Voltage	18		V
I <sub>D</sub>	Drain Current	Internally Limited		A
I <sub>R</sub>	Reverse DC Output Current	-50		A
V <sub>esd</sub>	Electrostatic Discharge (C= 100 pF, R=1.5 KΩ)	2000		V
P <sub>tot</sub>	Total Dissipation at T <sub>c</sub> = 25 °C	125	40	W
T <sub>j</sub>	Operating Junction Temperature	Internally Limited		°C
T <sub>c</sub>	Case Operating Temperature	Internally Limited		°C
T <sub>stg</sub>	Storage Temperature	-55 to 150		°C

### THERMAL DATA

		ISOWATT220	PowerSO-10	D2PAK	
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	3.12	1	1	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5	50	62.5	°C/W

### ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>CLAMP</sub>	Drain-source Clamp Voltage	I <sub>D</sub> = 200 mA V <sub>in</sub> = 0	60	70	80	V
V <sub>CLTH</sub>	Drain-source Clamp Threshold Voltage	I <sub>D</sub> = 2 mA V <sub>in</sub> = 0	55			V
V <sub>INCL</sub>	Input-Source Reverse Clamp Voltage	I <sub>in</sub> = -1 mA	-1		-0.3	V
I <sub>DSS</sub>	Zero Input Voltage Drain Current (V <sub>in</sub> = 0)	V <sub>DS</sub> = 13 V V <sub>in</sub> = 0 V <sub>DS</sub> = 25 V V <sub>in</sub> = 0			50 200	μA μA
I <sub>ISS</sub>	Supply Current from Input Pin	V <sub>DS</sub> = 0 V V <sub>in</sub> = 10 V		250	500	μA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>IN(th)</sub>	Input Threshold Voltage	V <sub>DS</sub> = V <sub>in</sub> I <sub>D</sub> + I <sub>in</sub> = 1 mA	0.8		3	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>in</sub> = 10 V I <sub>D</sub> = 18 A V <sub>in</sub> = 5 V I <sub>D</sub> = 18 A			0.028 0.035	Ω Ω

### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 13 V I <sub>D</sub> = 18 A	20	25		S
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 13 V f = 1 MHz V <sub>in</sub> = 0		980	1400	pF

**ELECTRICAL CHARACTERISTICS** (continued)**SWITCHING (\*\*)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 28\text{ V}$ $I_d = 18\text{ A}$		100	200	ns
$t_r$	Rise Time	$V_{gen} = 10\text{ V}$ $R_{gen} = 10\ \Omega$		350	600	ns
$t_{d(off)}$	Turn-off Delay Time	(see figure 3)		650	1000	ns
$t_f$	Fall Time			200	350	ns
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 28\text{ V}$ $I_d = 18\text{ A}$		500	800	ns
$t_r$	Rise Time	$V_{gen} = 10\text{ V}$ $R_{gen} = 1000\ \Omega$		2.7	4.2	$\mu\text{s}$
$t_{d(off)}$	Turn-off Delay Time	(see figure 3)		10	16	$\mu\text{s}$
$t_f$	Fall Time			4.3	6.5	$\mu\text{s}$
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 28\text{ V}$ $I_D = 18\text{ A}$ $V_{in} = 10\text{ V}$ $R_{gen} = 10\ \Omega$		60		A/ $\mu\text{s}$
$Q_i$	Total Input Charge	$V_{DD} = 12\text{ V}$ $I_D = 18\text{ A}$ $V_{in} = 10\text{ V}$		100		nC

**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 18\text{ A}$ $V_{in} = 0$			1.6	V
$t_{rr}(**)$	Reverse Recovery Time	$I_{SD} = 18\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 25\text{ }^\circ\text{C}$		250		ns
$Q_{rr}(**)$	Reverse Recovery Charge	(see test circuit, figure 5)		1		$\mu\text{C}$
$I_{RRM}(**)$	Reverse Recovery Current			8		A

**PROTECTION**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{lim}$	Drain Current Limit	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$	25 25	35 35	45 45	A A
$t_{dim}(**)$	Step Response Current Limit	$V_{in} = 10\text{ V}$ $V_{in} = 5\text{ V}$		35 70	60 140	$\mu\text{s}$ $\mu\text{s}$
$T_{jsh}(**)$	Overtemperature Shutdown		150			$^\circ\text{C}$
$T_{jrs}(**)$	Overtemperature Reset		135			$^\circ\text{C}$
$I_{gf}(**)$	Fault Sink Current	$V_{in} = 10\text{ V}$ $V_{DS} = 13\text{ V}$ $V_{in} = 5\text{ V}$ $V_{DS} = 13\text{ V}$		50 20		mA mA
$E_{as}(**)$	Single Pulse Avalanche Energy	starting $T_j = 25\text{ }^\circ\text{C}$ $V_{DD} = 20\text{ V}$ $V_{in} = 10\text{ V}$ $R_{gen} = 1\text{ K}\Omega$ $L = 10\text{ mH}$	2.5			J

(\*) Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

(\*\*) Parameters guaranteed by design/characterization

### PROTECTION FEATURES

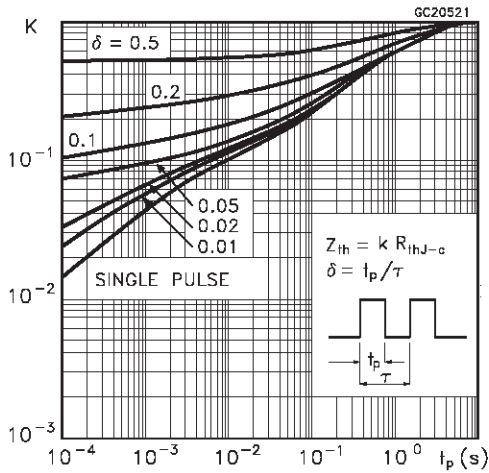
During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current ( $I_{ISS}$ ) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

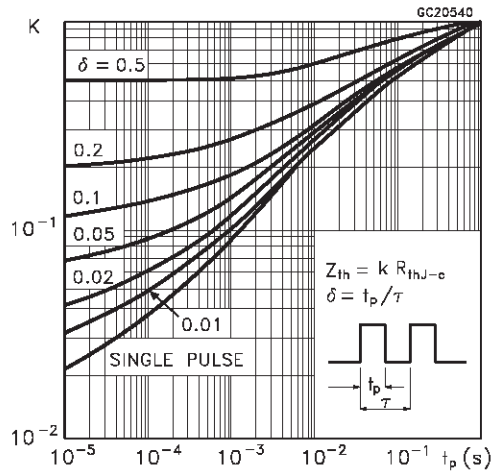
- **OVERVOLTAGE CLAMP PROTECTION:** internally set at 70V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- **LINEAR CURRENT LIMITER CIRCUIT:** limits the drain current  $I_D$  to  $I_{lim}$  whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold  $T_{jsh}$ .
- **OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION:** these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs at minimum 150°C. The device is automatically restarted when the chip temperature falls below 135°C.
- **STATUS FEEDBACK:** In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 100 Ω. The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in  $R_{DS(on)}$ ).

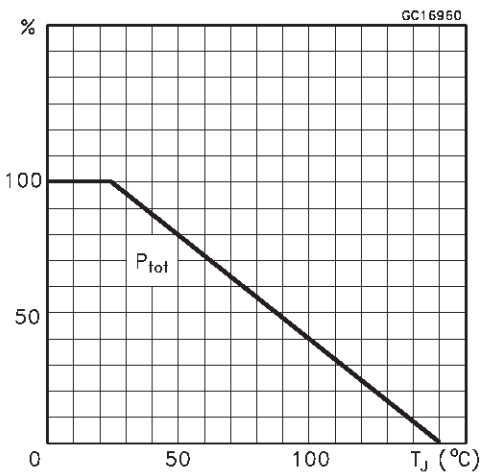
Thermal Impedance For ISOWATT220



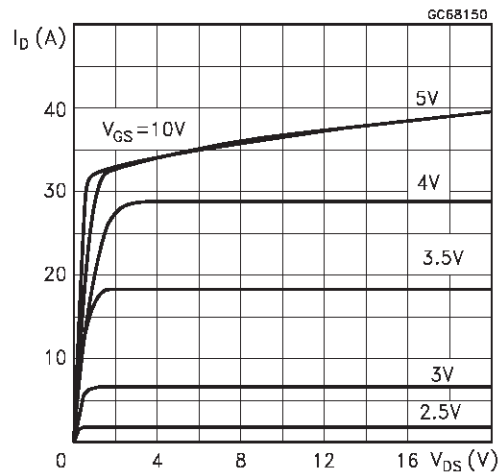
Thermal Impedance For D2PAK / PowerSO-10



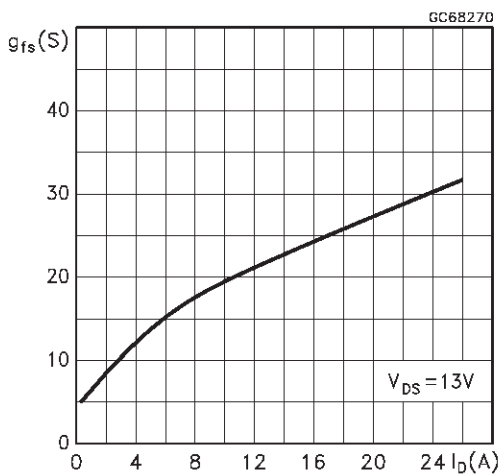
Derating Curve



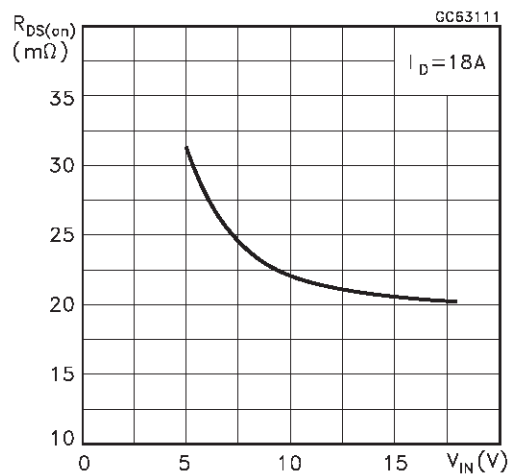
Output Characteristics



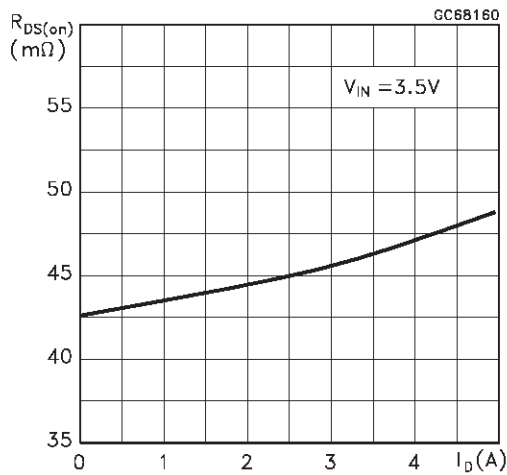
Transconductance



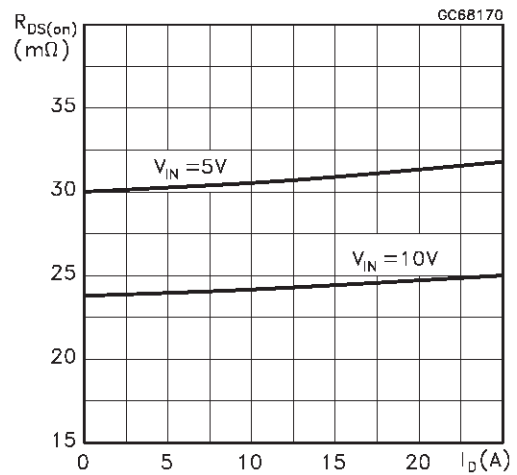
Static Drain-Source On Resistance vs Input Voltage



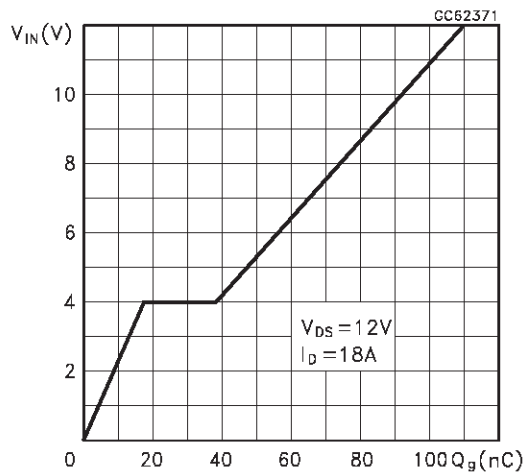
Static Drain-Source On Resistance



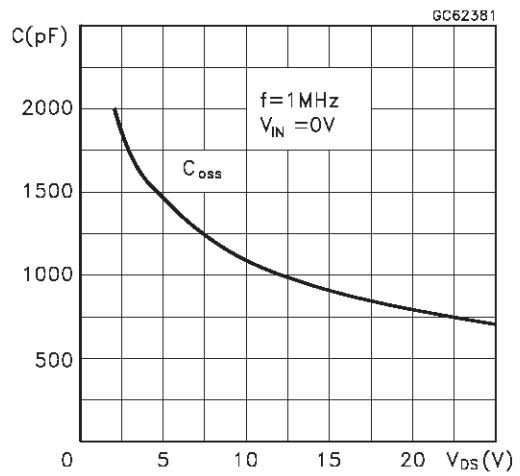
Static Drain-Source On Resistance



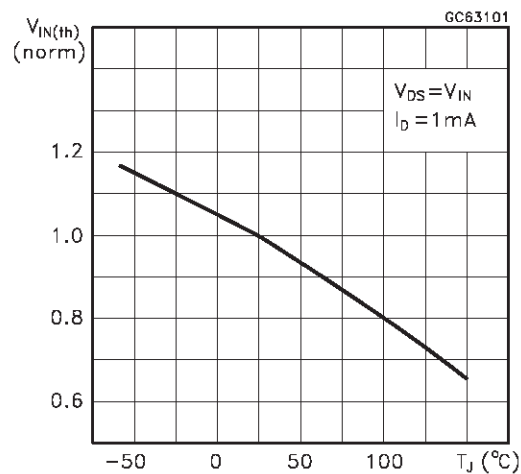
Input Charge vs Input Voltage



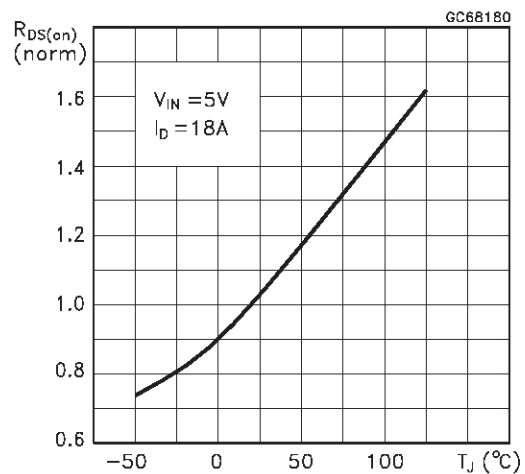
Capacitance Variations



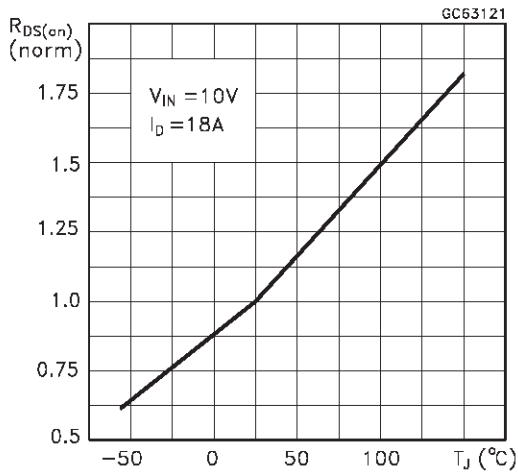
Normalized Input Threshold Voltage vs Temperature



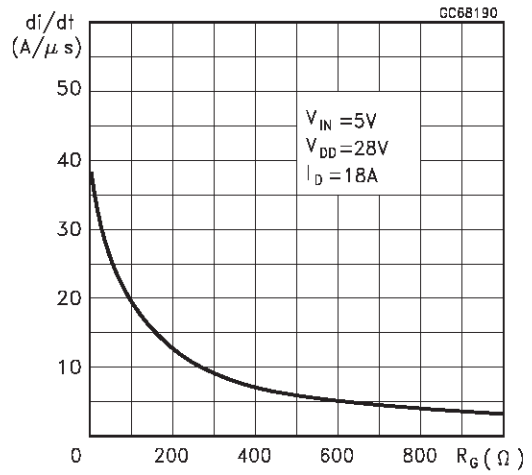
Normalized On Resistance vs Temperature



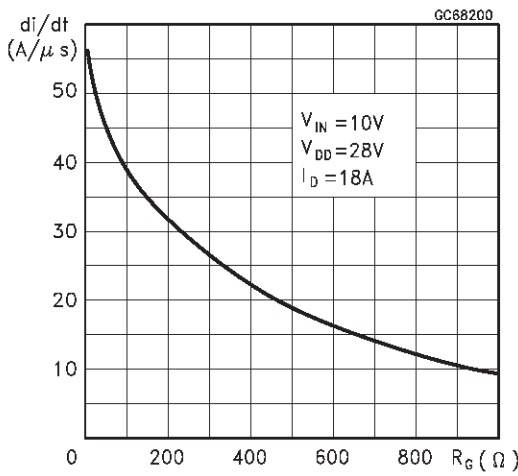
Normalized On Resistance vs Temperature



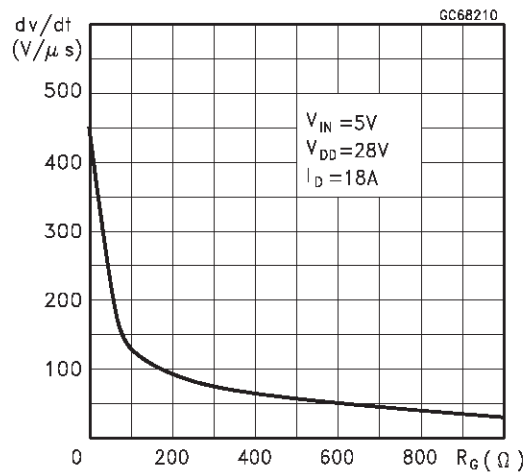
Turn-on Current Slope



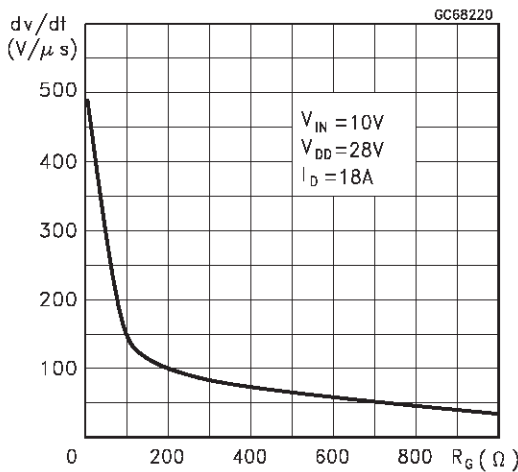
Turn-on Current Slope



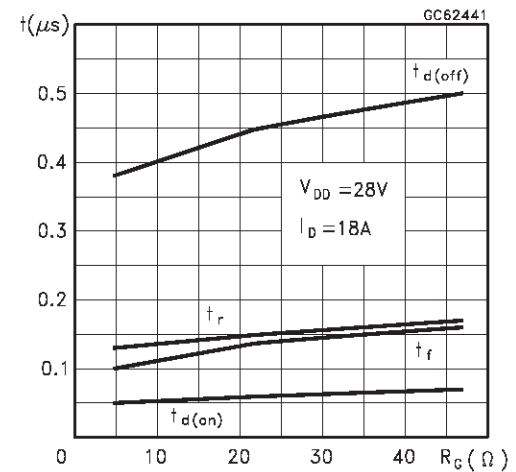
Turn-off Drain-Source Voltage Slope



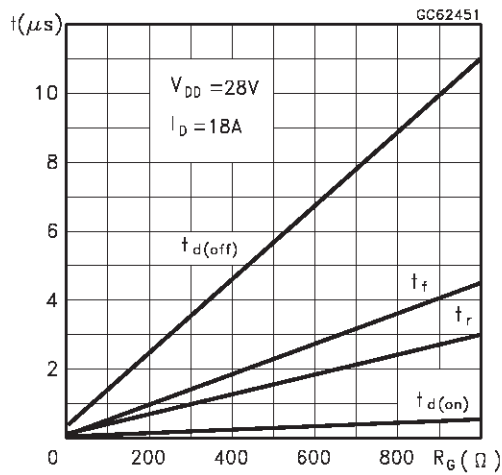
Turn-off Drain-Source Voltage Slope



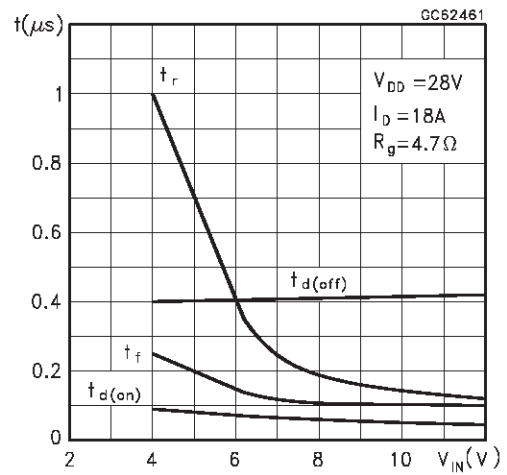
Switching Time Resistive Load



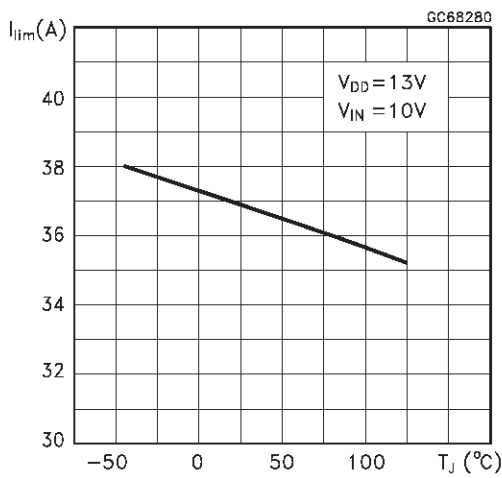
Switching Time Resistive Load



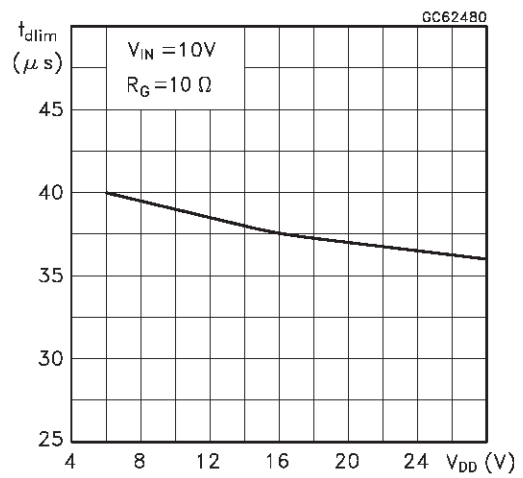
Switching Time Resistive Load



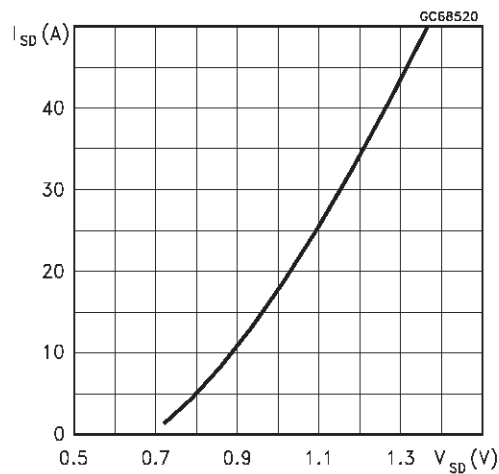
Current Limit vs Junction Temperature



Step Response Current Limit

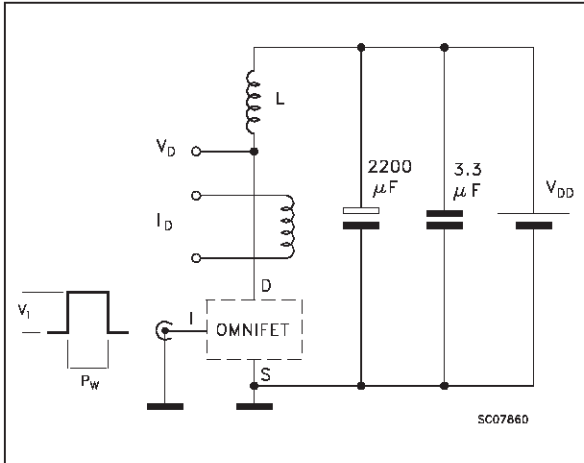


Source Drain Diode Forward Characteristics

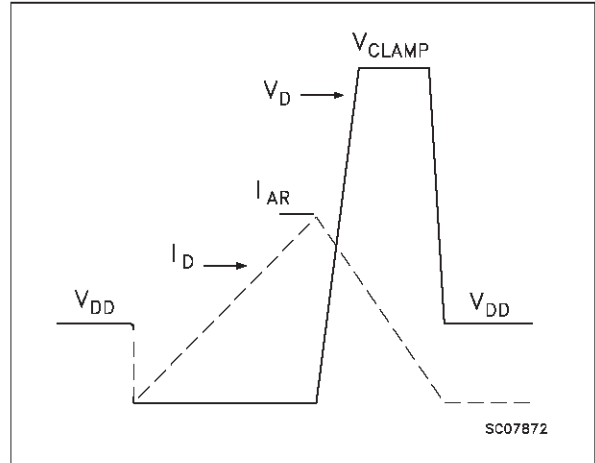




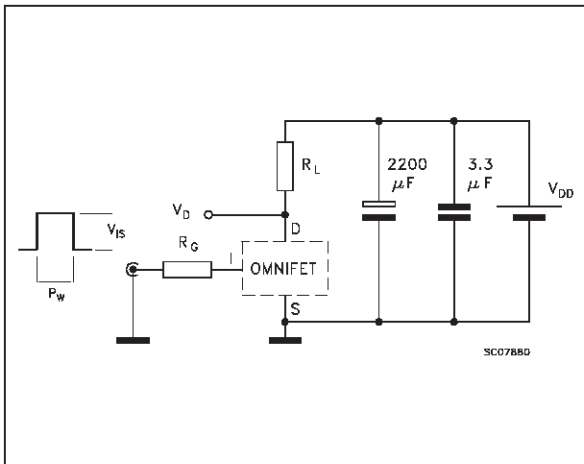
**Fig. 1: Unclamped Inductive Load Test Circuits**



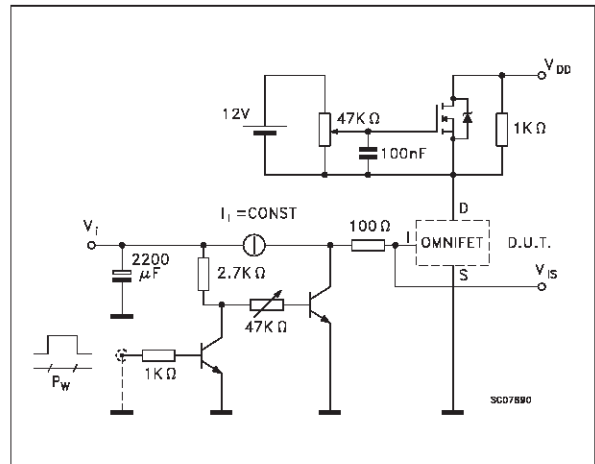
**Fig. 2: Unclamped Inductive Waveforms**



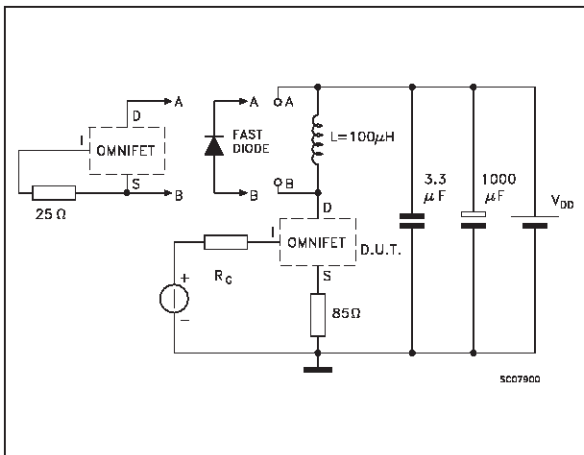
**Fig. 3: Switching Times Test Circuits For Resistive Load**



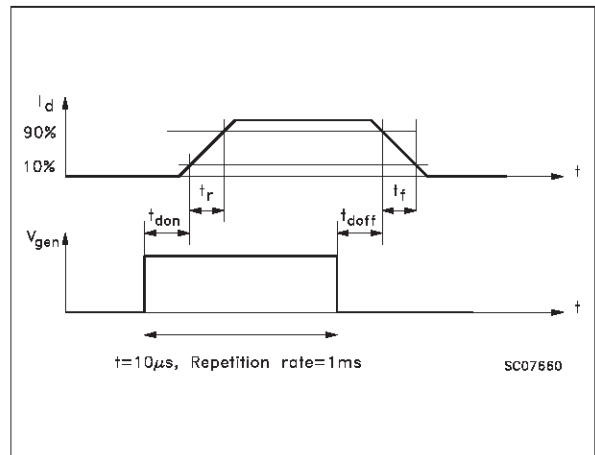
**Fig. 4: Input Charge Test Circuit**



**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**

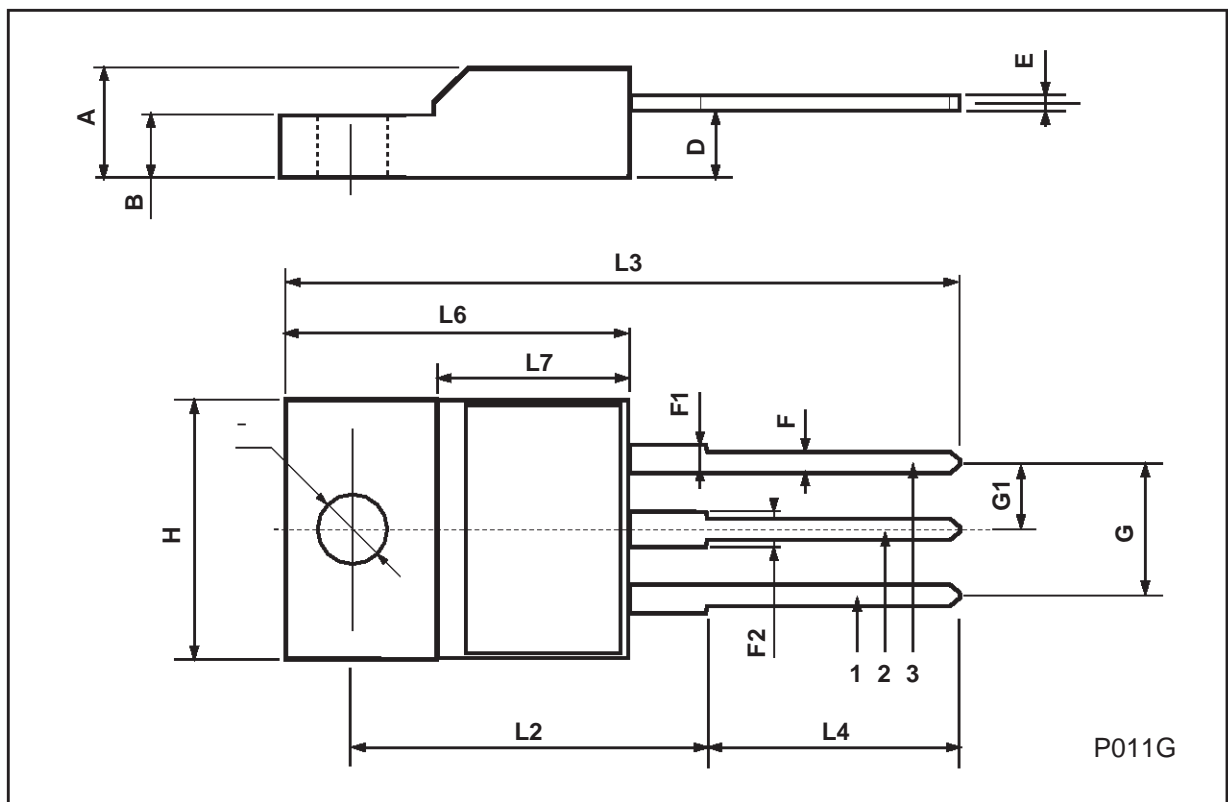


**Fig. 6: Waveforms**



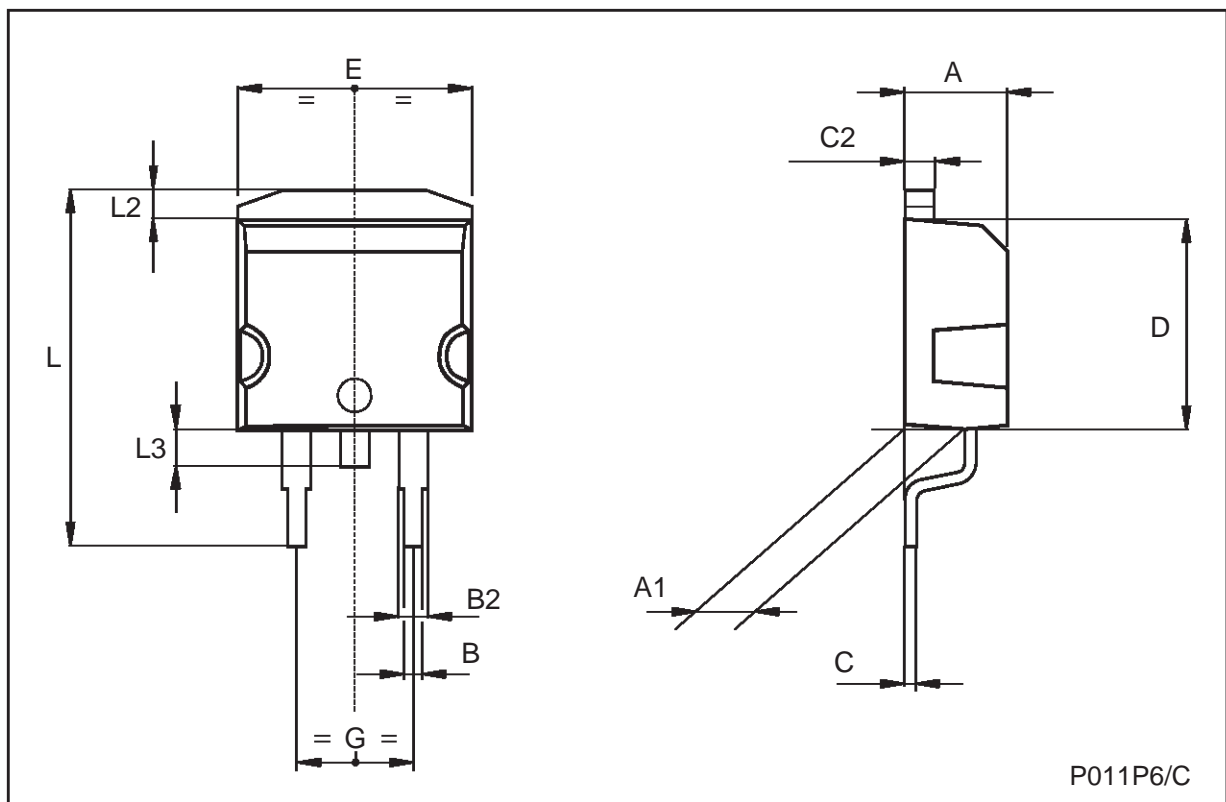
**ISOWATT220 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.4		0.7	0.015		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126



**TO-263 (D2PAK) MECHANICAL DATA**

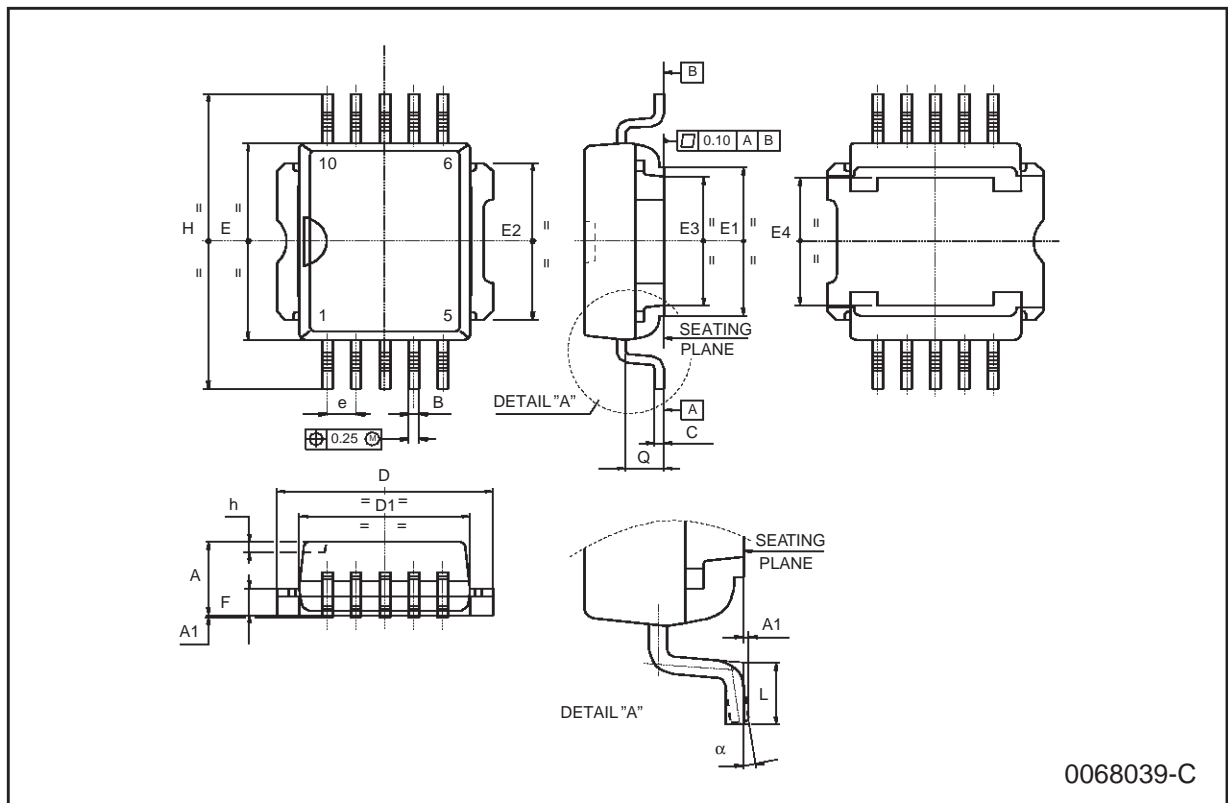
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.3		4.6	0.169		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.25		1.4	0.049		0.055
C	0.45		0.6	0.017		0.023
C2	1.21		1.36	0.047		0.053
D	8.95		9.35	0.352		0.368
E	10		10.28	0.393		0.404
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



P011P6/C

**PowerSO-10 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
c	0.35		0.55	0.013		0.022
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E1	7.20		7.40	0.283		0.291
E2	7.20		7.60	0.283		0.300
E3	6.10		6.35	0.240		0.250
E4	5.90		6.10	0.232		0.240
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
H	13.80		14.40	0.543		0.567
h		0.50			0.002	
L	1.20		1.80	0.047		0.071
q		1.70			0.067	
$\alpha$	0°		8°			



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specification mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a trademark of STMicroelectronics

© 1998 STMicroelectronics – Printed in Italy – All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - France - Germany - Italy - Japan - Korea - Malaysia - Malta - Mexico - Morocco - The Netherlands -  
Singapore - Spain - Sweden - Switzerland - Taiwan - Thailand - United Kingdom - U.S.A.