



VNH100N04

“OMNIFET”: FULLY AUTOPROTECTED POWER MOSFET

TARGET DATA

TYPE	V _{clamp}	R _{DS(on)}	I _{lim}
VNH100N04	42 V	0.012 Ω	100 A

- LINEAR CURRENT LIMITATION
- THERMAL SHUT DOWN
- SHORT CIRCUIT PROTECTION
- INTEGRATED CLAMP
- LOW CURRENT DRAWN FROM INPUT PIN
- DIAGNOSTIC FEEDBACK THROUGH INPUT PIN
- ESD PROTECTION
- DIRECT ACCESS TO THE GATE OF THE POWER MOSFET (ANALOG DRIVING)
- COMPATIBLE WITH STANDARD POWER MOSFET
- STANDARD TO-218 PACKAGE



TO-218

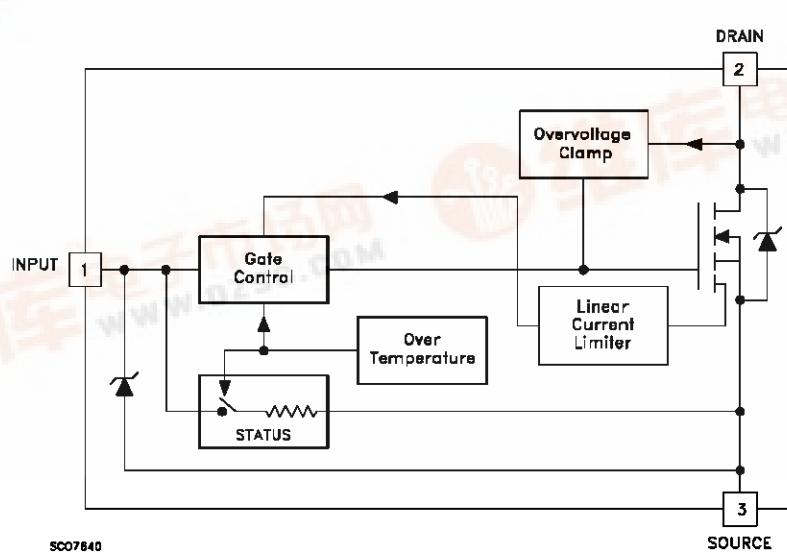
DESCRIPTION

The VNH100N04 is a monolithic device made using SGS-THOMSON Vertical Intelligent Power M0 Technology, intended for replacement of standard power MOSFETs in DC to 50 KHz applications. Buit-in thermal shut-down, linear

current limitation and overvoltage clamp protect the chip in harsh enviroments.

Fault feedback can be detected by monitoring the voltage at the input pin.

BLOCK DIAGRAM



VNH100N04

ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{in} = 0$)	Internally Clamped	V
V_{in}	Input Voltage	18	V
I_D	Drain Current	Internally Limited	A
I_R	Reverse DC Output Current	-50	A
V_{esd}	Electrostatic Discharge ($C = 100 \text{ pF}$, $R = 1.5 \text{ k}\Omega$)	2000	V
P_{tot}	Total Dissipation at $T_c = 25 \text{ }^\circ\text{C}$	208	W
T_j	Operating Junction Temperature	Internally Limited	$^\circ\text{C}$
T_c	Case Operating Temperature	Internally Limited	$^\circ\text{C}$
T_{stg}	Storage Temperature	-55 to 150	$^\circ\text{C}$

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	0.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	30	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25 \text{ }^\circ\text{C}$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CLAMP}	Drain-source Clamp Voltage	$I_D = 30 \text{ A}$ $V_{in} = 0$	36	42	48	V
V_{CLTH}	Drain-source Clamp Threshold Voltage	$I_D = 2 \text{ mA}$ $V_{in} = 0$	35			V
V_{INCL}	Input-Source Reverse Clamp Voltage	$I_{in} = -1 \text{ mA}$	-1		-0.3	V
I_{DSS}	Zero Input Voltage Drain Current ($V_{in} = 0$)	$V_{DS} = 13 \text{ V}$ $V_{DS} = 25 \text{ V}$			50 200	μA μA
I_{ISS}	Supply Current from Input Pin	$V_{DS} = 0 \text{ V}$ $V_{in} = 10 \text{ V}$		250	500	μA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{IS(th)}$	Input Threshold Voltage	$V_{DS} = V_{in}$ $I_D = 1 \text{ mA}$	0.8		3	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{in} = 10 \text{ V}$ $I_D = 30 \text{ A}$ $V_{in} = 5 \text{ V}$ $I_D = 30 \text{ A}$			0.012 0.015	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} \text{ (*)}$	Forward Transconductance	$V_{DS} = 13 \text{ V}$ $I_D = 30 \text{ A}$		40		S
C_{oss}	Output Capacitance	$V_{DS} = 13 \text{ V}$ $f = 1 \text{ MHz}$ $V_{in} = 0$		1800	3000	pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15 \text{ V}$ $I_d = 30 \text{ A}$ $V_{gen} = 10 \text{ V}$ $R_{gen} = 10 \Omega$		100 400	TBD TBD	ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	(see figure 3)		900 400	TBD TBD	ns ns
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15 \text{ V}$ $I_d = 30 \text{ A}$ $V_{gen} = 10 \text{ V}$ $R_{gen} = 10 \Omega$			TBD	ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$T_j = 125 \text{ }^\circ\text{C}$ (see figure 3)			TBD TBD	ns ns
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 15 \text{ V}$ $I_d = 30 \text{ A}$ $V_{gen} = 10 \text{ V}$ $R_{gen} = 1000 \Omega$			TBD TBD	μs μs
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	(see figure 3)			TBD TBD	μs μs
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 15 \text{ V}$ $I_d = 30 \text{ A}$ $V_{in} = 10 \text{ V}$		TBD		$\text{A}/\mu\text{s}$
Q_g	Total Gate Charge	$V_{DD} = 12 \text{ V}$ $I_D = 30 \text{ A}$ $V_{in} = 10 \text{ V}$		TBD		nC

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 30 \text{ A}$ $V_{in} = 0$			TBD	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 30 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$		TBD		ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = \text{V}$ $T_j = 150 \text{ }^\circ\text{C}$		TBD		μC
I_{RRM}	Reverse Recovery Current	(see test circuit, figure 5)		TBD		A

PROTECTION

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{lim}	Drain Current Limit	$V_{in} = 10 \text{ V}$ $V_{DS} = 13 \text{ V}$	70	100	140	A
t_{dlim}	Step Response Current Limit	$V_{in} = 10 \text{ V}$ $V_{DS} = 13 \text{ V}$			TBD	μs
T_{jsh}	Overtemperature Shutdown		150	170	190	$^\circ\text{C}$
T_{jrs}	Overtemperature Reset		135			$^\circ\text{C}$
I_{gf}	Fault Sink Current	$V_{in} = 10 \text{ V}$ $V_{DS} = 13 \text{ V}$		50		mA
E_{as}	Single Pulse Avalanche Energy	starting $T_j = 25 \text{ }^\circ\text{C}$ $V_{DD} = 20 \text{ V}$ $V_{in} = 10 \text{ V}$ $R_{gen} = 1 \text{ K}\Omega$ $L = \text{mH}$	TBD			J

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

PROTECTION FEATURES

During normal operation, the Input pin is electrically connected to the gate of the internal power MOSFET. The device then behaves like a standard power MOSFET and can be used as a switch from DC to 50 KHz. The only difference from the user's standpoint is that a small DC current (I_{iss}) flows into the Input pin in order to supply the internal circuitry.

The device integrates:

- OVERVOLTAGE CLAMP PROTECTION: internally set at 42V, along with the rugged avalanche characteristics of the Power MOSFET stage give this device unrivalled ruggedness and energy handling capability. This feature is mainly important when driving inductive loads.
- LINEAR CURRENT LIMITER CIRCUIT: limits the drain current I_d to I_{lim} whatever the Input pin voltage. When the current limiter is active, the device operates in the linear region, so power dissipation may exceed the capability of the heatsink. Both case and junction temperatures increase, and if this phase lasts long enough, junction temperature may reach the overtemperature threshold T_{jsh} .

– OVERTEMPERATURE AND SHORT CIRCUIT PROTECTION: these are based on sensing the chip temperature and are not dependent on the input voltage. The location of the sensing element on the chip in the power stage area ensures fast, accurate detection of the junction temperature. Overtemperature cutout occurs in the range 150 to 190°C, a typical value being 170°C. The device is automatically restarted when the chip temperature falls below 135°C.

- STATUS FEEDBACK: In the case of an overtemperature fault condition, a Status Feedback is provided through the Input pin. The internal protection circuit disconnects the input from the gate and connects it instead to ground via an equivalent resistance of 200 Ω. The failure can be detected by monitoring the voltage at the Input pin, which will be close to ground potential.

Additional features of this device are ESD protection according to the Human Body model and the ability to be driven from a TTL Logic circuit (with a small increase in $R_{DS(on)}$).

Fig. 1: Unclamped Inductive Load Test Circuits

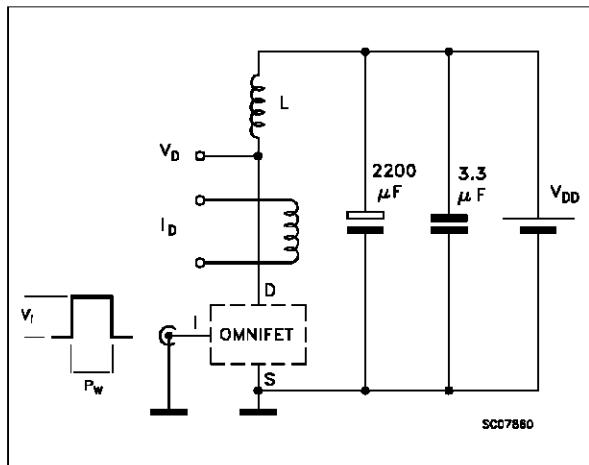


Fig. 2: Unclamped Inductive Waveforms

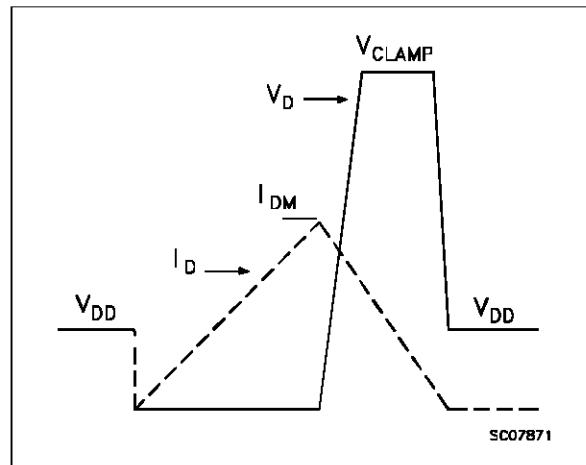


Fig. 3: Switching Times Test Circuits For Resistive Load

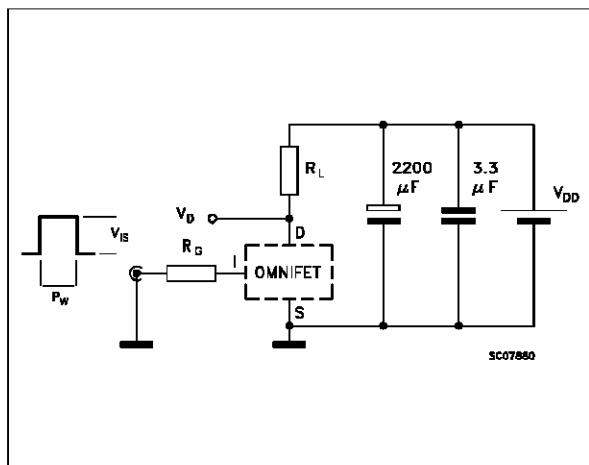


Fig. 4: Input Charge Test Circuit

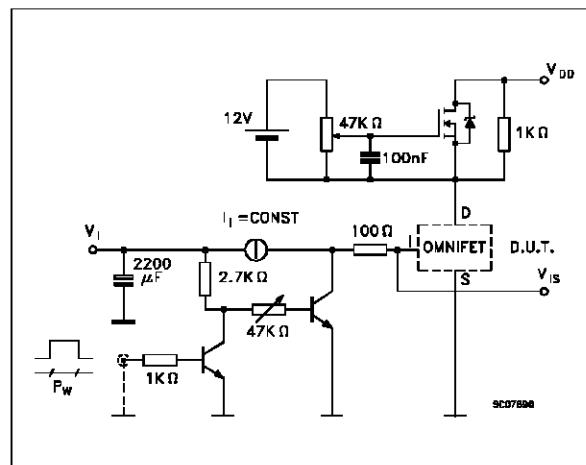


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times

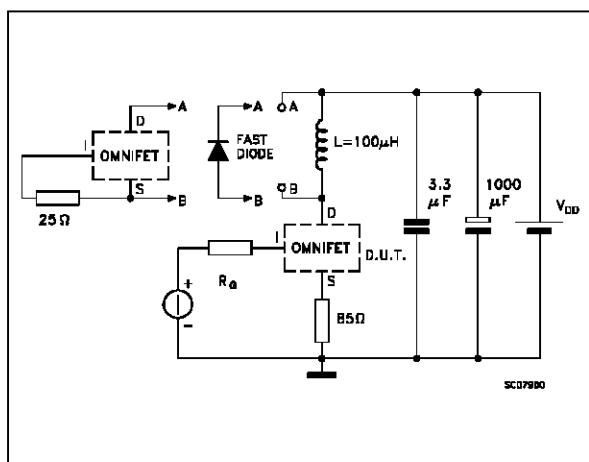
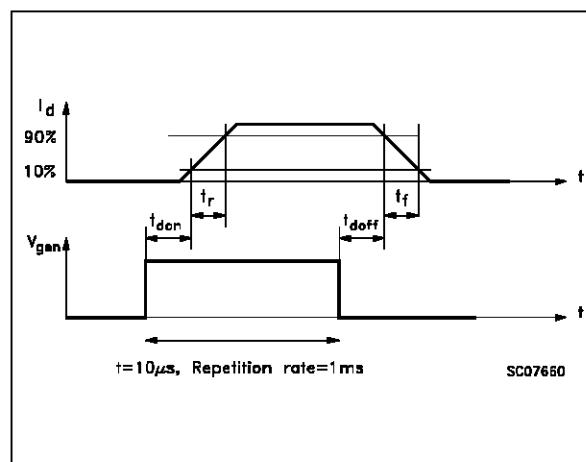


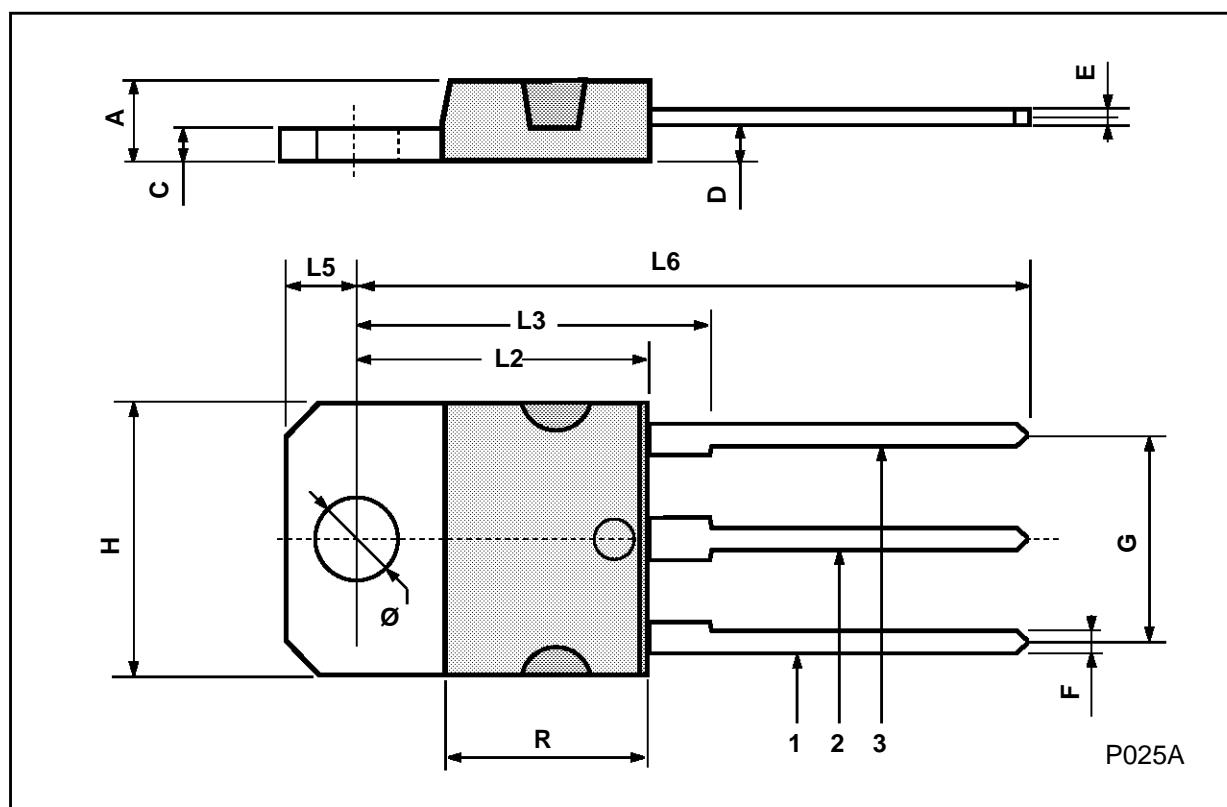
Fig. 6: Waveforms



VNH100N04

TO-218 (SOT-93) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		4.9	0.185		0.193
C	1.17		1.37	0.046		0.054
D		2.5			0.098	
E	0.5		0.78	0.019		0.030
F	1.1		1.3	0.043		0.051
G	10.8		11.1	0.425		0.437
H	14.7		15.2	0.578		0.598
L2	—		16.2	—		0.637
L3		18			0.708	
L5	3.95		4.15	0.155		0.163
L6		31			1.220	
R	—		12.2	—		0.480
Ø	4		4.1	0.157		0.161



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