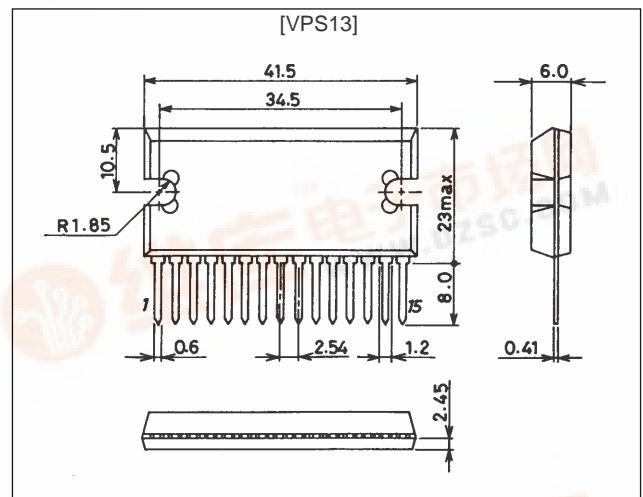Ordering number : EN5548A

VPS13

CRT Display Video Output Amplifier, High-Voltage/Wideband Amplifier

Features

- High output voltage and wide bandwidth; optimal for use in f_H (horizontal deflection frequency) = 100 kHz class monitors.
  (f = 130 MHz –3 dB at V_{OUT} = 40 Vp-p)
- SIP molded 15-pin package houses three amplifier channels.

Package Dimensions

unit: mm

2127A

[VPS13]

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		90	V
	V_{BB} max		15	V
Allowable power dissipation	Pd max	With an ideal heat sink at Tc = 25°C	30	W
Maximum junction temperature	Tj max		150	°C
Maximum case temperature	Tc max		100	°C
Storage temperature	Tstg		−20 to +110	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage	V_{CC}		80	V
	V_{BB}		10	V

Electrical Characteristics at Ta = 25°C (for a single channel)

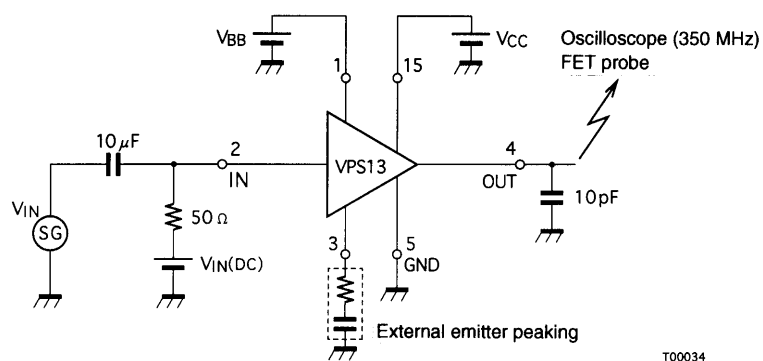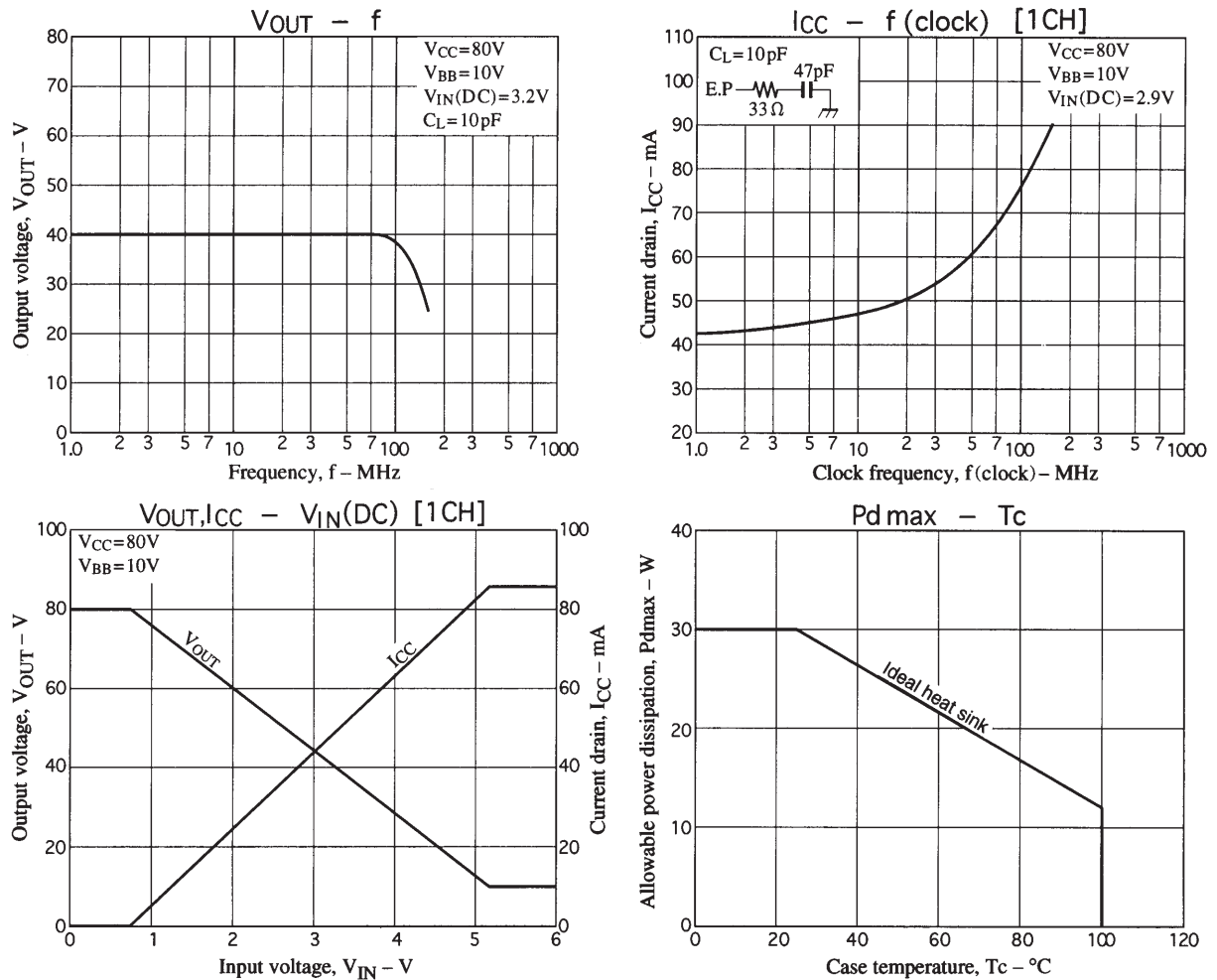| Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
Frequency band (–3 dB)	f_c	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF V_{IN} (DC) = 3.2 V, V_{OUT} (p-p) = 40 V		130		MHz
Impulse response	t_r	V_{CC} = 80 V, V_{BB} = 10 V, C_L = 10 pF		3.5		ns
	t_f	V_{IN} (DC) = 3.2 V, V_{OUT} (p-p) = 40 V		2.9		ns
Voltage gain	VG (DC)		13	15	17	double
Current drain	I_{CC}(1)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.9 V, f = 10 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		47		mA
	I_{CC}(2)	V_{CC} = 80 V, V_{BB} = 10 V, V_{IN} (DC) = 2.9 V, f = 130 MHz clock, C_L = 10 pF, V_{OUT} (p-p) = 40 V		85		mA

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Internal Equivalent Circuit

Unit (resistance: Ω)

T00035
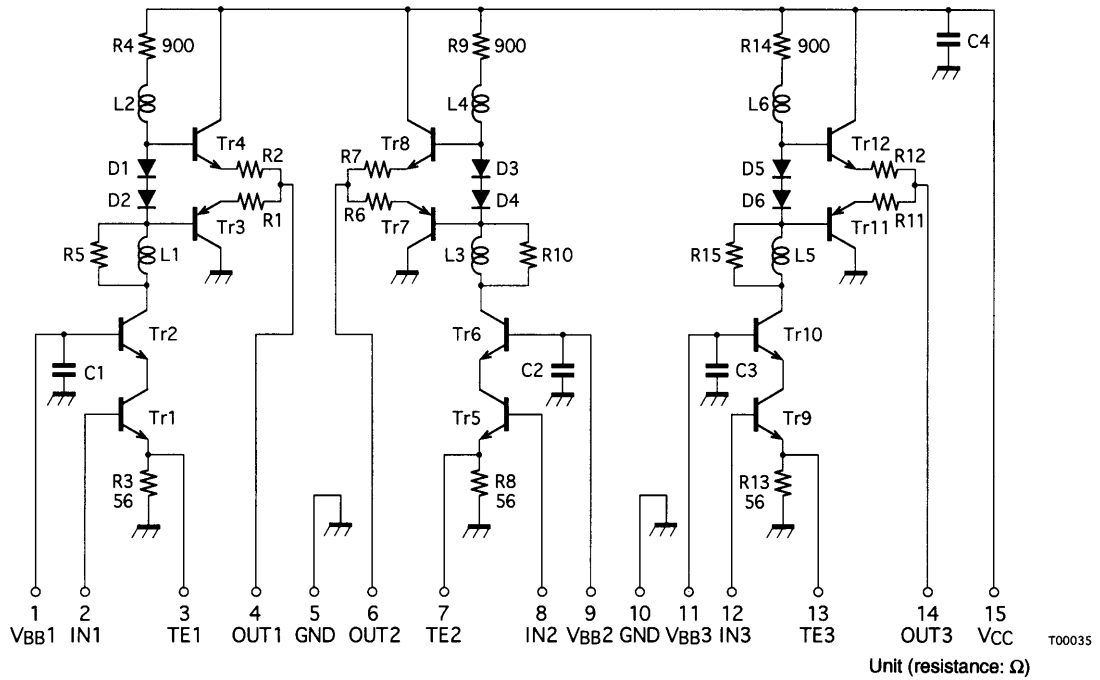
Test Circuit (for a single channel)

T00034

$V_{OUT} - f$

$V_{CC}=80V$
$V_{BB}=10V$
$V_{IN}(DC)=3.2V$
$C_L=10pF$

Output voltage, $V_{OUT} - V$

Frequency, $f - MHz$

$I_{CC} - f$ (clock) [1CH]

$C_L=10pF$
E.P — 33Ω — 47pF

$V_{CC}=80V$
$V_{BB}=10V$
$V_{IN}(DC)=2.9V$

Current drain, $I_{CC} - mA$

Clock frequency, f (clock) $- MHz$

$V_{OUT}, I_{CC} - V_{IN}(DC)$ [1CH]

$V_{CC}=80V$
$V_{BB}=10V$

V_{OUT}
I_{CC}

Output voltage, $V_{OUT} - V$

Current drain, $I_{CC} - mA$

Input voltage, $V_{IN} - V$

Pd max $-$ Tc

Ideal heat sink

Allowable power dissipation, $Pdmax - W$

Case temperature, $Tc - °C$

Thermal Design

Since the VPS13 includes three channels as shown in the circuit diagram on page 2, we first consider a single channel. The chip temperature of each transistor under actual operating conditions is determined using the following formula.

$$Tj = (Tri) = \theta j\text{-}c\ (Tri) \times Pc\ (Tri) + \Delta Tc + Ta\ (°C) \dots\dots\dots\dots(1)$$

θj-c (Tri) : Thermal resistance of an individual transistor
Pc(Tri)   : Collector loss for an individual transistor
ΔTc : Case temperature rise
Ta   : Ambient temperature

The θj-c (Tri) for each chip is: θj-c (Tr1) = 35°C/W

$$\theta j\text{-}c\ (Tr2)\ to\ (Tr4) = 30°C/W \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(2)$$

Although the loss for each transistor in a video pack varies with frequency and is not uniform, if we assume the maximum operating frequency, f = 130 MHz (clock), then the chip with the largest loss will be transistor 3 (Tr3) of the emitter-follower stage. From the Pd-f (clock) figure we see that loss will be 22% of the total loss for a single channel:

$$Pc\ (\text{emitter-follower stage})_{(f = 130\ MHz)} = Pd\ (1ch)_{(f = 130\ MHz)} \times 0.22\ [W] \quad (3)$$

Here, we must select a heat sink with a capacity θh such that the Tj of these transistors does not exceed 150°C. Equation (4) below gives the relationship between θh and ΔTc.

$$\Delta Tc = Pd\ (Total) \times \theta h \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots(4)$$

The required θh is calculated using this equation and equation (1).

VPS13 Thermal Design Example

Conditions: Using an $f_H = 100$ kHz class monitor, $f_V = 130$ MHz (clock)

$V_{CC} = 80$ V, $V_{BB} = 10$ V, $V_{OUT} = 40$ Vp-p ($C_L = 10$ pF)

Here we consider the case where this class of monitor is operated up to Ta = 60°C at a maximum clock frequency of f = 130 MHz.

As mentioned previously, the chip with the largest loss is transistor 3 (Tr3) of the emitter-follower stage. Determining that value gives:

Pc (emitter-follower stage) = $6.8 \times 0.22 \approx 1.5$ [W] ....(5)

Now, determine ΔTj by substituting the value for $\theta j\text{-}c$ in equation (5).

$\Delta Tj = 1.5 \times 30 = 45$ [°C]

Here, $\Delta Tj < 50$°C, and we need only consider cases where Tc < 100 °C. Therefore, we must design a θh for the heat sink such that the Tc < 100°C condition holds when three channels are operating at maximum levels, i.e., Pd(TOTAL) = Pd(one channel) × 3.

ΔTc will be $100 - 60 = 40$ °C, and therefore:

$\theta h = \Delta Tc \div Pd$ (TOTAL) = $40 \div (6.8 \times 3) = 2.0$, i.e. $\theta h = 2.0$ °C/W

In actual practice, the ambient temperature and operating conditions will allow a heat sink smaller than that indicated by this calculation to be used. Therefore, design optimization taking the actual conditions and the above data into account is also required.

Pd – f(clock) [1CH]

Pc(Tri) Ratio – f(clock)
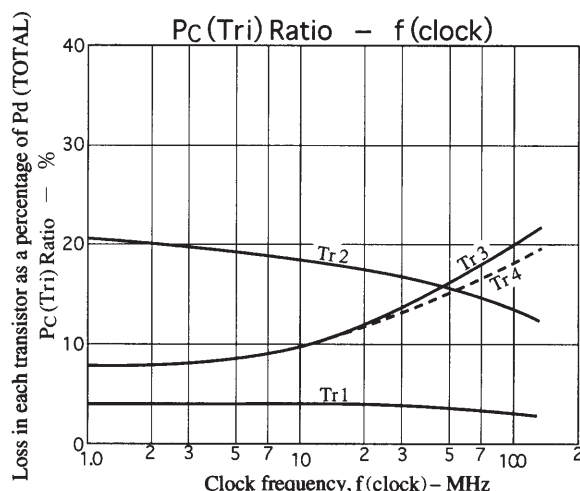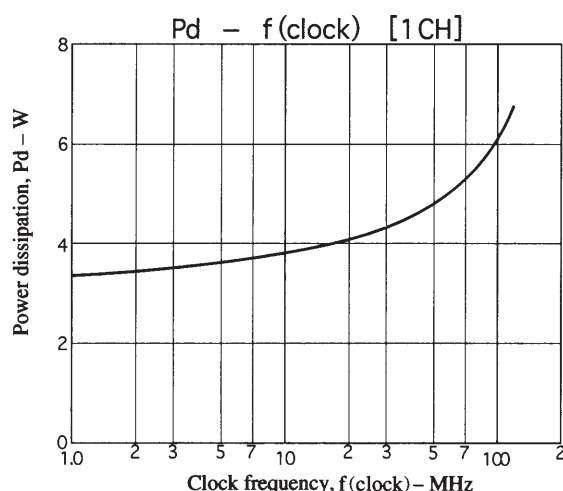
V_CC (V)	V_BB (V)	V_OUT (V)	V_O (center)
80	10	40	45