DATA SHEET

Memory Module Part Number

VS133-R512

1. Description

168pin Registered DIMM PC133/CL=3

2. Module Specification

Item	Specification
Capacity	512MByte
Physical Bank(s)	2
Module Organization	64M x 72bit
Module Type	ECC Registered
Speed Grade	PC133/CL=3 PC100/CL=2
Interface	LVTTL
Power Supply Voltage	3.3V±0.3V
Burst Lengths	1,2,4,8,Full
DRAM Organization	32M x 8bit SDR SDRAM
PCB Part No.	ZEY8RWF-A
Contact Tab	168pin GOLD Flash Plating Ni : min 2.00µm / Au : min 0.05µm
Serial PD	Support

3. Mechanical Design and Module Pinout

Item	Reference standard
Mechanical Design and Pinout	Mechanical Design and Pinout SDR 168Pin DIMM (PDRB-28998-X059-01) Y(PCB Height) : 43.18 mm Z1 : Undefined Z2 : 4.52 mm MAX(Double Sided)

4. Block Diagram

Item	Reference standard
Block Diagram	Block Diagram PC133/PC100 Registered DIMM(x8bitDRAM 2Bank) (PDRB-28998-X090-01)

5. Electrical Specifications

5.1 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage Any Pin Relative to Vss	V_T	-0.3~Vcc+0.3 (max 4.6)	V
Supply Voltage Relative to Vss	V_{CC}	-0.3~4.6	V
Power Dissipation	P_D	22	W
Short Circuit Output Current	I_O	50	mA

5.2 Recommended Operating Conditions

Parameter	Symbol	MIN	MAX	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
High Level Input Voltage	V_{IH}	2.0	Vcc+0.3	V
Low Level Input Voltage	V_{IL}	-0.3	0.8	V
Operating Ambient Temperature	T_A	0	70	°C

5.3 Pin Capacitance

Parameter		Symbol	Maximum Pin Capacitance	Unit
CK Input Pin Capacitance	CK0	C_{ICK1}	18	pF
	CK1	C_{ICK2}	12	pF
	CK2	C_{ICK3}	12	pF
	CK3	C_{ICK4}	12	pF
/S Input Pin Capacitance	S0	C_{IS1}	9.0	pF
	S1	C_{IS2}	9.0	pF
	S2	C_{IS3}	9.0	pF
	S3	C_{IS4}	9.0	pF
CKE Input Pin Capacitance	CKE0	C_{ICKE1}	18	pF
	CKE1	C_{ICKE2}	——	pF
DQM Input Pin Capacitance	DQMB0~7	C_{IDQM1}	9.0	pF
DQ Input / Output Pin Capacitance	DQ0~DQ63	C_{OUT1}	13	pF
	CB0~7	C_{OUT2}	13	pF
Other Input Pin Capacitance	A,BA,/RAS,/CAS,/WE	C_{IN}	18	pF

5.4 D.C. Characters

Parameter	Symbol	Value		Unit	Test Condition
Operating current	I_{CC1}	MAX	2749 *	mA	Burst length=1, $t_{RC} \geq t_{RC}$ (min), I_O=0mA, One bank active
Precharge Standby current in power down mode	I_{CC2P}	MAX	805 *	mA	CKE ≤ V_{IL}(max), t_{CK} = 12ns
	I_{CC2PS}	MAX	805 *	mA	CKE ≤ V_{IL}(max), t_{CK} = ∞
Precharge Standby current in non power down mode	I_{CC2N}	MAX	1399 *	mA	CKE, /S ≥ V_{IH}(min), t_{CK} = 12ns
	I_{CC2NS}	MAX	1039 *	mA	CKE ≥ V_{IH} (min), t_{CK} = ∞
Active standby current in power down mode	I_{CC3P}	MAX	949 *	mA	CKE ≤ V_{IL}(max), t_{CK} = 12ns
	I_{CC3PS}	MAX	877 *	mA	CKE ≤ V_{IL}(max), t_{CK} = ∞
Active standby current in non power down mode	I_{CC3N}	MAX	1849 *	mA	CKE, /S ≥ V_{IH}(min), t_{CK} = 12ns
	I_{CC3NS}	MAX	1309 *	mA	CKE ≥ V_{IH} (min), t_{CK} = ∞
Operating current (Burst mode)	I_{CC4}	MAX	2749 *	mA	$t_{CK} \geq t_{CK}$ (min) Io=0mA, One bank active
Auto refresh current	I_{CC5}	MAX	6529 *	mA	$t_{RC} \geq t_{RC}$ (min)
Self refresh current	I_{CC6}	MAX	823 *	mA	CKE ≤ 0.2V
Input leakage current	I_{IL}	MIN	-10 *	µA	All other pins are not under test=0V 0V ≤ V_{IN} ≤ V_{CC}
		MAX	10 *	µA	
Output High Voltage	V_{OH}	MIN	2.4 *	V	I_{OH} = -2mA
Output Low Voltage	V_{OL}	MAX	0.4 *	V	I_{OL} = 2mA

* : No guarantee against this value.

5.5 A.C. Timing Characters

Parameter	Symbol	MIN	MAX	Unit
Clock Period /CAS Latency = 2 /CAS Latency = 3	t_{CLK}	 10 7.5	 1000 1000	ns
Clock High Pulse Width	t_{CH}	2.5	——	ns
Clock Low Pulse Width	t_{CL}	2.5	——	ns
Input Setup Time	t_{SI}	1.5	——	ns
Input Hold Time	t_{HI}	0.8	——	ns
Output Valid From Clock /CAS Latency = 2 /CAS Latency = 3	t_{AC}	 —— ——	 6 5.4	ns
Output Hold From Clock	t_{OH}	2.7	——	ns
/RAS to /CAS Delay	t_{RCD}	20	——	ns
/RAS Active Time	t_{RAS}	45	100,000	ns
/RAS Precharge Time	t_{RP}	20	——	ns
Act to Act Command Period	t_{RRD}	15	——	ns
Row Cycle Time	t_{RC}	67.5	——	ns
Average Periodic Refresh Interval	t_{REF}	——	7.8	µs
Mode Register cycle time	t_{MRC}	15	——	ns

6. Serial Presence Detect (SPD) Data Structure

Byte No.	Function	Hex Value	Function Supported
0	Defines # of bytes written into serial memory at module manufacturer	80	128Bytes
1	Total # of bytes of SPD memory device	08	256Bytes
2	Fundamental memory type (FPM, EDO, SDRAM..)	04	SDR SDRAM
3	# of row addresses on this assembly	0D	13
4	# Column Addresses on this assembly	0A	10
5	# Module Banks on this assembly	02	2Banks
6	Data Width of this assembly	48	72bits
7	... Data Width continuation	00	
8	Voltage interface standard of this assembly	01	LVTTL
9	SDRAM Cycle time (highest CAS latency)	75	7.5ns (CL=3)
10	SDRAM Access from Clock (highest CAS latency)	54	5.4ns (CL =3)
11	DIMM Configuration type (non-parity, ECC)	02	ECC
12	Refresh Rate/Type	82	7.8µs
13	Primary SDRAM Width	08	x8bit
14	Error Checking SDRAM width	08	x8bit
15	Minimum Clock Delay Back to Back Random Column Address	01	1CLK
16	Burst Lengths Supported	8F	Burst Lengths (1,2,4,8,FULL)
17	# of Banks on Each SDRAM Device	04	4Banks
18	CAS# Latency	06	CAS Latency =2,3
19	CS# Latency	01	CS Latency =0
20	Write Latency	01	WE Latency =0
21	SDRAM Module Attributes	1F	Registered with PLL
22	SDRAM Device Attributes: General	0E	Supports Write1/Read Burst Supports Precharge All Supports Auto-Precharge
23	SDRAM Cycle time (2nd highest CAS latency)	A0	10ns (CL=2)
24	SDRAM Access from Clock (2nd highest CAS latency)	60	6ns (CL=2)
25	SDRAM Cycle time (3rd highest CAS latency)	00	Non Support
26	SDRAM Access from Clock (3rd highest CAS latency)	00	Non Support
27	Minimum Row Precharge Time	14	20ns
28	Row Activate to Row Activate Min.	0F	15ns
29	RAS to CAS Delay Min	14	20ns
30	Minimum RAS Pulse Width	2D	45ns
31	Density of each bank on module	40	256MB
32	Command and Address signal input setup time	15	1.5ns
33	Command and Address signal input hold time	08	0.8ns
34	Data signal input setup time	15	1.5ns
35	Data signal input hold time	08	0.8ns
36-61	Superset Information (may be used in future)	00	Undefined
62	SPD Data Revision Code	12	Rev 1.2
63	Checksum for bytes 0-62	04	Checksum
64-66	Manufacturer's JEDEC ID code per JEP-108E	7F	MELCO inc.
67		83	
68-71		00	
72	Manufacturing Location	01	
73-90	Manufacturer's Part Number	20	Blank
91-92	Revision Code	00	Undefined
93-94	Manufacturing Date	00	Undefined
95-98	Assembly Serial Number	00	Undefined
99-125	Manufacturer Specific Data	00	Undefined
126	Intel specification frequency	64	100MHz Compatible
127	Intel Specification CAS# Latency support	87	Clock=0 CL =2,3
128+	Unused storage locations	00	Undefined

7. Packing/Label Specification

Item	Reference standard
Packing/Label Specification	Packing/Label Specification –for 5.25inchWidth DIMM (PDRB-28998-X062-01)

8. Revision History

Rev.	Date	Changes	Issued
01	Jan.24.2003	———	J.Onisi