VITESSE
SEMICONDUCTOR CORPORATION

Advance Product Information

VSC7146

2.5Gb/s, 20-Bit Transceiver

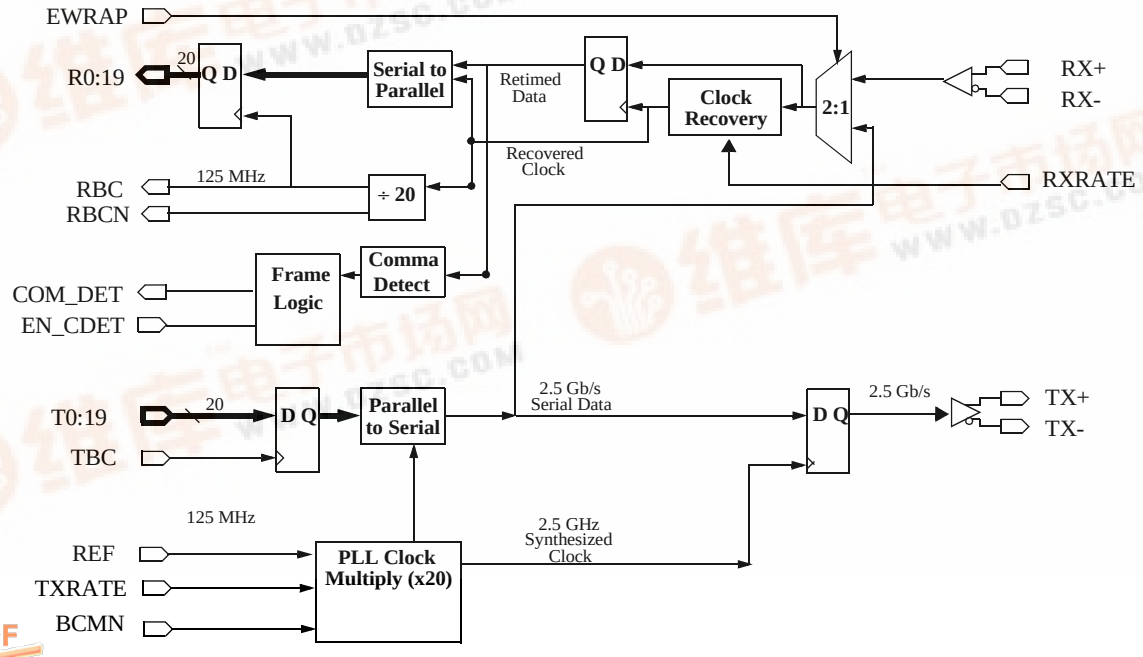
Features

- Speed Selectable Full-Duplex Transceiver:
  - 1.06/2.12Gb/s for FibreChannel
  - 1.25/2.5Gb/s for Gigabit Ethernet
- 20-Bit TTL Interface for Transmit and Receive Data at 125MHz
- Monolithic Clock Synthesis and Clock Recovery - No External Components
- 125MHz TTL Reference Clock
- Automatic Lock-to-Reference Function
- Suitable for Both Coaxial and Optical Link Applications
- Low Power Operation: 2.5 W max
- 80-Pin, 14mm Thermally-Enhanced EDQUAD Package
- Single +3.3V Supply

General Description

The VSC7146 is a 2.5Gb/s Transceiver optimized for ease-of-use and efficiency in high-performance data transmission systems. The VSC7146 accepts two 10-bit 8b/10b encoded transmit characters, latches them on the rising edge of Transmit Byte Clock (TBC) and serializes the data onto the TX+/- differential outputs at a baud rate, which is 20 times the TBC frequency. The VSC7146 also samples serial receive data on the RX+/- differential inputs, recovers the clock and data, deserializes it onto two 10-bit receive characters, outputs a recovered clocks at one-twentieth of the incoming baud rate and detects Fibre Channel “comma” characters. The VSC7146 contains on-chip Phase-Lock Loop (PLL) circuitry for synthesis of the baud-rate transmit clock, and extraction of the clock from the received serial stream. These circuits are fully monolithic and require no external components.

Block Diagram



Functional Description

Clock Synthesizer

The VSC7146 clock synthesizer multiplies the 125MHz reference frequency provided on the REF input by 20 to achieve a baud rate clock at 2.5GHz. The clock synthesizer contains a fully monolithic PLL which requires no external components. An additional 125MHz clock, TBC, should be provided to clock in the data bus. Since TBC is only used for the purpose of clocking data in, it is not required to have the same jitter constraints as REF. REF clock and TBC should preserve certain phase margins and be of the same frequency.

Serializer

The VSC7146 accepts TTL input data as two parallel 10-bit characters on the T[0:19] bus which is latched into the input latch on the rising edge of a 125MHz clock at TBC. This data will be serialized and transmitted on the TX differential outputs at a baud rate of 20 times the frequency of the TBC input, with bit T0 transmitted first. User data should be encoded for transmission using the 8B/10B block code described in the Fibre Channel specification, or an equivalent, edge rich, DC-balanced code. If EWRAP is HIGH, the transmitter will be disabled with TX+ HIGH and TX- LOW. If EWRAP is LOW, the transmitter outputs serialized data. The phases of REF clock and TBC can be identical, but there is a phase relationship between the two input clocks which must be maintained.

Transmission Character Interface

In Fibre Channel, an encoded byte is 10 bits and is referred to as a transmission character. The 20-bit interface on the VSC7146 corresponds to two transmission characters. This mapping is shown in Figure 1.

Figure 1: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10B Bit Position	j	h	g	f	i	e	d	c	b	a	j	h	g	f	i	e	d	c	b	a
Valid “Comma” Position														1	1	1	1	1	0	0

Last Data Bit Transmitted

First Data Bit Transmitted

Clock Recovery

The VSC7146 accepts differential high-speed serial inputs on the RX+/RX- pins, (when EWRAP is LOW), extracts the clock and retimes the data. The serial bit stream should be encoded so as to provide DC balance and limited run length by a Fibre Channel-compatible 8B/10B transmitter or equivalent. The VSC7146 clock recovery circuitry is completely monolithic and requires no external components. For proper operation, the baud rate of the data stream to be recovered should be within 200ppm of twenty times the REF frequency. This allows oscillators on either end of the link to be 125MHz +/- 100ppm.

Deserializer

The retimed serial bit stream is converted into two 10-bit parallel output characters. The VSC7146 provides a TTL recovered clock, RBC, at one twentieth of the serial baud rate. The clock is generated by dividing down the high-speed clock which is phase-locked to the serial data. The serial data is retimed by the internal high-speed clock, and deserialized. The resulting parallel data will be captured by the adjoining protocol logic on the rising edge of RBC.

If serial input data is not present, or does not meet the required baud rate, the VSC7146 will continue to produce a recovered clock and RBC will automatically lock to the REF reference clock. This eliminates the need for a Lock-to-Reference input pin and simplifies the support software for that function.

Word Alignment

The VSC7146 provides 7-bit Fibre Channel “comma” character recognition and data word alignment. Word synchronization is enabled by asserting EN_CDET HIGH. When synchronization is enabled, the VSC7146 constantly examines the serial data for the presence of the Fibre Channel “comma” character. This pattern is “0011111XXX”, where the leading zero corresponds to the first bit received. The “comma” sequence is not contained in any normal 8B/10B coded data character or pair of adjacent characters. It occurs only within special characters, known as K28.1, K28.5 and K28.7, which are defined specifically for synchronization in Fibre Channel systems. Improper alignment of the “comma” character is defined as either of the following conditions:

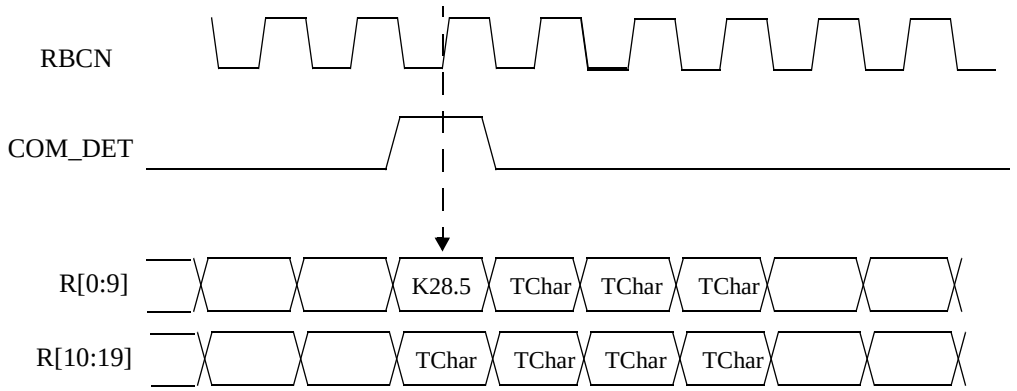
1) The “comma” is not aligned within the 10-bit transmission character such that T0...T6 = “0011111.”

2) The “comma” straddles the boundary between two 10-bit transmission characters.

When EN_CDET is HIGH and an improperly aligned “comma” is encountered, the internal data is shifted in such a manner that the “comma” character is aligned properly in R[0:6] as shown in Figure 1. This results in proper character and word alignment. When the parallel data alignment changes in response to a improperly aligned “comma” pattern, some data which would have been presented on the parallel output port may be lost. However, the synchronization character and subsequent data will be output correctly and properly aligned. When EN_CDET is LOW, the current alignment of the serial data is maintained indefinitely, regardless of data pattern.

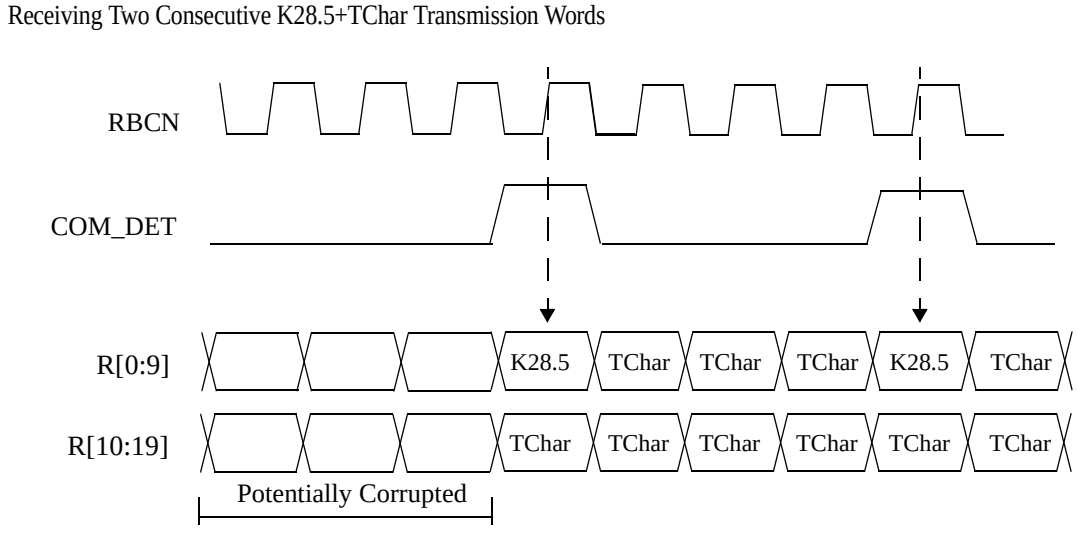
On encountering a “comma” character, COM_DET is driven HIGH to inform the user that realignment of the parallel data field may have occurred. The COM_DET pulse is presented simultaneously with the “comma” character and has a duration equal to the data. The COM_DET signal is timed such that it can be captured by the adjoining protocol logic on the rising edge of RBC. Functional waveforms for synchronization are shown in Figure 2 and Figure 3. Figure 2 shows the case when a “comma” character is detected and no phase adjustment is necessary. It illustrates the position of the COM_DET pulse in relation to the “comma” character on R[0:6]. Figure 3 shows the case where the K28.5 is detected, but it is out-of-phase and a change in the output data alignment is required. Note that up to three characters prior to the “comma” character may be corrupted by the realignment process.

Figure 2: Detection of a Properly Aligned "Comma" Character



TChar: 10 bit Transmission Character

Figure 3: Detection and Resynchronization of an Improperly Aligned "Comma" Character



Dual Data Rate Operation

The VSC7146 performs at two data rates, full-speed (2.5 Gb/s on the serial link, 125MHz on the parallel 20-bit data bus) and half-speed (1.25 Gb/s on the serial link, 62.5 Mb/s on the parallel 20-bit data bus). To accommodate for this, the user is provided with 3 signal pins for data rate control: TXRATE, RXRATE and BCMN. The usage of these signals is as follows:

If BCMN = 0 (Backwards Compatibility Mode), TXRATE controls both the serializer and deserializer speeds. TXRATE should be HIGH for full-speed operation and LOW for half-speed operation.

If BCMN = 1, TXRATE controls the serializer speed and RXRATE controls the deserializer speed. TXRATE and/or RXRATE must be HIGH for full-speed operation and/or LOW for half-speed operation.

Table 1: Data Rate

BCMN	*TXRate*	*RXRate*	*Description*
0	1	X	Both serializer and deserializer run at full-speed.
0	0	X	Both serializer and deserializer run at half-speed.
1	0	0	Both serializer and deserializer run at half-speed.
1	0	1	Serializer is run at half-speed and deserializer is run at full-speed.
1	1	0	Serializer is run at full-speed and deserializer is run at half-speed.
1	1	1	Both serializer and deserializer run at full-speed.

For “comma” character (K28.5) detection, it is recommended not to use differing RXRATE inputs to actual RX rate data reception, as shown in the Table 2 (assumes EN_CDET = 1):

Table 2: Comma Detect

RXRate	*RX+/- Actual Data Rate*	*“Comma” Detect*
0 Half-Speed	2.5Gb/s	Will only detect 00/00/11/11/11/11/11 pattern as “comma”. **Do not use**.
0 Half-Speed	1.25Gb/s	Normal detection operation.
1 Full-Speed	2.5Gb/s	Normal detection operation.
1 Full-Speed	1.25Gb/s	Will detect false characters (e.g., those that include “0111”) as “comma”. **Do not use**.

Similarly, it is recommended not to use differing TXRATE inputs to actual TX rate data reception. The T[19:0] data bus, TBC and REF clock inputs must be at 125Mb/s rates if TXRATE = 1 and 62.5Mb/s if TXRATE = 0. It is important to note that the PLL will not lock otherwise.

Along with the 20-bit data input to the serializer, the user will also have to send the appropriate transmit byte clock signal (TBC)—that is, 125MHz when TXRATE = 1 and 62.5MHz when TXRATE = 0. REF and TBC should be frequency-locked in all cases and should maintain a certain phase relationship as shown in Figure 6. The output recovered clocks (RBC/RBCN), the output deserialized data (R[19:0]) and the internal VCO high-speed clock multiplier will be automatically adjusted by the TXRATE and RXRATE signals.

The baud rate of the data stream to be recovered in the deserializer should be within 200ppm of the REF frequency. In other words: $\left|F_{REF-TX} - F_{REF-RX}\right| \leq 200ppm$

Figure 4: Transmit Timing Waveforms

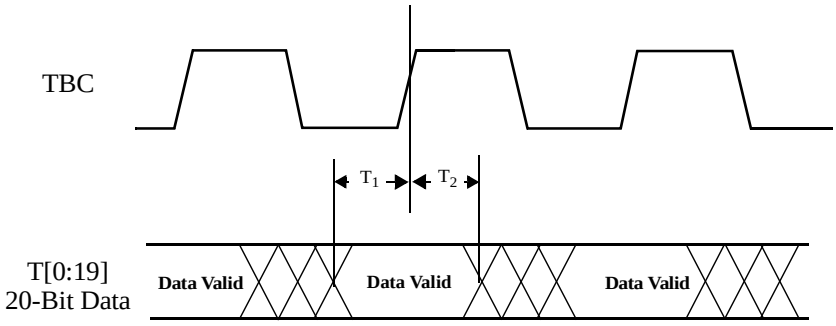


Table 3: Transmit AC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_1	T[0:19] setup time to the rising edge of TBC	1.5		—	ns	Measured between the valid data level of T[0:19] to the 1.4V point of TBC.
T_2	T[0:19] hold time after the rising edge of TBC	1.0		—	ns	
T_{SDR},T_{SDF}	TX+/TX- rise and fall time	—		160	ps	20% to 80% into 50Ω load to V_{SS}. Tested on a sample basis.
T_{LAT}	Latency from rising edge of TBC to T0 appearing on TX+ TX-	24 bc +1ns		45 bc +1ns	Bit Clock	Bit clock periods (PLL locked)
Transmitter Output Jitter Allocation						
T_{RJ}	Serial data output random jitter (RMS)	—	5	7.5	ps	RMS, tested on a sample basis.
T_{DJ}	Serial data output deterministic jitter (p-p)	—	25	30	ps	Peak-to-peak, tested on a sample basis.

Figure 5: Receive Timing Waveforms

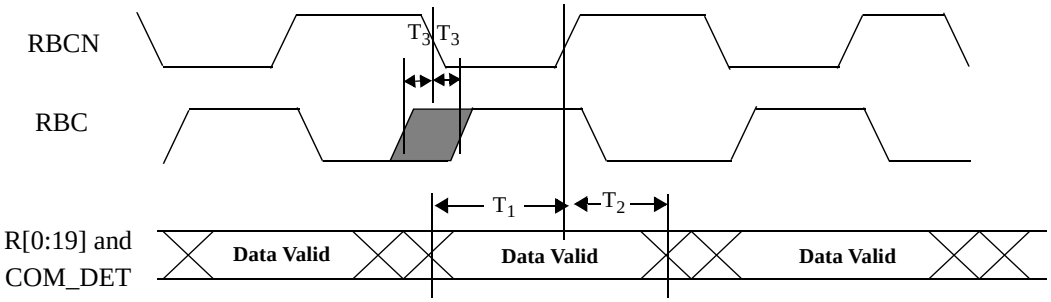
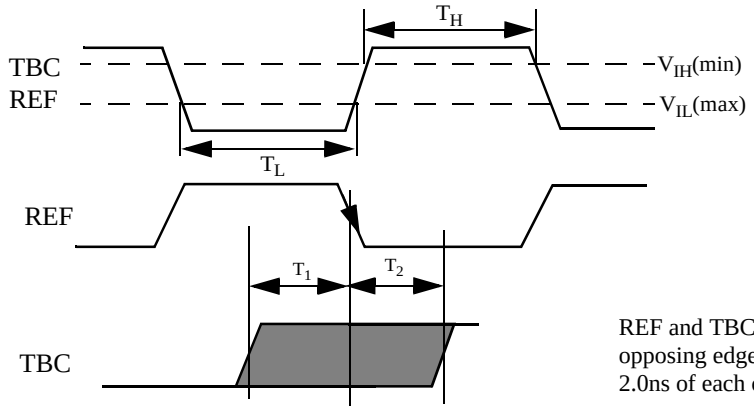


Table 4: Receive AC Characteristics

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_1	Data or COM_DET valid prior to RBCN rise	1.0 2.0	—	ns	Measured between the 1.4V point of RBCN and a valid level of R[0:19] or COM_DET. All outputs driving 10pF load. The spec on top relects RXMODE=1 and the bottom one reflects RXMODE=0.
T_2	Data or COM_DET valid after RBCN rise	5.0 10.0	—	ns	
T_3	Time difference between RBC and RBCN edges	—	1	ns	
T_{R1}, T_{F1}	RBC/RBCN rise and fall time	0.6	2.0	ns	Between V_{IL}(max) and V_{IH}(min), into 10pF load.
T_{R2}, T_{F2}	R[0:19], COM_DET rise and fall time	0.7	2.4	ns	Between V_{IL}(max) and V_{IH}(min), into 10pF load.
R_{LAT}	Latency from RX to R[0:19]	36bc+ 2ns	56bc+ 2ns	Bit Clocks	When locked to valid data.
T_{RBC}	RBC period	7.9 15.8	8.1 16.2	ns	The spec on top relects RXMODE=1 and the bottom one reflects RXMODE=0.
DC	RBC duty cycle	40%	60%	period	
T_{LOCK}	Data acquisition lock time @ 2.5Gb/s	—	1250	Bit Clocks	Tested on a sample basis. 95% probability of lock.

Figure 6: TBC and REF Timing Waveforms



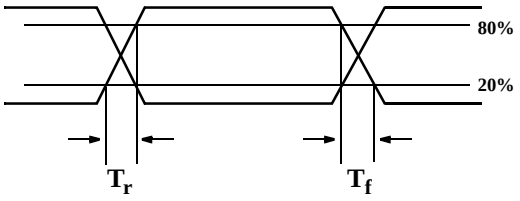
REF and TBC must not have their opposing edges coincident within 2.0ns of each other.

Table 5: TBC and REF Requirements

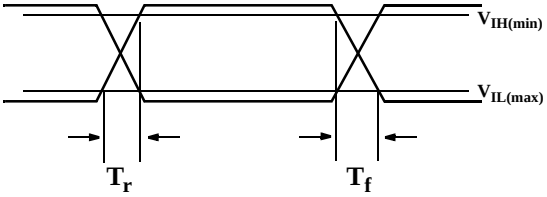
Parameters	***Description***	Min	Max	Units	***Conditions***
T_1	Necessary lag time between TBC and REF	—	2.0	ns	Measured from falling edge of REF to rising edge of TBC.
T_2	Necessary lead time between TBC and REF	—	2.0	ns	Measured from falling edge of REF to rising edge of TBC.
FR	Frequency Range	105 52.5	127 63.5	MHz	Range over which both transmit and receive reference clocks on any link may be centered. The figure on top relects TXMODE=1 and the bottom one reflects TXMODE=0.
FO	Frequency Offset	–100	+100	ppm	$\lvert TX_{TBC} - RX_{TBC} \rvert$
T_L,T_H	Pulse Width, Low / High	4.5	2.5	ns	Low is measured from V_{IL}(max) to V_{IL}(max), High is measured from V_{IH}(min) to V_{IH}(min). Min measurement refers to TXMODE=0 and Max measurement refers to TXMODE=1.
DC	TBC and REF duty cycle	40	60	%	Measured at 1.5V.
T_{RCR},T_{RCF}	TBC and REF rise and fall time	0.6	1.5	ns	Between V_{IL}(max) and V_{IH}(min).

Figure 7: Parametric Measurement Information

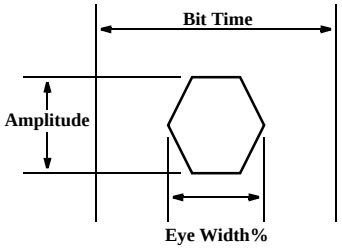
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

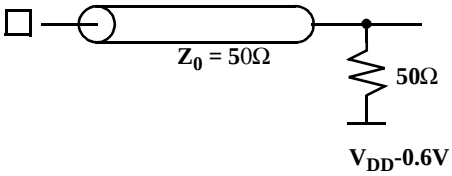


Receiver Input Eye Diagram Jitter Tolerance Mask

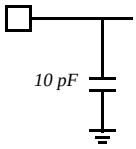


Parametric Test Load Circuit

Serial Output Load



TTL AC Output Load



Absolute Maximum Ratings (1)

Power Supply Voltage, (V_{DD}) ..... –0.5V to +4V
DC Input Voltage (Differential inputs) ..... –0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... –0.5V to V_{DD}+0.5V
DC Output Voltage (TTL Outputs) ..... –0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... ±50mA
Output Current (Differential Outputs) ..... ±50mA
Case Temperature Under Bias ..... –55°C to +125°C
Storage Temperature ..... –65°C to +150°C
Relative Humidity (Storage) ..... 0% - 95% (Non-condensing)
Relative Humidity (Operating) ..... 8% - 80%
Maximum Input ESD (Human Body Model) ..... 1500V(2)

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied.Exposure to these values for extended periods may affect device reliability.

(2) High-speed PECL receiver inputs only are rated at 700V.

Recommended Operating Conditions

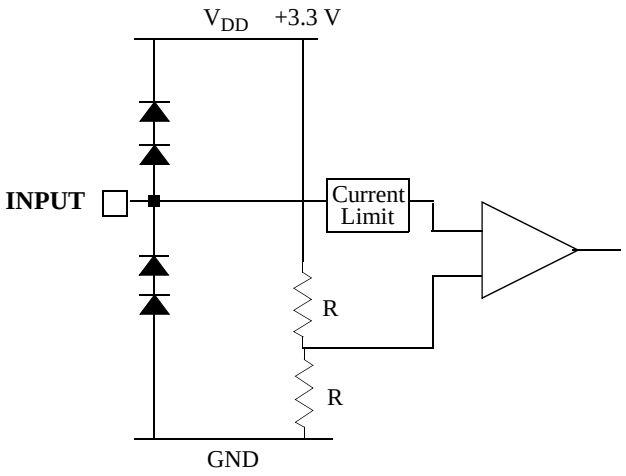
Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Power Supply Noise, (V_{DD}) ..... 100mVp-p from 100Hz to TBD MHz
Operating Temperature Range ..... 0°C Ambient to +90°C Case Temperature

DC Characteristics *(Over recommended operating conditions)*

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = –1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
ΔV_{OUT50}(1)	Serial output absolute voltage differential peak-to-peak swing (TX+/TX-)	600	1100	2000	mV	Driving a 50Ω transmission line (TX+ - TX-)
ΔV_{OUT75}(1)	Serial output absolute voltage differential peak-to-peak swing (TX+/TX-)	600	1100	2000	mV	Driving a 75Ω transmission line (TX+ - TX-)
ΔV_{IN} (1)	Serial input absolute voltage differential peak-to-peak swing (RX+/RX-)	400	—	2200	mV	(RX+ - RX-)
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	
I_{IH}	Input HIGH current (TTL)	—		1000	µA	V_{IN} = 2.4 V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5 V
V_{DD}	Supply voltage	3.14	—	3.47	V	+3.3V± 5%
P_D	Power dissipation	—	1.8	2.6	W	Outputs open, V_{DD} = V_{DD} max
I_{DD}	Supply current	—	550	750	mA	Outputs open, V_{DD} = V_{DD} max
Z_O	Output resistance (TX)	—	50	—	Ω	
Z_I	Input resistance (RX)	—	50	—	Ω	

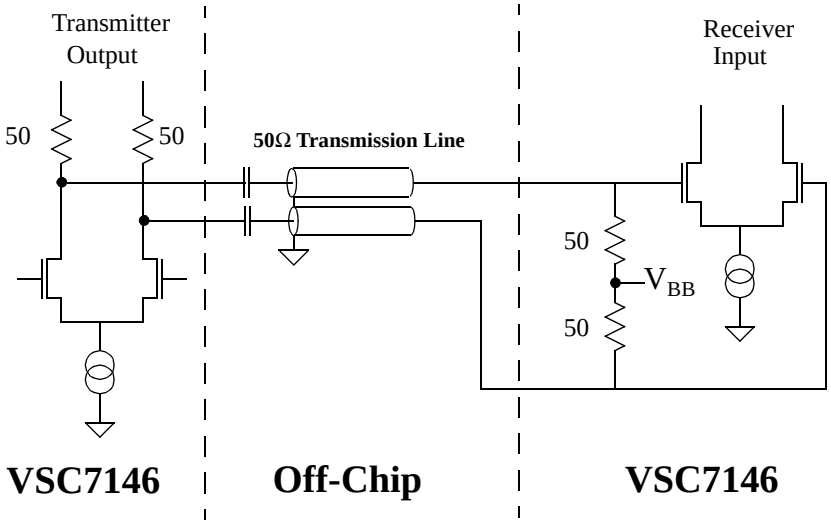
Note: (1) Refer to Application Note, AN-37, for differential measurement techniques.

Figure 8: Input Structures



TTL Inputs

Figure 9: High-Speed I/O Termination Scheme

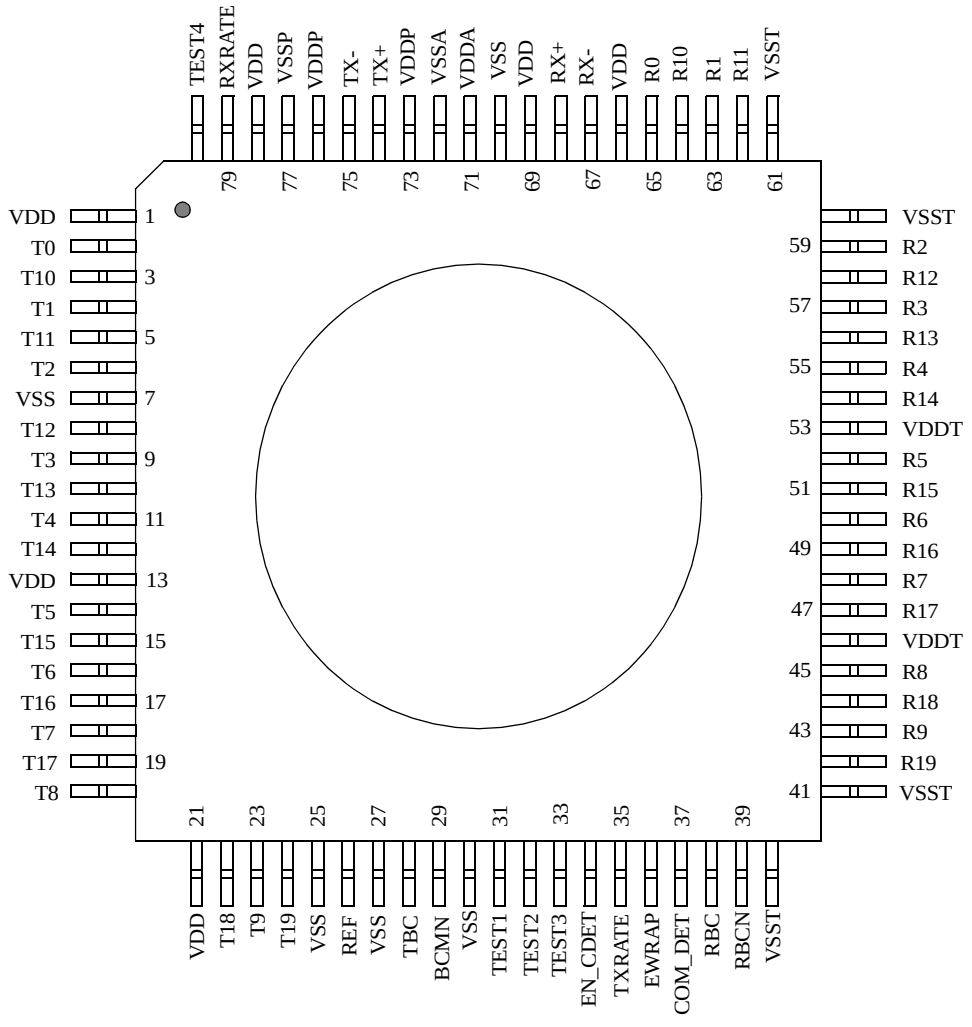


No external resistor terminations are necessary on the high-speed I/O

Package Pin Descriptions

Figure 10: Pin Diagram

(Top View)



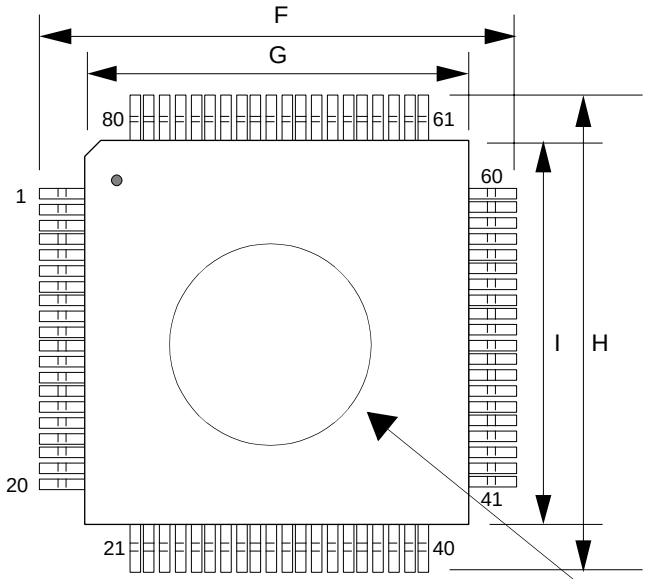
NOTES: Heat Sink is not connected electrically. It should not be connected electrically by the user.
Pin 80 has changed from **SLOOP** in previous versions of the spec to **TEST4**. Tie this pin to V_{SS}.

Table 6: Pin Identifications

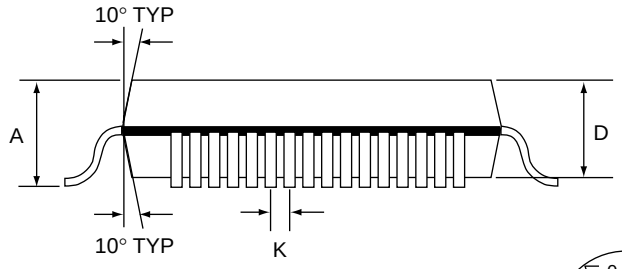
Pin #	*Name*	*Description*
2, 4, 6, 9, 11, 14, 16, 18, 20, 23, 3, 5, 8, 10, 12, 15, 17, 19, 22, 24	T[0:19]	INPUTS - TTL: Transmit Data Bus, Bit 0 through Bit 19. 20-bit Transmit Character. Parallel data on this bus is clocked in on the rising edge of TBC. The data bit corresponding to T0 is transmitted first.
26	REF	INPUT - TTL: Reference Clock. REF goes to the PLL/CMU circuitry and is multiplied 20 times
28	TBC	INPUT - TTL: Transmit Byte Clock. This rising edge of this clock latches T[0:19] into the input register and provides the reference clock at 1/20th of the baud rate to the PLL.
74,75	TX+, TX-	OUTPUTS - Differential (AC-coupling recommended): Transmitter Serial Outputs. These pins output the serialized transmit data when EWRAP is LOW. When EWRAP is HIGH, TX+ is HIGH and TX- is LOW.
65, 63, 59, 57, 55, 52, 50, 48, 45, 43, 64, 62, 58, 56, 54, 51, 49, 47, 44, 42	R[0:19]	OUTPUTS - TTL: Receive Data Bus, Bits 0 thru 19. 20-bit received character. Parallel data on this bus can be sampled on the rising edge of RBC. R0 is the first bit received on RX+/RX-.
35	TXRATE	INPUT - TTL: Transmitter Dual Rate Selector. LOW for half-speed operation (1.25Gb/s). HIGH for full-speed operation (2.5 Gbps).
79	RXRATE	INPUT - TTL: Receiver Dual Rate Selector. LOW for half-speed operation (1.25Gb/s). HIGH for full-speed operation (2.5Gb/s).
29	BCMN	INPUT - TTL: Backwards Compatibility Mode Selector. LOW to allow operation in previous version compatibility (no separate rate controls for transmitter and receiver). HIGH to allow operation with separate rate controls for transmitter and receiver.
36	EWRAP	INPUT - TTL: Enable Internal WRAP Mode. LOW for Normal Operation. When HIGH, an internal loopback path from the transmitter to the receiver is enabled, TX+ = HIGH and TX- is LOW.
68, 67	RX+, RX-	INPUTS - Differential (AC-coupling recommended): Receive Serial Inputs. The receiver inputs when EWRAP is LOW.
38, 39	RBC, RBCN	OUTPUT - TTL: Recovered Byte Clock. Recovered clock and complement derived from 1/20th of the RX+/- data rate. The rising edge of RBC corresponds to a new word on R[0:19].
34	EN_CDET	INPUT - TTL: ENable Comma DETect. Enables COM_DET and word resynchronization when HIGH. When LOW, keeps current word alignment and disables COM_DET.
37	COM_DET	OUTPUT - TTL: COMma DETect. This output goes HIGH to indicate that R[0:6] contains a “comma” character (‘0011111’). COM_DET can be sampled on the rising edge of RBC.

Pin #	*Name*	*Description*
31, 32, 33	TEST1, TEST2, TEST3	TEST Pins For internal Vitesse use only. Customers should tie TEST1, TEST2 and TEST3 to V_{DD}.
80	TEST4	TEST Pins For internal Vitesse use only. Customers should tie TEST4 to V_{SS}.
1, 13,21, 66, 69,78	VDD	Digital Power Supply, +3.3V.
46, 53	VDDT	TTL Power Supply, +3.3V.
71	VDDA	Analog Power Supply, +3.3V.
73, 76	VDDP	High-Speed Output Driver Power Supply, +3.3V
7, 25, 27, 30, 70	VSS	Digital Ground, 0V.
40, 41, 60, 61	VSST	TTL Ground, 0V.
72	VSSA	Analog Ground, 0V.
77	VSSP	High-Speed Output Driver Ground, 0V.

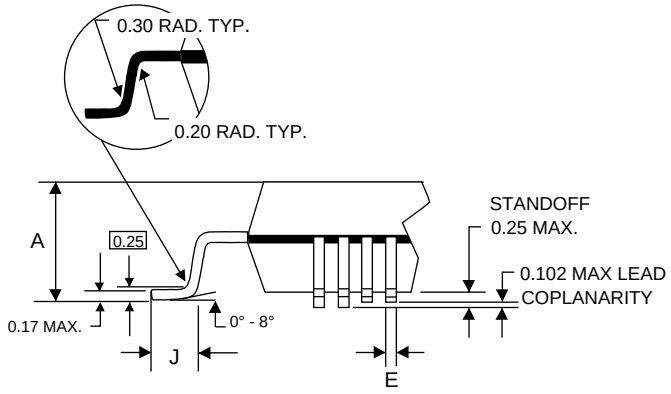
Package Information



Item	*14 mm*	*Tolerance*
A	2.35	MAX
D	2.00	+0.10/-0.05
E	0.30	±.05
F	17.20	±.25
G	14.00	±.10
H	17.20	±.25
I	14.00	±.10
J	0.88	+.15/-.10
K	0.65	BASIC



EXPOSED HEATSINK
6.85 ± .50 DIA
HEATSINK INTRUSION
.0127 MAX



NOTES:

Drawing not to scale.
All units in mm unless otherwise noted.

Package Thermal Characteristics

The VSC7146 is packaged in an 80-pin, 14mm thermally-enhanced EDQUAD with an internal heat spreader. These packages use industry-standard EIAJ footprints, which have been enhanced to improve thermal dissipation. The construction of the packages are as shown in Figure 11. The VSC7146 is designed to operate with a case temperature up to 90°C. The user must guarantee that the temperature specification is not violated.

Figure 11: Package Cross Section

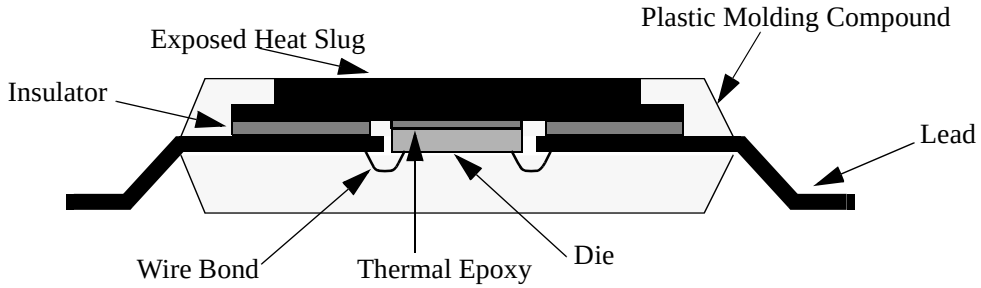
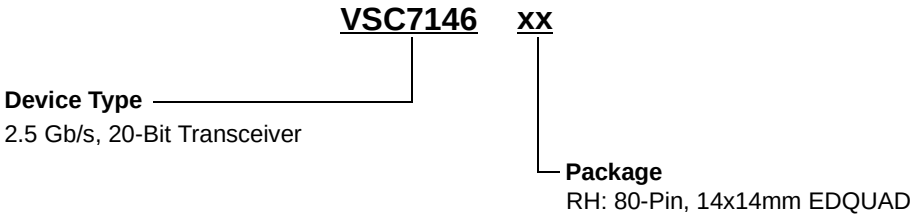


Table 7: Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction-to-case	2.5	°C/W
θ_{ca-0}	Thermal resistance from case-to-ambient, still air	35	°C/W
θ_{ca-100}	Thermal resistance from case-to-ambient, 100 LFPM air	29	°C/W
θ_{ca-200}	Thermal resistance from case-to-ambient, 200 LFPM air	26	°C/W
θ_{ca-400}	Thermal resistance from case-to-ambient, 400 LFPM air	22	°C/W
θ_{ca-600}	Thermal resistance from case-to-ambient, 600 LFPM air	19	°C/W

Ordering Information

The part number for this product is formed by a combination of the device number and the package style:



Notice

This document contains information about a new product during its fabrication or early sampling phase of development. The information contained in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this data sheet is current prior to design or order placement.

Warning

Vitesse Semiconductor Corporation's products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without written consent is prohibited.

Revision History:

1.0 Initial Release

1.1 Fix Fig 5, Add Figure 10, New numbers for Power Supply, Dissipation, Zi/Zo/Ri/Ro & Termination.

1.2 Added T_{rj}/T_{dj}, Power Supply Noise, Pinout Diagram, Different Thermals, Added Reliability

1.3 Filled in TBA's, package pinout, pin description, dual-mode description. For internal CDR.

2.0 Post CDR. Rev.A target spec.

2.1 Pre-CDR. Rev. B target spec.

2.2 Post-CDR. Rev. B API. Removed reliability table. Changed BCLK name to TBC.

2.2.1 Removed 50 ohm termination wording in table on page 10.

2.3 Modified title and features section to reflect dual speed.

2.4 Added facility loop-back (SLOOP) and speed negotiation port (TXRATE, RXRATE, BCMN) features. Modified pinout list and diagram accordingly.

Modified spec as per ICR results.

Changed package type from QZ to RH.

2.5 Removed facility loop-back (SLOOP) feature. Changed pin# 80 from SLOOP to TEST4.

Modified Figures 2 and 3 to better reflect RBCN relationship with output data R[0:19].

Modified RBCN vs. R bus timing as per characterization findings.

2.6 Revised max Idd to 750 ma, max power to 2.6 W; Modified ESD rating on p.10; removed "Vitesse Confidential"

2.7Added typ column to Table 3: TRJ:added typ 5 ps, changed max from 5ps to 7.5ps; TDJ: added typ 25ps. Corrected grammatical/typo errors and corrected inconsistencies. Updated format. Removed marking information.