VITESSE
SEMICONDUCTOR CORPORATION

Preliminary Data Sheet

VSC7212

Gigabit Interconnect Chip

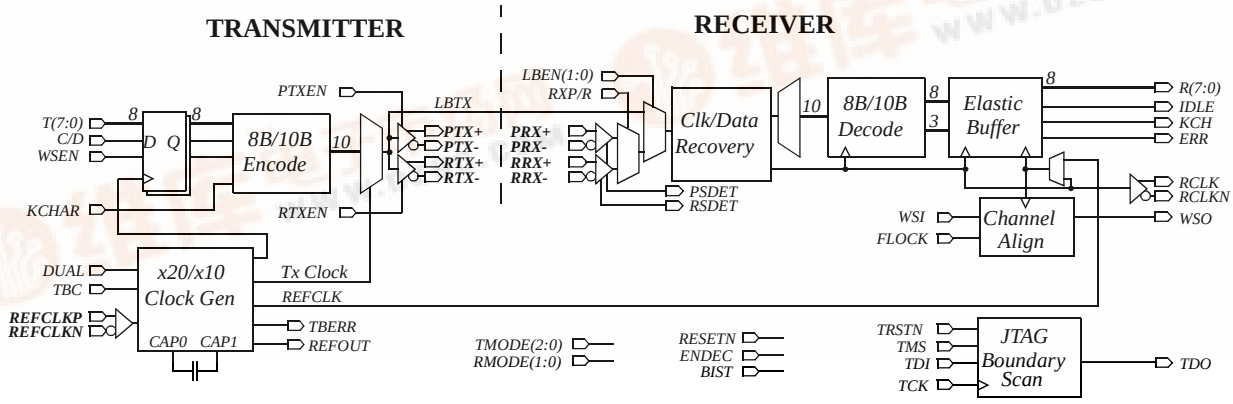
Features

- ANSI X3T11 Compliant Fibre Channel and IEEE 802.3z Compliant Gigabit Ethernet Transceiver
- Over 2Gb/s Duplex Raw Data Rate
- Redundant PECL Tx Outputs and Rx Inputs
- 8B/10B Encoder/Decoder, Optional Encoder/ Decoder Bypass Operation
- "ASIC-Friendly™" Timing Options for Transmitter Parallel Input Data
- Elastic Buffer for Chip-to-Chip Cable Deskewing
- Tx/Rx Rate Matching via IDLE Insertion/Deletion
- Compatible with VSC7211, VSC7214 and VSC7216
- Received Data Aligned to Local REFCLK or to Recovered Clock
- PECL Rx Signal Detect and Cable Equalization
- Serial Tx-to-Rx and Parallel Rx-to-Tx Internal Loopback Modes
- Clock Multiplier Generates Baud Rate Clock
- Automatic Lock-to-Reference
- JTAG Boundary Scan Support for TTL I/O
- Built-In Self Test
- 3.3V Supply, 1.0 W
- 100-pin, 14mm TQFP package

General Description

The VSC7212 is an 8-bit parallel-to-serial and serial-to-parallel transceiver chip used for high bandwidth interconnection between busses, backplanes, or other subsystems. A Fibre Channel and Gigabit Ethernet compliant transceiver provides up to 2.18Gb/s of duplex raw data transfer. The VSC7212 can operate at a maximum data transfer rate of 1088Mb/s (8 bits at 136MHz) or a minimum rate of 784Mb/s (8 bits at 98MHz). The VSC7212 contains an 8B/10B encoder, serializer, de-serializer, 8B/10B decoder and elastic buffer which provide the user with a simple interface for transferring data serially and recovering it on the receive side. The device can also be configured to operate as a non-encoded 10-bit transceiver with redundant I/O.

VSC7212 Block Diagram



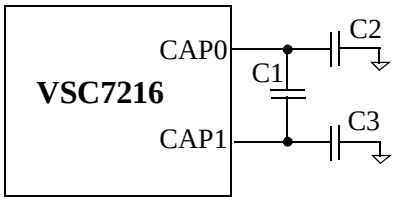
Notation

Differential signals (i.e., PTX+ and PTX-) may be referred to as a single signal (i.e., PTX) by dropping reference to the "+" and "- ". REFCLK refers to the single-ended TTL or differential PECL input pair REFCLKP/REFCLKN, whichever is used.

Clock Synthesizer

Depending on the state of the DUAL input, the VSC7212 clock synthesizer multiplies the reference frequency provided on the REFCLK input by 10 (DUAL is LOW) or 20 (DUAL is HIGH) to achieve a baud rate clock between 0.98GHz and 1.36GHz. The on-chip PLL uses a single external 0.1µF capacitor, connected between CAP0 and CAP1, to control the Loop Filter. This capacitor should be a multilayer ceramic dielectric, or better, with at least a 5V working voltage rating and a good temperature coefficient; NPO is preferred but X7R may be acceptable. These capacitors are used to minimize the impact of common-mode noise on the Clock Multiplier Unit, especially power supply noise. Higher value capacitors provide better robustness in systems. NPO is preferred because if an X7R capacitor is used, the power supply noise sensitivity will vary with temperature. For best noise immunity, the designer may use a three capacitor circuit with one differential capacitor between CAP0 and CAP1, C1, a capacitor from CAP0 to ground, C2, and a capacitor from CAP1 to ground, C3. Larger values are better but 0.1µF is adequate. However, if the designer cannot use a three capacitor circuit, a single differential capacitor, C1, is adequate. These components should be isolated from noisy traces.

Figure 1: Loop Filter Capacitors (Best Circuit)



C1=C2=C3= >0.1µF
MultiLayer Ceramic
Surface Mount
NPO (Preferred) or X7R
5V Working Voltage Rating

The REFCLK signal can be either single-ended TTL or differential LVPECL. If TTL, connect the TTL input to REFCLKP but leave REFCLKN open. If LVPECL, connect the inputs to REFCLKP and REFCLKN. Internal biasing resistors sets the proper DC Level to $V_{DD}/2$.

Transmitter Functional Description

Transmitter Data Bus

The VSC7212 transmitter has an 8-bit input transmit data character, T(7:0), and two control inputs, C/D and WSEN. The C/D input determines whether a normal data character or a special "K-character" is transmitted, and the WSEN input initiates transmission of a 16-character "Word Sync Sequence" used to align the receiver. These data and control inputs are clocked either on the rising edge of REFCLK, on the rising edge of TBC, or within the data eye formed by TBC ("ASIC-Friendly" timing). The transmit interface mode is controlled by TMODE(2:0) as shown in Table 1.

When used, TBC must be frequency locked to REFCLK. No phase relationship is assumed. A small skew buffer is provided to tolerate phase drift between TBC and REFCLK. This buffer is recentered by the RESETN input, and the total phase drift after recentering must be limited to +/- 180× (where 360× is one character time). The VSC7212 has an error output, TBERR, that is asserted HIGH to indicate that the phase drift between TBC and REFCLK has accumulated to the point that the elastic limit of the skew buffer has been exceeded and a transmit data character has been either dropped or duplicated. This error can not occur when input timing is referenced to REFCLK. The TBERR output timing is identical to the low-speed receiver outputs, as selected by RMODE(1:0) in Table 5.

Table 1: Transmit Interface Input Timing Mode

TMODE(2:0)	*Input Timing Reference*
0 0 0	REFCLK Rising Edge
0 0 1 0 1 X	Reserved
1 0 X	TBC Rising Edge
1 1 X	TBC Data Eye

The following figures show the possible relationships between data and control inputs and the selected input timing source. Figure 2 shows how REFCLK is used as an input timing reference. This mode of operation is also used in the VSC7211 and VSC7214. Figure 3 and Figure 4 show how TBC is used as an input timing reference. When TBC is used to define a data eye as shown in Figure 4, it functions as an additional data input that simply toggles every cycle.

Note that the REFCLK and TBC inputs are not used directly to clock the input data. Instead, an internal PLL generates edges aligned with the appropriate clock. The arrows on the rising edges of these signals define the reference edge for the internal phase detection logic. An internal clock is generated at 1/10 the serial transmit data rate that is locked to the selected input timing source. This is an especially important issue when DUAL is HIGH and input timing is referenced to REFCLK, since the falling edge is NOT used. The internal clock active edges are placed coincident with the REFCLK rising edges and halfway between the REFCLK rising edges in this mode.

A similar situation exists when TBC is used to define a data eye; only the rising edges of TBC are used to define the external data timing. The internal clock active edges are placed at 90× and 270× points between consecutive TBC rising edges (which are assumed to be 360× apart).

Figure 2: Transmit Timing, *TMODE(2:0)* = 000

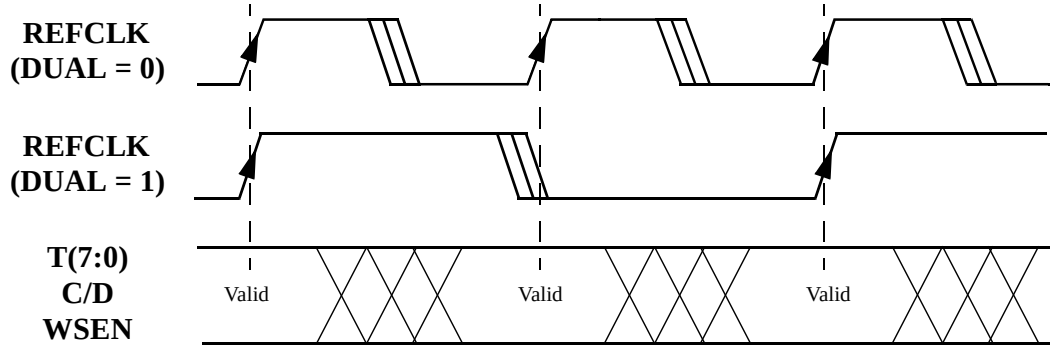


Figure 3: Transmit Timing, *TMODE(2:0)* = 10X

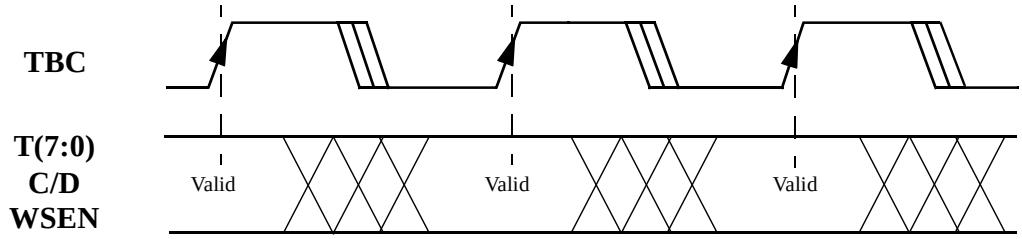
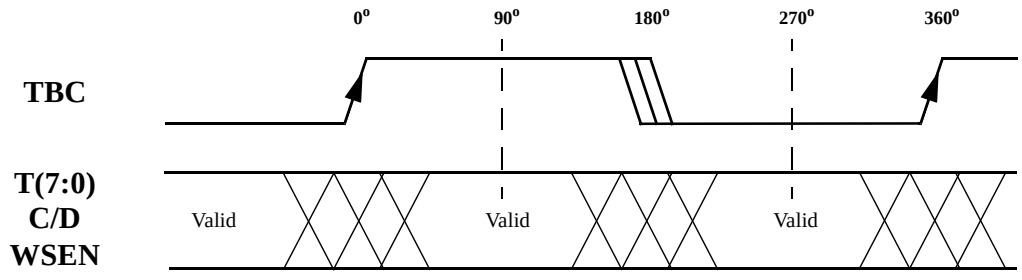


Figure 4: Transmit Timing, *TMODE(2:0)* = 11X ("ASIC-Friendly" Timing)



8B/10B Encoder

The VSC7212 contains an 8B/10B encoder which translates the 8-bit input data on T(7:0) into a 10-bit encoded data character. A C/D input is also provided which, along with KCHAR, allow the transmission of special Fibre Channel Kxx.x characters (see Table 2). Note that KCHAR is a static input, and does NOT have the same input timing as T(7:0), C/D and WSEN. Normally C/D is LOW in order to transmit data. If C/D is HIGH and KCHAR is LOW, then a Fibre Channel defined IDLE Character (K28.5 = '0011111010' or '1100000101' depending on disparity) is transmitted and T(7:0) is ignored. If C/D is HIGH and KCHAR is HIGH, a Kxx.x character is transmitted as determined by the data on T(7:0) (see Table 3). Data patterns other than those defined in Table 3 produce undefined 10B encodings.

Table 2: Transmit Data Controls

WSEN	*C/D*	*KCHAR*	*Encoded 10-bit Output*
0	0	X	Data Character
0	1	0	IDLE Character (K28.5)
0	1	1	Special Kxx.x Character
1	X	X	16-Character Word Sync Sequence

Table 3: Special Characters (Selected when C/D and KCHAR are HIGH)

Code	*T(7:0)*	*Comment*	*Code*	*T(7:0)*	*Comment*
K28.0	000 11100	User Defined	K28.6	110 11100	User Defined
K28.1	001 11100	User Defined	K28.7	111 11100	Test Only
K28.2	010 11100	User Defined	K23.7	111 10111	User Defined
K28.3	011 11100	User Defined	K27.7	111 11011	User Defined
K28.4	100 11100	User Defined	K29.7	111 11101	User Defined
K28.5	101 11100	IDLE	K30.7	111 11110	User Defined

Encoder Bypass Mode

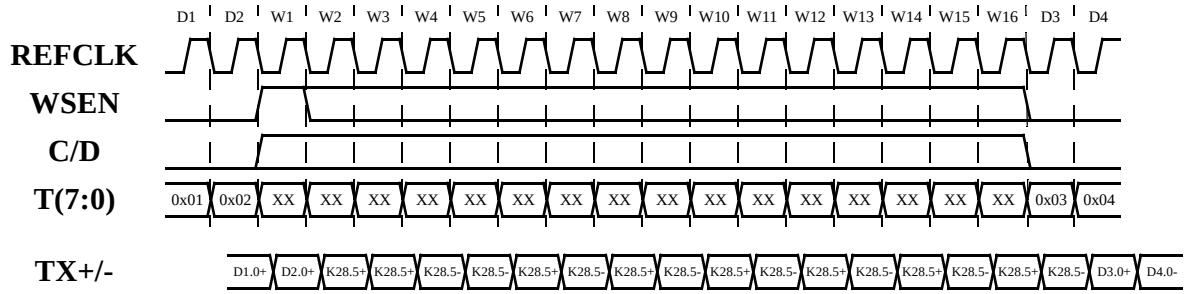
When ENDEC is LOW the 8B/10B encoder is bypassed and a 10-bit input character T(7:0) is serialized onto PTX/RTX with bit T0 is transmitted first. The C/D input becomes T8, and WSEN becomes T9. The KCHAR input becomes ENCDET which is not used in the transmitter, but when HIGH, enables "Comma" detection in the receiver. Refer to the "Decoder Bypass Mode" section for a description of this mode of operation in the receiver. The latency through the transmitter is reduced by one character time when ENDEC is LOW. This mode of operation is similar to a 10-bit interface commonly found in serializer/deserializers for the Fibre Channel (e.g., VSC7125) and Gigabit Ethernet markets (e.g., VSC7135).

Word Sync Generation

The VSC7212 can perform chip-to-chip alignment (also referred to as “word alignment” or “word sync”), meaning that the receive data output streams from multiple chips are aligned such that the same n-byte word presented to the n transmit channels for serialization will be transferred on the receive channel parallel outputs. The Word Sync Sequence provides a unique synchronization point in the serial data stream that is used to align the receive channels. This sequence consists of 16 consecutive K28.5 IDLE characters with disparity reversals on the second and fourth characters. The Word Sync Sequence is sent either as “I+ I+ I- I- I+ I- I+ I- I+ I- I+ I- I+ I- I+ I-” or as “I- I- I+ I+ I- I+ I- I+ I- I+ I- I+ I- I+ I- I+”, depending on the transmitter’s running disparity at the time the first IDLE character is serialized.

Transmission of the Word Sync Sequence is initiated when the WSEN input is asserted HIGH for one character time (see Figure 5). When WSEN is HIGH, the C/D and T(7:0) inputs are ignored. The WSEN, C/D and T(7:0) inputs are also ignored for the subsequent 15 character times. In Figure 5, the Word Sync Sequence is initiated in cycle W1 and transmitted through cycle W16. Normal data transmission (or the transmission of another Word Sync Sequence) resumes in cycle D3. This figure is drawn assuming that input timing is referenced to REFCLK (e.g. TMODE(2:0)=000) with the DUAL input LOW. As long as WSEN remains asserted, another Word Sync Sequence will be generated.

Figure 5: Word Sync Sequence Generation



Serializer

The 10-bit output from the encoder (or from the skew buffer if ENDEC is LOW) is fed into a multiplexer which serializes the parallel data using the synthesized transmit clock. The least significant bit of the 10B data is transmitted first. The VSC7212 has both primary and redundant serial output ports, PTX and RTX, respectively, which consist of differential PECL output buffers operating at either 10 or 20 times the REFCLK rate. The primary and redundant transmitter outputs are separately controllable. The primary PECL outputs PTX are enabled when the PTXEN input is HIGH, and the redundant PECL outputs RTX are enabled when the RTXEN input is HIGH. When a PECL output is disabled, the associated output buffers do not consume power and the attached pins are un-driven.

Receiver Functional Description

Serial Data Source

The receiver has both primary and redundant serial input ports, PRX and RRX, respectively, which consist of differential PECL input buffers. It also has a control input, RXP/R, used to select either the primary or redundant serial input as the data source. When RXP/R is HIGH, the serial data source is PRX. When LBEN(1:0)=10, the transmitter is looped back and becomes the serial data source regardless of the state of RXP/R (see Table 4).

Table 4: Serial Data Source Selection

LBEN(1:0)	*RXP/R*	*Serial Data Source*
≠ 1 0	0	RRX
≠ 1 0	1	PRX
= 1 0	X	LBTX (Loopback from PTX/RTX)

Signal Detection

The primary and redundant PECL input buffers have an associated signal detect output, PSDET and RSDET. Both outputs are available for continuous monitoring of the selected and non-selected input. Each signal detect output is asserted HIGH when transitions are detected on the associated PECL input and the signal amplitude exceeds 200mV. A LOW indicates that either no transitions are detected or the signal amplitude is below 100mV. The signal detect outputs are considered undefined when the signal amplitude is in the 100mV to 200mV range. The signal detect circuitry behaves like a re-triggerable one shot that is triggered by signal transitions, and whose time-out interval ranges from 40 to 80 bit times. The transition density is not checked to make sure that it corresponds to a valid Fibre Channel data stream. The PSDET and RSDET output timing is identical to the low-speed receiver outputs, as selected by RMODE(1:0) in Table 5.

Receiver Equalization

Incoming data on the PRX/RRX input typically contains a substantial amount of Inter Symbol Interference (ISI) or deterministic jitter which reduces the ability of the receiver to recover data without errors. An equalizer has been added to each of the receiver's input buffers in order to compensate for this deterministic jitter. This circuit has been designed to effectively reduce the ISI commonly found in copper cables or backplane traces due to low frequencies traveling faster than high frequencies as a result of the skin effect. The equalizer boosts high frequency edge response in order to reduce the adverse effects of ISI.

Clock and Data Recovery

The receiver has a Clock Recovery Unit (CRU) which accepts the selected serial input source, extracts the high-speed clock and retimes the data. The CRU is monolithic. The CRU automatically locks on data and if the data is not present, will automatically lock to the REFCLK. This maintains a very well-behaved recovered clock, RCLK/RCLKN which does not contain any slivers and will operate at a frequency of the REFCLK reference +/- 200 ppm. The use of an external Lock-to-Reference pin is not needed.

The Clock Recovery Unit must perform bit synchronization which occurs when the CRU locks onto and properly samples the incoming serial data as described in the previous paragraph. When the CRU is not locked onto the serial data, the 10-bit data out of the decoder is invalid which results in numerous 8B/10B decoding errors or disparity errors. When the link is disturbed (e.g., the cable is disconnected or the serial data source is switched), the CRU will require a certain amount of time to lock onto data, which is specified in the AC Timing Specification for “Data Acquisition Lock Time.”

Deserializer and Character Alignment

The retimed serial data stream is converted into 10-bit characters by the deserializer. A special 7-bit “Comma” pattern (‘0011111xxx’ or ‘1100000xxx’) is recognized by the receiver and allows it to identify the 10-bit character boundary. Note that this pattern is found in three special characters, K28.1, K28.5 and K28.7. However, K28.5 is chosen as the unique IDLE character. Only K28.1 and K28.5 should be used in normal operation. The K28.7 character should be reserved for test and characterization use.

Character alignment occurs when the deserializer synchronizes the 10-bit character framing boundary to a “Comma” pattern in the incoming serial data stream. If the receiver identifies a “Comma” pattern in the incoming data stream which is misaligned to the current framing boundary the receiver will re-synchronize the recovered data in order to align the data to the new “Comma” pattern. Re-synchronization ensures that the “Comma” character is output on the internal 10-bit bus so that bits 0 through 9 equal ‘0011111xxx’ or ‘1100000xxx’. If the “Comma” pattern is aligned with the current framing boundary, then re-synchronization will not change the current alignment. Re-synchronization is always enabled and cannot be turned off when ENDEC is HIGH. After character re-synchronization the VSC7212 ensures that within a link, the 8-bit data sent to the transmitting VSC7212 will be recovered by the receiving VSC7212 in the same bit locations as the transmitter (i.e. T(7:0) = R(7:0)). When ENDEC is LOW, “Comma” detection and alignment are enabled only if KCHAR is HIGH.

10B/8B Decoder

The 10-bit character from the deserializer is decoded in the 10B/8B decoder, which outputs the 8B data byte and three bits of status information. If the 10-bit character does not match any valid value, an Out-of-Band Error is generated which is output on the receiver status bus. Similarly, if the running disparity of the character does not match the expected value, a Disparity Error is generated. The decoder also reports when a K-character is received, and distinguishes the K28.5 (IDLE) character from other K-characters. This status information is combined with LOS State Machine status and FIFO error status, to produce the prioritized per-character link status output information (see Table 7).

Elastic Buffer and Channel De-Skewing

An elastic buffer is included in the receiver. Decoded data and status information is written into these buffers with the recovered clock, and is read with the selected word clock (either the recovered clock or REFCLK). In addition to allowing decoded data to easily cross from a receiver's recovered clock domain to its output clock domain, the elastic buffer facilitates chip-to-chip alignment (the reconstruction of a multi-byte word as presented to the transmitting devices), and facilitates rate matching via IDLE character insertion/deletion when the receiver's recovered clock is not frequency-locked to its selected word clock.

There are three conditions under which a receiver's elasticity buffer is recentered. The RESETN input, when asserted LOW, recenters the read/write pointers in the elasticity buffer. Whenever a "Comma" character is received which changes the receive character's framing boundary, the elasticity buffer is recentered. Lastly, it is also recentered whenever the receiver detects the synchronization point in the Word Sync Sequence. All three of these events are associated with chip initialization or link initialization and would not occur during normal data transfer. Note that recentering can result in the loss or duplication of decoded character data and status information.

When a condition changes transmit timing (e.g., phase shifts in TBC) or shifts phase/alignment into the receiver, the user should resend a Word Sync Event or assert RESETN in order to recenter the elasticity buffer. Otherwise, data corruption could occur. It is unsafe to assume that after a change in transmit timing that "Comma" characters will be misaligned and will cause recentering

The VSC7212 presents recovered data on R(7:0) and status on IDLE, KCH and ERR. These outputs are timed either to the receiver's recovered clock (RCLK/RCLKN) or to REFCLK. The output timing reference is selected by RMODE(1:0) (see Table 5). TBERR, PSDET and RSDET are also synchronized to the selected word clock. There are two choices for REFCLK-based timing, which differ in the positioning of the data valid window associated with the output signals timed to REFCLK. When RMODE(1:0)=00 REFCLK is approximately centered in the output data valid window as in the VSC7211 or VSC7214. When RMODE(1:0)=01 REFCLK slightly leads the data valid window so that output data appears to have a more typical "Clock-to-Q" timing relationship to REFCLK.

Table 5: Receive Interface Output Timing Mode

RMODE(1:0)	*Output Timing Reference*
0 0	REFCLK (Centered)
0 1	REFCLK (Leading)
1 X	RCLK/RCLKN

The term "word clock" will be used for whichever clock, REFCLK or RCLK/RCLKN, is selected as the output timing reference. If RMODE(1) is HIGH, the receiver's RCLK/RCLKN outputs are complementary outputs at 1/10th or 1/20th the baud rate of the incoming data depending upon DUAL. If RMODE(1) is LOW, then the RCLK/RCLKN outputs are held HIGH/LOW and the data bus and status outputs are timed to REFCLK. If DUAL is HIGH, all data at the receiver's output port is synchronously clocked out on both positive and negative edges of the selected word clock at 1/20th the baud rate. If DUAL is LOW, the data is clocked out

of the VSC7212 only on the rising edge of the selected word clock at 1/10th the baud rate. Timing waveforms for the output data and status are shown in Figure 6, Figure 7 and Figure 8.

Figure 6: Receive Timing, *RMODE(1:0)* = 00

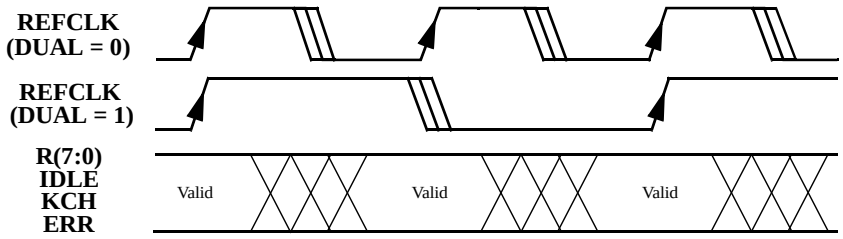


Figure 7: Receive Timing, *RMODE(1:0)* = 01

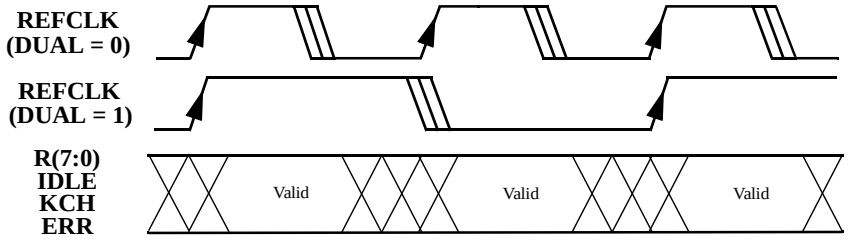
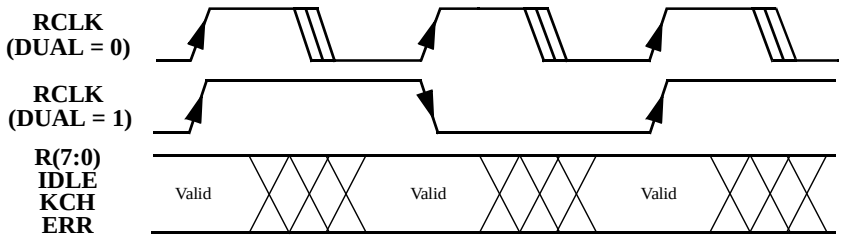


Figure 8: Receive Timing, *RMODE(1:0)* = 1X



If RMODE1 is LOW and if the transmitting device's REFCLK is not precisely frequency-locked to a receiver's REFCLK, then the channel's elastic buffer will tend to gradually fill or empty as the recovered clock (which is by definition frequency-locked to the transmitter's REFCLK) steadily drifts in phase relative to the word clock. In order to accommodate frequency differences between a transmitter's REFCLK and the receiver's REFCLK, the VSC7212 can automatically perform "rate matching" by either deleting or duplicating IDLE characters. FLOCK must be LOW and WSI must be connected to WSO to enable rate matching. It is the user's responsibility to ensure that the frequency at which IDLEs are transmitted accommodates the frequency differences, if any, in their system architecture. Not meeting the IDLE density requirements described below may result in Underrun/Overrun Errors.

The elastic buffer is designed to allow a maximum phase drift of +2 or -2 serial clock bit times between re-synchronizations, which sets a limit on the maximum data "packet" length allowed between IDLEs. This maximum packet length depends on the frequency difference between the transmitting and receiving devices REFCLKs. Let $\Delta\phi$ represent phase drift in bit times, and let 2π represent one full 10-bit character of phase drift. Limiting phase drift to two bit times means the following inequality must be satisfied:

(1) $$\Delta\phi \leq (0.2 \times 2\pi)$$

Let L be the number of 10-bit characters transmitted, and let Df be the frequency offset in ppm. The total phase drift in bit times is given by:

(2) $$\Delta\phi = (\Delta f / 10^6) \times 2\pi L$$

A simple expression for maximum packet length as a function of frequency offset is derived by substituting (2) in (1) and solving for L:

(3) $$L \leq (0.2 \times 10^6) / \Delta f$$

As an example, if the frequency offset is 200ppm, then the maximum packet length should not be more than 1K bytes. To increase the maximum packet length L, decrease the frequency offset Df. Note that if only one K28.5 is transmitted between "packets" of data, it might be dropped during compensation for phase drift. If the user must have at least one K28.5 between these two packets, then two K28.5s must be transmitted.

Using Multiple VSC7212s in Parallel

Multiple VSC7212s and VSC7216s can be used in parallel to form wider bus widths. In order for chip-to-chip word alignment to function correctly across multiple devices, each transmit channel's input data must be transmitted synchronously to a common REFCLK or TBC, and each receiver's output data must also be aligned to a common REFCLK. This requires that all transmitting devices use either the same or identical REFCLKs, and that TMODE(2:0)=000 (inputs timed to REFCLK) or TMODE(2:0)=1X0 (inputs timed to TBC). If inputs are timed to TBC, then all transmitting devices must use either the same or identical TBCs. Since all receive channels must use a common word clock, the receiving devices must also use the same or identical REFCLKs and it must be selected as the word clock for all receive channels (RMODE(1:0)=0X).

Within the receiver there are elastic buffers used to deskew multiple VSC7212s and/or VSC7216s in order to align them to a common word clock. The receiver's elastic buffer allows the chips' input to be skewed up to +/-7 bit times in order to accommodate circuit imperfections, differences in transmission delay and jitter. Multiple devices can be used in synchronous operation if the skew between all serial input pairs is maintained less than +/-7 serial clock bit times. This allows easy implementation of robust systems.

Chip-to-Chip word alignment is enabled by connecting the WSI input of all devices to the WSO output of an arbitrarily selected "Master" device. The FLOCK input state and WSI input source determine whether or not rate matching (IDLE deletion or duplication) will be performed. Chip-to-chip alignment is disabled when WSI is not connected to a WSO output. Rate matching is disabled when either FLOCK is HIGH or WSI is held LOW (see Table 6).

In order to perform word alignment, a synchronization point must be seen across all receivers to be aligned within the +/-7 bit time window. The VSC7212 receiver recognizes the first four characters of the Word Sync Sequence (either K28.5+ K28.5+ K28.5- K28.5- or K28.5- K28.5- K28.5+ K28.5+) as the synchronization point. As a model for understanding, consider the case where two VSC7212 transmitters send 16 bits of data to two receivers via copper media which has small cable length differences causing chip-to-chip skew. Both transmitters must be word aligned by simultaneously sending the Word Sync Sequence (within the +/-7 bit window). On detection of the synchronization point, the receivers will reposition the recovered data within their elastic buffers in order to align both devices and remove any chip-to-chip skew. All normal data characters following the Word Sync Sequence will be properly chip-to-chip word aligned. In the process of alignment, one or two of the final twelve K28.5 characters in the Word Sync Sequence may be deleted or duplicated.

The VSC7212 is capable of performing rate matching in multiple device applications by inserting or deleting IDLEs in parallel across all receivers. This requires that the chip-to-chip aligned data streams contain IDLEs inserted simultaneously on all transmitters according to the IDLE density requirement previously described.

Table 6: Word Alignment and Rate Matching Control

FLOCK	*WSI Source*	*Chip-to-Chip Alignment*	*Rate Matching*
0	0	Off	Off
0	It's own **WSO** or 1	Off	Enabled within chip
0	Another chips' WSO	Enabled	Enabled between chips
1	0	Off	Off
1	1	Off	Off
1	Another chips' WSO	Enabled	Off

There are four distinct modes of operation defined in Table 6. The first row disables both word alignment and rate matching. (The fourth and fifth row configurations function identically to the first row.) The second row configures the VSC7212 to perform rate matching within its receiver without regard to other devices. Word alignment is disabled and IDLEs will be dropped/duplicated independently of other devices. The third row configures the part to perform word alignment and rate matching across multiple devices. All receivers will be aligned per the device driving **WSO**, and IDLE words will be dropped/duplicated across the aligned channels as required. The last row configures the part to perform word alignment and disables rate matching. This mode of operation is appropriate for a frequency-locked application where it desired to align the receive channels without altering the received data streams.

WSO uses a simple 3-bit serial protocol, synchronous to the Master device's selected word clock, for indicating the required synchronization action to other VSC7212s. A steady LOW level indicates no action is required. '101' indicates that Master device has seen a Word Sync Event. The relative timing relationship between receiving a Word Sync Event (on all devices together) and seeing '101' on the **WSI** input in the other channels allows these channels to word-synchronize with to the Master. '110' indicates that the next IDLE encountered in the receive data stream should be deleted. '111' indicates that an IDLE should be inserted after the next IDLE encountered in the receive data stream. Note that the arbitrarily chosen Master device must have valid input data.

Decoder Bypass Mode

If ENDEC is LOW, the 8B/10B decoder is bypassed and a 10-bit received character, R(9:0), is output from the receiver. The KCH output becomes R8, and ERR becomes R9. Character alignment is handled differently in this mode of operation. As mentioned in the "Encoder Bypass Mode" section, the KCHAR input becomes ENCDET which enables "Comma" detection and re-synchronization when HIGH, and disables re-synchronization when LOW. Only the '0011111xxx' version of the Comma pattern is recognized when ENDEC is LOW. The IDLE output becomes COMDET (Comma Detect) which signals detection of the '0011111xxx' Comma pattern in the current 10-bit output character when high. This mode of operation is equivalent to a 10-bit interface commonly found in serializer/deserializers for the Fibre Channel (e.g., VSC7125) and Gigabit Ethernet markets (e.g., VSC7135).

The logic used to align multiple devices and perform rate matching is disabled when ENDEC is LOW. In order for this mode of operation to function without errors, the word clock source as selected by RMODE(1:0) must be frequency locked to the REFCLK of the remote transmitting device in each channel. This is guaranteed when RMODE(1:0) = 11. For other choices of RMODE(1:0) the frequency locked condition must be guaranteed by system design. When DUAL is HIGH and RMODE(1:0) = 10 or 11, the character containing the '0011111xxx' "Comma" pattern is aligned to RCLK/RCLKN so that COMDET will be asserted on the falling edge of RCLK (rising edge of RCLKN). This is done by adjusting the latency through the elastic buffer, the recovered clock is never stretched or slivered. When the "Comma" pattern changes the framing boundary, data characters prior to the assertion of COMDET on the falling edge of RCLK may be corrupted.

Receiver State Machine

The VSC7212 contains a Loss of Synchronization State Machine (LSSM) which is responsible for detecting and handling loss of bit and word clock synchronization in a controlled manner. There are three states in the LSSM: LOSS_OF_SYNC, RESYNC and SYNC_ACQUIRED as shown in the state diagram of Figure 9. The RESYNC state is entered when a 10-bit word has been received which contains the 7-bit "Comma" pattern (e.g., a K28.5 IDLE character). After entering the RESYNC state, the VSC7212 will stay in it until a valid, "non-Comma" transmission is received, then it transitions to the SYNC_ACQUIRED state indicating a normal operating condition. The RESYNC state is re-entered if four consecutive "Commas" are received or if a single "Comma" is received that changes the 10B character framing boundary. The LOSS_OF_SYNC state is entered whenever four consecutive invalid transmissions have been detected or when the occurrences of invalid transmission outnumber those of valid transmission by four. The relative occurrences of invalid vs. valid transmissions are monitored with a simple up/down counter that increments when an invalid transmission is detected and decrements otherwise. The LSSM transitions to the LOSS_OF_SYNC state when the counter reaches four, and the counter is reset. A state diagram for the invalid transmission counter is shown in Figure 10. The VSC7212 receiver will stay in the LOSS_OF_SYNC state until a valid "Comma" pattern is detected. Note that the RESYNC state is entered whenever the 10B framing boundary is changed, and whenever the Word Sync Sequence is received. When ENDEC is LOW, the LSSM logic is disabled.

Figure 9: State Diagram of the Loss of Synchronization State Machine

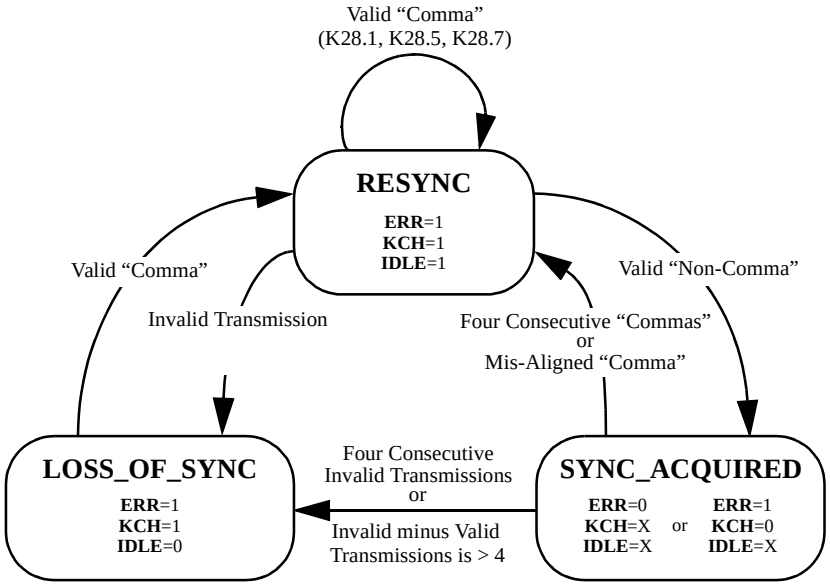
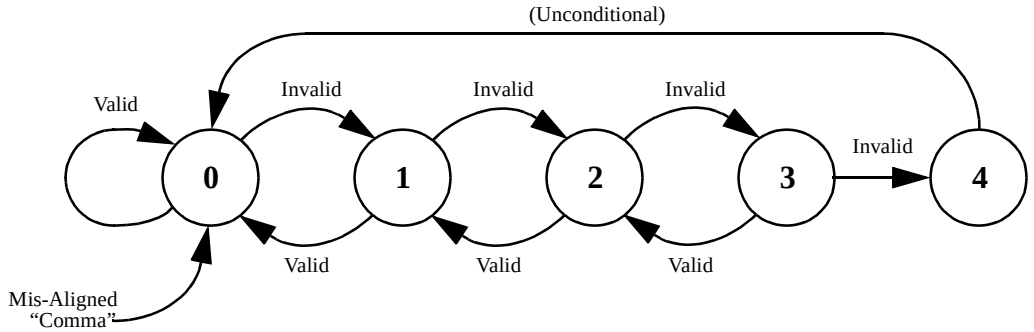


Figure 10: State Diagram of the Invalid Transmission Counter



Link Status Outputs

On the receiver output bus, the **ERR**, **KCH** and **IDLE** outputs indicate status for the receiver as shown below in Table 7. Since this status is encoded, multiple conditions could occur simultaneously so the states are prioritized as indicated (1 being highest priority). For example, if both Out-of-Band and Disparity Errors occur, only an Out-of-Band Error is reported because it has higher priority.

The **ERR**, **KCH** and **IDLE** status signals apply to the data on **R(7:0)** on a per-character basis. The only exception to this is the Underrun/Overrun indication, which is asserted coincident with the duplicated character when an underrun occurs, and is asserted following the deleted character (i.e. on the cycle where the deleted character should have appeared) when an overrun occurs.

Table 7: Receiver Status Signals

ERR	*KCH*	*IDLE*	*Priority*	*Link Status*
0	0	0	7	**Valid Data Transmission:** A valid 10B data character with correct disparity was received. The correctly decoded version of this character is on R(7:0).
0	0	1	1	**Underrun/Overrun Error:** The elastic buffer has not been able to add/drop an IDLE when required. Data on R(7:0) is invalid.
0	1	0	6	**Kxx.x Special Character Detected (not IDLE):** A valid 10B special character with correct disparity was received. The correctly decoded version of this character, per Table 3, is on R(7:0).
0	1	1	5	**IDLE Detected:** A valid IDLE character (K28.5) with correct disparity was received. The correctly decoded version of this character, per Table 3, is on R(7:0).
1	0	0	3	**Out-of-band Error Detected**: A character was received which was not a valid 10B data or control character. Data on R(7:0) is invalid.
1	0	1	4	**Disparity Error Detected:** A valid 10B character was received which did not have the expected disparity. R(7:0) is invalid.
1	1	0	2	**Loss of Synchronization:** The receiver state machine is in the Loss-of-Sync state. Data on R(7:0) is invalid.
1	1	1	2	**RESYNC:** The receiver state machine is in the re-Synchronization state. Data on R(7:0) is a decoded version of K28.1, K28.5 or K28.7.

Loopback Operation

Loop back control pins, LBEN(1:0), are provided to internally loopback data paths for on-chip diagnosis. Both serial and parallel loopback functions are provided.

Table 8: Loopback Mode Selection

LBEN(1:0)	*Loopback Mode*
0 0	Normal Operation
0 1	Internal Parallel Loopback
1 0	Internal Serial Loopback
1 1	Reserved

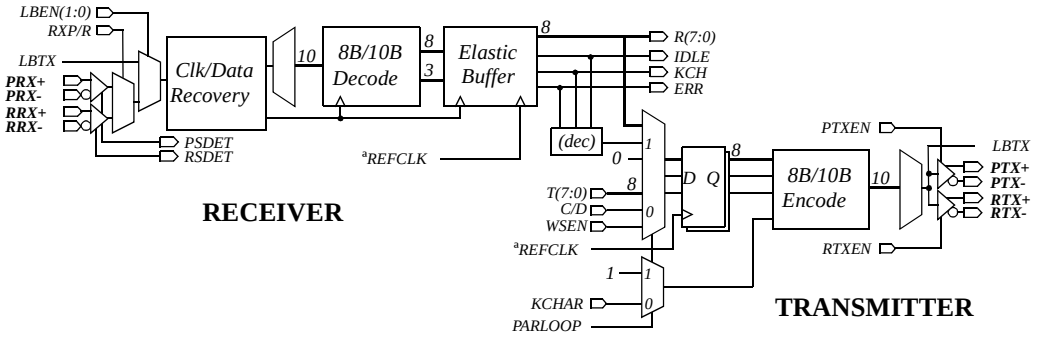
When LBEN(1:0)=10, Serial Loopback mode is selected. The transmitter's serial transmit data is internally connected to the receiver's CRU input. The serial loopback paths are labelled LBTX in the VSC7212 block diagram on the first page. This allows parallel data on T(7:0) to be encoded, serialized, looped back, deserialized and decoded. This mode is intended for the system to verify functionality of the local VSC7212 prior to attempting to establish an external link. The PTX and RTX outputs are unaffected by the state of LBEN(1:0).

When LBENn(1:0)=01, Parallel Loopback mode is selected. The R(7:0) outputs are looped back to the T(7:0) inputs (see Figure 11). WSEN does not have a loopback source and is internally connected to a logic LOW. KCHAR does not have a loopback source and is internally connected to a logic HIGH. The C/D input is obtained by decoding the link status outputs such that either a data character, special character, or IDLE (K28.5) is transmitted. When the link is in the LOS or RESYNC states, C/D is asserted and the data path is set to 0xBC so that an IDLE will be transmitted. For other link status conditions C/D follows the KCH status bit. This guarantees that IDLE and special characters will be correctly looped back along with normal data, and also has the effect of looping back the data received as a normal data character when a disparity error, out-of-band character, or underflow/overflow link status condition occurs.

In Parallel Loopback mode the receiver uses REFCLK as the word clock with RMODE(1:0) internally set to 00. This data is looped back to the transmitter with TMODE(2:0) internally set to 000. This guarantees that the parallel loopback data to be re-transmitted will be frequency locked to the transmitter's REFCLK, but means that the receiver parallel output data timing may not match the normal system timing that is externally selected by RMODE(1:0). In this case, the parallel output data should be ignored.

This internal loopback configuration also allows rate matching to be performed in the receivers' elastic buffers. Rate matching is controlled and operates exactly the same way that it does in normal mode. This is needed to avoid receiver Overrun/Underrun errors in the loopback device if the remote transmitting device's REFCLK is not frequency locked to the loopback device's REFCLK. Keep in mind that the LBEN(1:0), RXP/R, PTXEN, RTXEN and BIST inputs must all be configured appropriately in order for end-to-end parallel loopback to function correctly in a user environment. Parallel Loopback mode is internally disabled when BIST mode is enabled.

Figure 11: Parallel Loopback Mode Operation

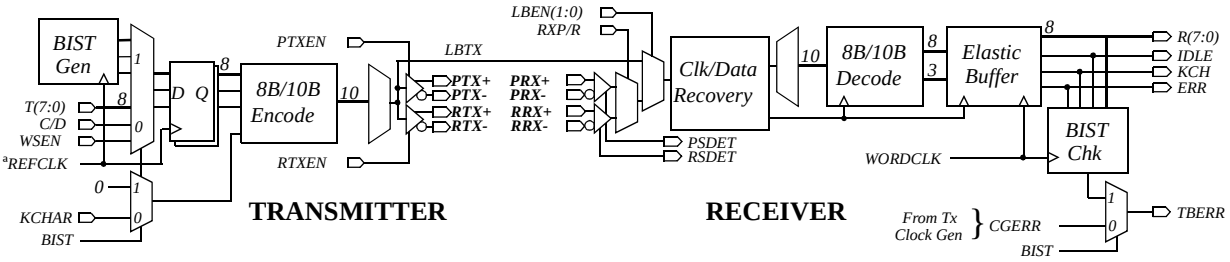


Built-In Self Test Operation

Built-In Self Test operation is enabled when the BIST input is HIGH, which causes TMODE(2:0) to be internally set to 000. Upon entering BIST mode, the transmitter will issue a Word Sync Sequence in order to recenter the elasticity buffers in the receive channel. Then the transmitter repeatedly sends a simple 256-byte incrementing data pattern (prior to 8B/10B encoding) followed by three IDLE characters (K28.5). Note that this incrementing pattern plus three IDLEs will cause both disparities of each data character and the IDLE character to be transmitted, and contains a sufficient IDLE density for any application requiring IDLE insertion/deletion. It is up to the user to enable IDLE insertion/deletion if the receiver's word clock is not frequency locked to the transmitter's REFCLK.

The receiver monitors incoming data for this pattern and indicates if any errors are detected. Correct reception of the pattern is reported on each receiver's TBERR output, a LOW means the pattern is being received correctly and a HIGH means that errors are detected. When BIST transitions from LOW to HIGH, each TBERR output is initialized HIGH. It will be cleared LOW whenever one or more IDLE characters followed by all 256 data characters are sequentially received without error, and set HIGH whenever a pattern mis-match or receiver error is encountered. Received data and associated status will be output as in normal operation. Please note that Serial Loopback mode and receiver output timing mode selection via RMODE(1:0) operate independently of BIST mode, but BIST mode disables Parallel Loopback mode.

Figure 12: BIST Mode Operation



Compatibility with VSC7214 and VSC7211

Care has been taken in the functional definition of the VSC7212 to be sure that it is compatible with the VSC7211 and VSC7214 at the serial link level, and that the transmitter and receiver low-speed interfaces have compatible modes of operation. It is strongly recommended that the VSC7212 not be connected in any way through the WSO and/or WSI pins to a VSC7211 or VSC7214.

Serial Link Compatibility

The VSC7212 uses the same Fibre Channel 8b/10b encoding scheme and the same Word Sync Sequence used in the VSC7211 and VSC7214. The only difference in serial link operation is that the VSC7211 and VSC7214 require four consecutive identically-aligned "Comma" patterns to set the character framing boundary, while the VSC7212 requires a single "Comma." This means that from the LOSS_OF_SYNC state, the VSC7212 will make an earlier transition to the RESYNC state (one "Comma" instead of four) as shown in Figure 9. Once out of the LOSS_OF_SYNC state, there is no difference in receiver behavior in the absence of data link errors. When transmitting in multiple chip aligned mode from a VSC7212 to a VSC7211 or VSC7214, use TMODE(2:0)=000 or =1X0 (common transmit interface timing source) to minimize transmitter inter-channel skew.

Parallel Interface Compatibility

In general the VSC7212 low-speed parallel interfaces can be configured so that there are input and output signals that are compatible with their VSC7211 and VSC7214 counterparts. On the transmit interface, the signals T(7:0) and C/D behave identically on the VSC7212 as long as the input timing is referenced to REFCLK (i.e. TMODE(2:0)=000). On the receive interface, the signals R(7:0), ERR, KCH and IDLE behave identically on the VSC7212 as long as the output data is centered around REFCLK (RMODE(1:0)=00) or timed to RCLK/RCLKN (RMODE(1:0)=10). When RMODE(1:0)=10 the VSC7212 RCLK/RCLKN outputs provide four copies of RCLK/RCLKN, which are equivalent to the VSC7211 and VSC7214 RCLK/RCLKN outputs.

The VSC7212 KCHAR input is no longer a synchronous input timed to REFCLK as on the VSC7211 and VSC7214. It is a static input used to define the control character encoding mode when C/D=1 as shown in Table 2.

Operational Mode Compatibility

The VSC7211 and VSC7214 specifications define eight operating modes based on the binary combinations of the RCLKEN, FLOCK and INDEP inputs. Note that these mode inputs control VSC7211 and VSC7214 receiver operation only, and have no effect on transmitter operation. For each of these modes, the equivalent VSC7212 receiver configuration is presented. There is no INDEP input in the VSC7212.

VSC7214 MODE 0: RCLKEN=LOW, FLOCK=LOW, INDEP=LOW

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to REFCLK, IDLE insertion/deletion is enabled, and multiple receivers are word aligned. The VSC7212 should be configured with RMODE(1:0)=00, FLOCK=0, and WSI connected to its own WSO or to the WSO of another VSC7212 if multiple devices are to be used in parallel. The WSI connection allows IDLE insertion/deletion to occur in parallel across all word-aligned devices.

VSC7214 MODE 1: RCLKEN=LOW, FLOCK=LOW, INDEP=HIGH

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to REFCLK, IDLE insertion/deletion is enabled. The VSC7212 should be configured with RMODE(1:0)=00, FLOCK=0, and WSI=1. The WSI connection inhibits chip-to-chip alignment, and allows IDLE insertion/deletion to occur independently in each device.

VSC7214 MODE 2: RCLKEN=LOW, FLOCK=HIGH, INDEP=LOW

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to REFCLK, IDLE insertion/deletion is disabled, and multiple receivers are word aligned. The VSC7212 should be configured with RMODE(1:0)=00, FLOCK=1, and WSI connected to its own WSO or to the WSO of another VSC7212 if multiple devices are to be used in parallel. The WSI connection allows word alignment to occur, and the FLOCK connection inhibits IDLE insertion/deletion.

VSC7214 MODE 3: RCLKEN=LOW, FLOCK=HIGH, INDEP=HIGH

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to REFCLK, IDLE insertion/deletion is disabled. The VSC7212 should be configured with RMODE(1:0)=00, FLOCK=1, and WSI=0. The WSI connection inhibits chip-to-chip alignment, and the FLOCK connection inhibits IDLE insertion/deletion.

VSC7214 MODE 4: RCLKEN=HIGH, FLOCK=LOW, INDEP=LOW

This configuration does not require IDLE insertion/deletion, use Mode 6 instead.

VSC7214 MODE 5: RCLKEN=HIGH, FLOCK=LOW, INDEP=HIGH

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to RCLK/RCLKN, IDLE insertion/deletion is enabled. The VSC7212 should be configured with RMODE(1:0)=10, FLOCK=0, and WSI=1. The WSI connection inhibits chip-to-chip alignment, and allows IDLE insertion/deletion to occur.

VSC7214 MODE 6: RCLKEN=HIGH, FLOCK=HIGH, INDEP=LOW

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to RCLK/RCLKN, IDLE insertion/deletion is disabled, and multiple receivers are word aligned. The VSC7212 should be configured with RMODE(1:0)=10, FLOCK=1, and WSI connected to its own WSO. Multiple VSC7212 devices should not be used in parallel when the outputs are synchronous to RCLK/RCLKN. The WSI connection allows word alignment to occur, and the FLOCK connection inhibits IDLE insertion/deletion.

VSC7214 MODE 7: RCLKEN=HIGH, FLOCK=HIGH, INDEP=HIGH

Receiver R(7:0), ERR, KCH and IDLE outputs are synchronous to RCLK/RCLKN, IDLE insertion/deletion is disabled. The VSC7212 should be configured with RMODE(1:0)=10, FLOCK=1, and WSI=0. The WSI connection inhibits chip-to-chip alignment, and the FLOCK connection inhibits IDLE insertion/deletion.

AC Characteristics

Figure 13: Transmit Input Timing Waveforms with *TMODE* = 000

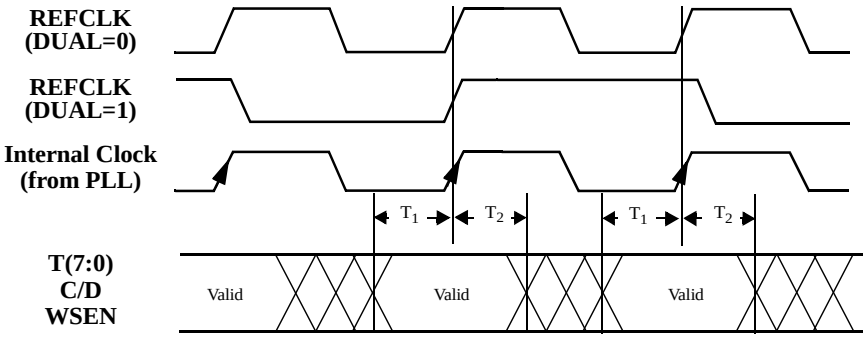


Figure 14: Transmit Input Timing Waveforms with *TMODE* = 10X

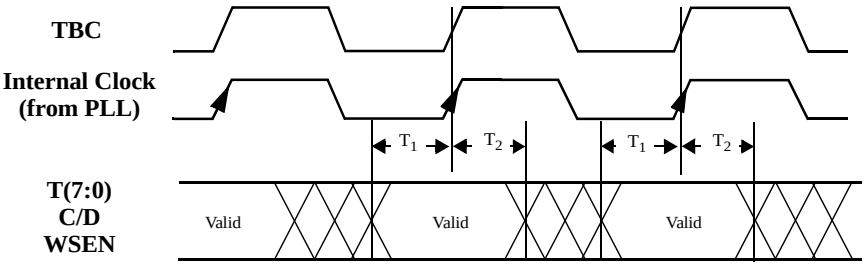


Table 9: Transmit Input AC Characteristics with *TMODE* = 000 or *TMODE* = 10X

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_1	Input Setup time to the rising edge of REFCLK or TBC	1.5	—	ns	Measured between the valid data level of the input and the 1.4V point of REFCLK or TBC
T_2	Input Hold time after the rising edge of REFCLK or TBC	1.0	—	ns	

Figure 15: Transmit Input Timing Waveforms with *TMODE* = 11X ("ASIC-Friendly" Timing)

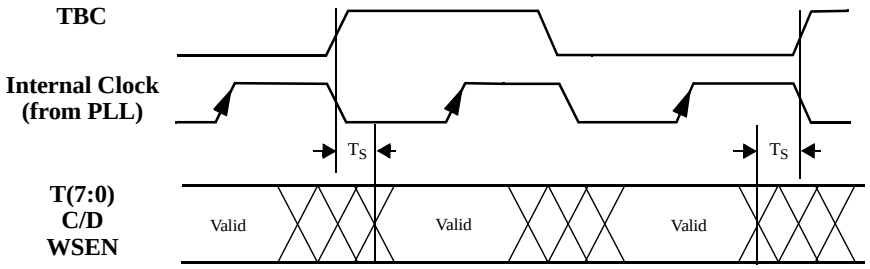


Table 10: Transmit Input AC Characteristics with *TMODE* = 11X

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_S	Input Skew relative to the rising edge of TBC	—	2.0	bc	Measured between the valid data level of the input and the 1.4V point of TBC

Figure 16: Transmit Serial Timing Waveforms

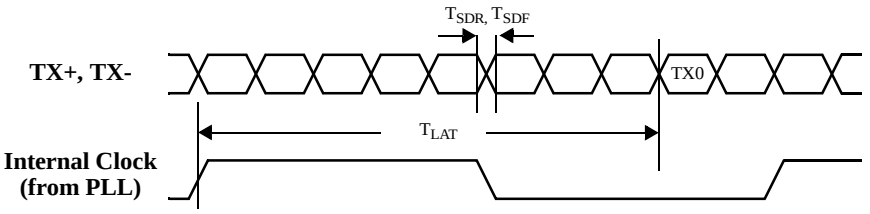


Table 11: Transmit Serial AC Characteristics

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{SDR}, T_{SDF}	TX+/- rise and fall time	—	330	ps	Between $V_{OL(MAX)}$ and $V_{OH(MIN)}$
T_{LAT}	Latency, REFCLK to TX0 Latency, TBC to TX0	22bc+0.2ns 36bc+0.0ns	22bc+0.8ns 38bc+0.3ns	bc + ns	ENDEC=1 TMODE=000 ENDEC=1 TMODE=10X
T_J	Serial data output Total Jitter (p-p)	—	192	ps	IEEE 802.3z Clause 38.69, Tested on a sample basis
T_{DJ}	Serial data output Deterministic Jitter (p-p)	—	80	ps	IEEE 802.3z Clause 38.69, Tested on a sample basis

Figure 17: Receive Output Timing Waveforms with *RMODE* = 00 or 01

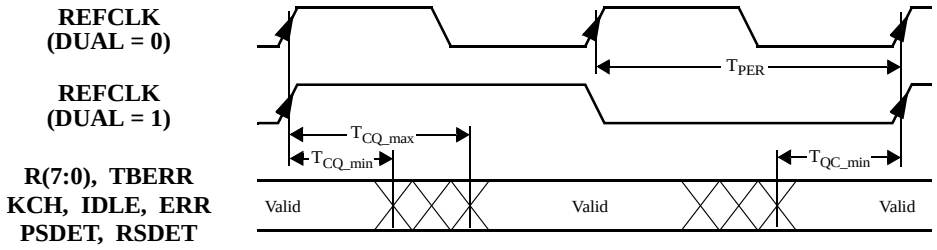


Table 12: Receive Output AC Characteristics with *RMODE* = 00 or 01

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{CQ}	REFCLK Rising Edge to TTL Output Transition	2.58 ns - 0 bc	5.43 ns - 0 bc	ns	RMODE = 00 bc = Bit Clock
T_{CQ}	REFCLK Rising Edge to TTL Output Transition	2.58 ns - 2 bc	5.43 ns - 2 bc	ns	RMODE = 01 bc = Bit Clock
T_{QC}	TTL Output Transition to REFCLK Rising Edge	T_{PER} - T_{CQ_max}	T_{PER} - T_{CQ_min}	ns	

Figure 18: Receive Output Timing Waveforms with *RMODE* = 10 or 11

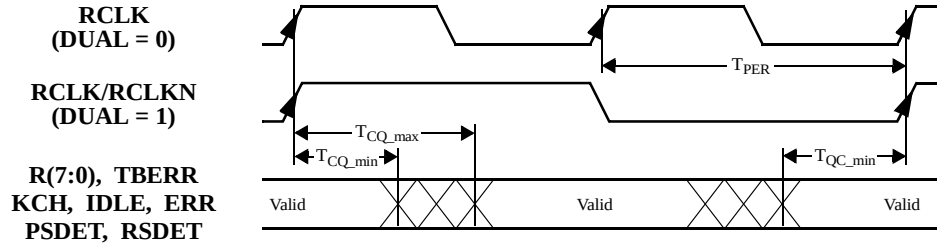


Table 13: Receive Output AC Characteristics with *RMODE* = 10 or 11

Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
T_{CQ}	RCLK/RCLKN Rising Edge to TTL Output Transition	-1.25 ns + 4 bc	1.25 ns + 4 bc	ns	RMODE = 10 or 11 bc = Bit Clock
T_{QC}	TTL Output Transition to RCLK/ RCLKN Rising Edge	T_{PER} - T_{CQ_max}	T_{PER} - T_{CQ_min}	ns	
DC	RCLK/RCLKN Duty Cycle	50% - 1 ns	50% + 1 ns	ns	Measured at 1.4 V

Figure 19: RCLK and RCLKN Timing Waveforms with *DUAL* = 1

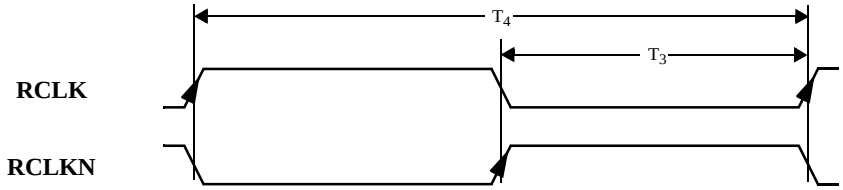


Table 14: General Receive AC Characteristics

Parameters	*Description*	*Min.*	*Max.*	*Units*	*Conditions*
T_3	Delay between rising edge of RCLK to rising edge of RCLKN	10 x T_{RX} -500	10 x T_{RX} +500	ps	T_{RX} is the bit period of the incoming data on Rx.
DT_3	RCLK to RCLKN skew $Delay = \frac{10}{f_{baud}} \pm \Delta T_3$	-500	500	ps	Deviation of RCLK rising edge to RCLKN rising edge. Nominal delay is 10-bit times.
T_4	Period of RCLK and RCLKN	0.49 x T_{REFCLK}	0.51 x T_{REFCLK}	ps	Whether or not locked to serial data, independent of DUAL input.
DT_4	Deviation of RCLK/RCLKN period from REFCLK period $T_{RCLK} = T_{REFCLK} \pm \Delta T_4$	-1.0	1.0	%	Whether or not locked to serial data, independent of DUAL input.
T_R, T_F	Output rise and fall time	—	2.4	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$ into 10pF load
R_{LAT}	Latency from RX0 to REFCLK or RCLK	70.5bc-1.6ns 48.5bc-1.6ns	81.5bc+4.1ns 102.5bc+4.1ns	bc+ns	ENDEC=1, recenter only ENDEC=X, recenter + drift
T_{LOCK}(1)	Data acquisition lock time	—	2500	bc	8B/10B IDLE pattern, Tested on a sample basis.
T_{JTD}	Receive data Total Jitter Tolerance (p-p)	—	600	ps	IEEE 802.3z Clause 38.68, tested on a sample basis.
D_{JTD}	Receive data Deterministic Jitter Tolerance (p-p)	—	370	ps	IEEE 802.3z Clause 38.69, tested on a sample basis.

NOTE: (1) The probability of correct data acquisition and recovery is 95% per FC-PH 4.3 Section 5.3.

Figure 20: REFCLK Timing Waveforms

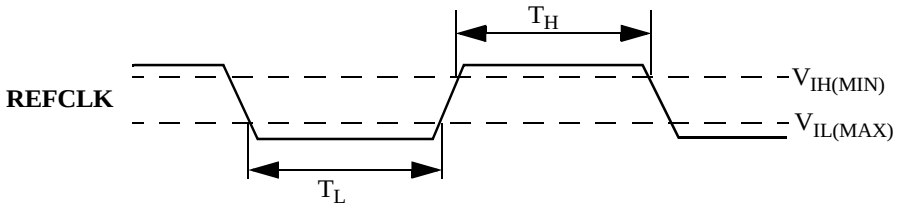
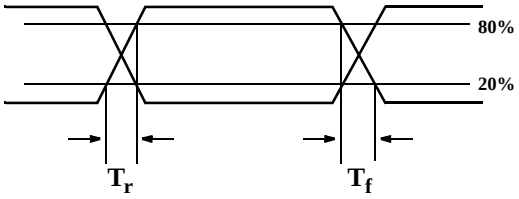


Table 15: Reference Clock Requirements

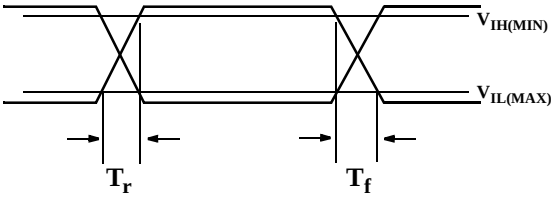
Parameters	*Description*	*Min*	*Max*	*Units*	*Conditions*
FR	Frequency range	98	136	MHz	DUAL = 0
		49	68	MHz	DUAL = 1
FO	Frequency offset	-200	200	ppm	| REFCLK (Tx) - REFCLK (Rx) | = max offset between Tx and Rx device REFCLKs on one serial link
DC	REFCLK duty cycle	35	65	%	Measured at 1.4V
T_H,T_L	REFLCK and TBC pulse width	3	—	ns	
T_{RCR},T_{RCF}	REFCLK rise and fall time	—	1.5	ns	Between $V_{IL(MAX)}$ and $V_{IH(MIN)}$
REFCLK Jitter	REFCLK Jitter Power $\int_{100Hz}^{3MHz} PhaseNoise$	—	100	ps	RMS for 10^{-12} Bit Error Ratio with zero length external path, tested on a sample basis

Figure 21: Parametric Measurement Information

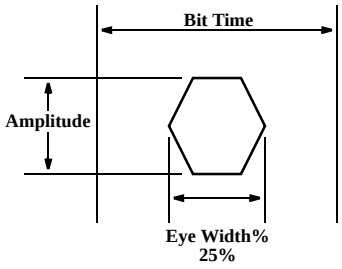
Serial Input Rise and Fall Time



TTL Input and Output Rise and Fall Time

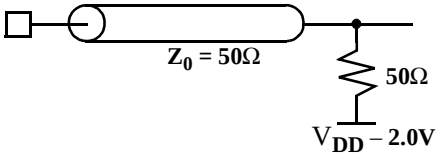


Receiver Input Eye Diagram Jitter Tolerance Mask

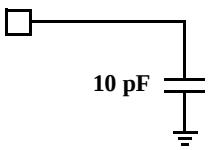


Parametric Test Load Circuit

Serial Output Load



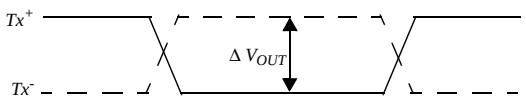
TTL A.C. Output Load



DC Characteristics

Parameters	*Description*	*Min.*	*Typ*	*Max*	*Units*	*Conditions*
TTL Outputs (R(7:0), KCH, IDLE, ERR, RCLK/RCLKN, TBERR, PSDET, RSDET, WSO, REFOUT)						
V_{OH}	TTL output HIGH voltage	2.4	—	—	V	I_{OH} = -1.0mA
V_{OL}	TTL output LOW voltage	—	—	0.5	V	I_{OL} = +1.0mA
I_{OZ}	TTL output leakage current	—	—	50	µA	When set to high-impedance state through JTAG.
TTL Inputs (TBC, T(7:0), C/D, WSEN, KCHAR, BIST, LBEN(1:0), TMODE(2:0), RMODE(1:0), DUAL, PTXEN, RTXEN, RXP/R, RESETN, ENDEC, WSI, FLOCK, TRSTN, TDI, TDO, TMS, TCK)						
V_{IH}	TTL input HIGH voltage	2.0	—	—	V	
V_{IL}	TTL input LOW voltage	0	—	0.8	V	
I_{IH}	TTL input HIGH current	—	50	500	µA	V_{IN} =2.4V
I_{IL}	TTL input LOW current	—	—	-1000	µA	V_{IN} =0.5V
PECL Inputs (REFCLKP/REFCLKN)						
V_{IH}	PECL input HIGH voltage	V_{DD} - 1.1	—	V_{DD} - 0.7	V	
V_{IL}	PECL input LOW voltage	V_{DD} - 2.0	—	V_{DD} - 1.5	V	
I_{IH}	PECL input HIGH current	—	—	200	µA	V_{IN} =$V_{IH(MAX)}$
I_{IL}	PECL input LOW current	- 50	—	—	µA	V_{IN} =$V_{IL(MIN)}$
ΔV_{IN}	PECL input differential peak-to-peak voltage swing	200	—	—	mV	$\lvert V_{IH(MIN)} - V_{IL(MAX)} \rvert$[a]
V_{CM}	PECL input common-mode voltage	V_{DD} - 1.5	—	V_{DD} - 0.7	V	
V_{BIAS}	REFCLKP/REFCLKN internal input bias voltage	—	V_{DD}/ 2	—		
PECL Outputs (PTX+/-, RTX+/-)						
ΔV_{OUT}	PECL differential peak-to-peak output voltage swing	500	—	1100	mV	| PTX+ - PTX- | 50Ω to V_{DD} - 2.0V
PECL Inputs (PRX+/-, RRX+/-)						
ΔV_{IN}	PECL differential peak-to-peak input voltage swing	200	—	1300	mV	| PRX+ - PRX- |
Miscellaneous						
V_{DD}	Power supply voltage	3.14	—	3.47	V	3.3V ± 5%
P_D	Power dissipation	—	0.65	1.2	W	Maximum at 3.47V, at 1.3Gb.s, typical at 3.3V, outputs open, RTX disabled.
I_{DD}	Supply current	—	200	345	mA	

a. Single-ended measurement results are quoted here. Differential techniques used in Fibre Channel would yield values that are twice the magnitude. See diagram below.



Absolute Maximum Ratings (1)

Power Supply Voltage (any V_{DDX}) ..... 0.5V to +3.8V
PECL Differential Input Voltage ..... -0.5V to V_{DD} +0.5V
TTL Input Voltage ..... -0.5V to 5.5V
TTL Output Voltage ..... -0.5V to V_{DD} + 0.5V
TTL Output Current 50mA
PECL Output Current 50mA
Case Temperature Under Bias (T_C) ..... -55°C to +125°C
Storage Temperature (T_{STG}) ..... -65°C to +150°C

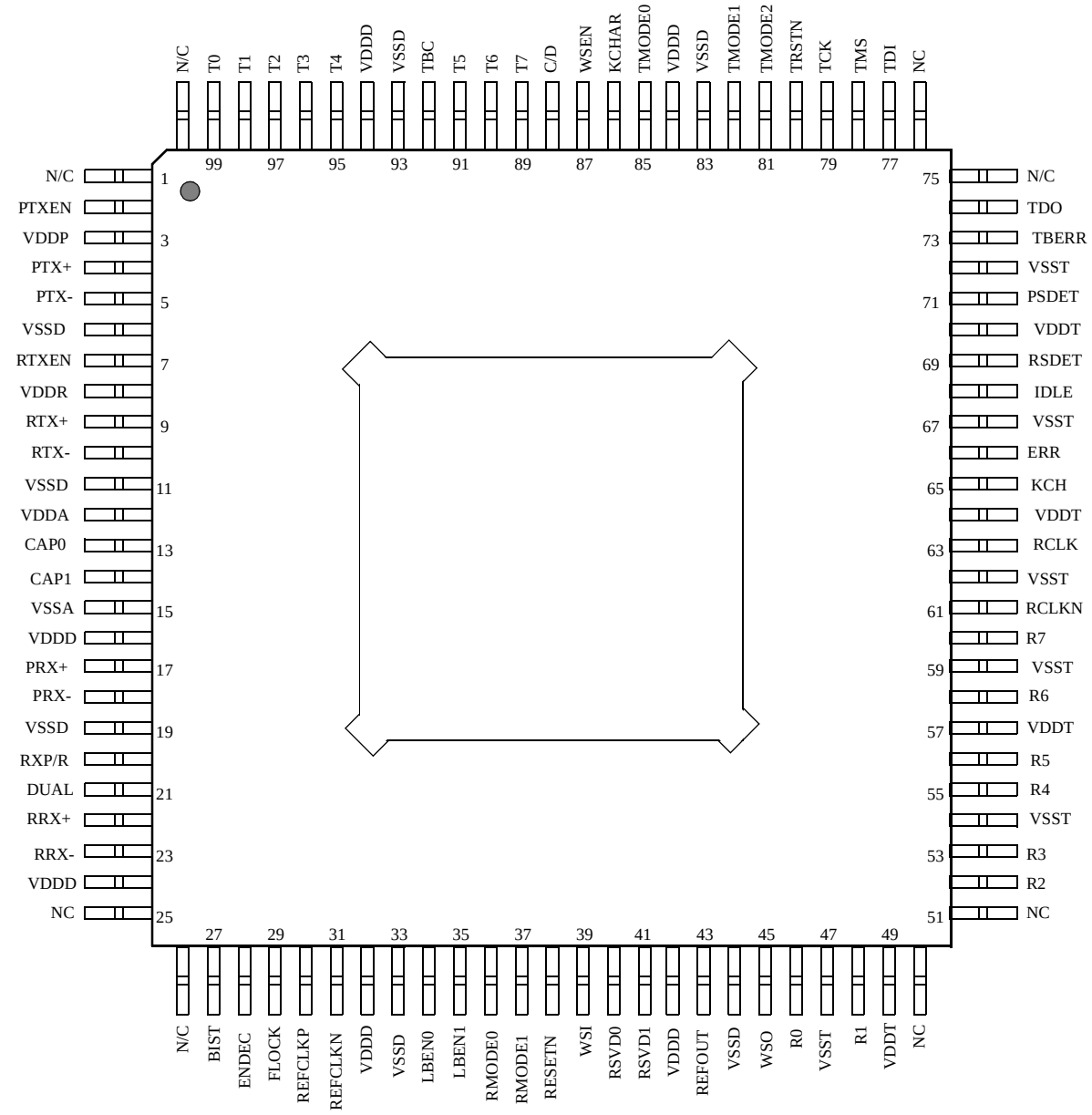
Recommended Operating Conditions

Power Supply Voltage, (V_{DD}) ..... +3.3V±5%
Operating Temperature Range ..... 0°C Ambient to +100°C Case

NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Package Pin Descriptions

Figure 22: Pin Diagram



(Top View)

Table 16: Pin Identification

Pin	*Name*	*I/O*	*Type*	*Pin Description*
99,98,97 96,95,91 90,89	T0, T1, T2 T3, T4, T5 T6, T7	I	TTL	**T**ransmit data, synchronous to REFCLK or TBC.
88	C/D	I	TTL	**C**ontrol/**D**ata. If KCHAR=C/D=LOW, then T(7:0) is used to generate transmit data. If KCHAR=C/D=HIGH then special Kxx.x characters are transmitted based upon the value of T(7:0). If KCHAR=LOW and C/D =HIGH, IDLE characters are transmitted. When ENDEC=LOW, this is equivalent to data bit T8.
87	WSEN	I	TTL	**W**ord **S**ync **EN**able. Asserted HIGH for one cycle to initiate transmission of the Word Sync Sequence as defined in Figure 5 and related text. When ENDEC=LOW, this is equivalent to data bit T9.
92	TBC	I	TTL	**T**ransmit **B**yte **C**lock. Optional input data timing reference for T(7:0), WSEN and C/D.
86	KCHAR	I	TTL	Special **K**xx.x **CHAR**acter Enable. When C/D is HIGH, KCHAR controls data sent to the transmitter. When LOW, IDLE characters are sent. When HIGH, Kxx.x special characters are sent as encoded on T(7:0). This is intended to be a static input and cannot be changed on a cycle-by-cycle basis. When ENDEC=LOW, this is equivalent to ENCDET. A HIGH enables comma detection and alignment. A LOW disables both.
85 82 81	TMODE0 TMODE1 TMODE2	I	TTL	**T**ransmit Input Data Timing **MODE**. Determines the timing reference for T(7:0), WSEN and C/D as defined in Table 1.
73	TBERR	O	TTL	**T**ransmit **B**uffer **ERR**or. When HIGH indicates that the elastic limit of the transmit input skew buffer was exceeded, output timing is same as R(7:0). A LOW indicates correct reception of the 256-byte incrementing pattern in BIST mode.
4 5	PTX+ PTX-	O	PECL	**P**rimary Differential Serial **TX** Output. These pins output serialized transmit data when PTXEN is HIGH. AC-coupling is recommended.
9 10	RTX+ RTX-	O	PECL	**R**edundant Differential Serial **TX** output. These pins output serialized transmit data when RTXEN is HIGH. AC-coupling is recommended.
2	PTXEN	I	TTL	**P**rimary **TX** Output **EN**able. When HIGH, PTX+/- is active, when LOW PTX+/- is powered down and the outputs are un-driven.
7	RTXEN	I	TTL	**R**edundant **TX** Output **EN**able. When HIGH RTX+/- is active, when LOW RTX+/- is powered down and the outputs are un-driven.
46,48,52 53,55,56 58,60	R0, R1, R2 R3, R4, R5 R6, R7	O	TTL	**R**eceive Data. Synchronous to RCLK/RCLKN or REFCLK as selected by RMODE(1:0).
68	IDLE	O	TTL	**IDLE** Detect. When HIGH, an IDLE character has been detected by the decoder and is on R(7:0) When ENDEC=LOW, this is equivalent to COMDET.
65	KCH	O	TTL	**K**xx.x **CH**aracter Detect. When HIGH, a special Kxx.x character has been detected by the decoder and is on R(7:0). When ENDEC=LOW, this is equivalent to data bit R8.

Pin	*Name*	*I/O*	*Type*	*Pin Description*
66	ERR	O	TTL	**ERR**or Detect. When HIGH, an invalid 10-bit character or disparity error has been detected and the data on R(7:0) is invalid. When ENDEC=LOW, this is equivalent to data bit R9.
63 61	RCLK RCLKN	O	TTL	**R**ecovered **CL**oc**K** Outputs. These outputs are driven from the recovered clock, at 1/10 or 1/20 the baud rate, as selected by RMODE(1:0) and DUAL. When unused, RCLK is HIGH and RCLKN is LOW.
36 37	RMODE0 RMODE1	I	TTL	**R**eceive Output Data Timing **MODE**. Determines the timing reference for R(7:0), IDLE, KCH, ERR, PSDET, RSDET and TBERR, as defined in Table 5.
17 18	PRX+ PRX-	I	PECL	**P**rimary Differential Serial **RX** Inputs. These pins receive the serialized input data when LBEN(1) is LOW and RXP/R is HIGH, otherwise they are unused. They are internally biased at $V_{DD}/2$ through a 3.2KW resistor to the bias voltage. AC coupling is recommended.
22 23	RRX+ RRX-	I	PECL	**R**edundant Differential Serial **RX** Inputs. These pins receive the serialized input data when LBEN(1) is LOW and RXP/R is LOW, otherwise they are unused. They are internally biased at $V_{DD}/2$ through a 3.2KW resistor to the bias voltage. AC coupling is recommended.
34 35	LBEN0 LBEN1	I	TTL	**L**oop **B**ack **EN**able. These inputs control serial or parallel loopback configuration as described in Table 8.
20	RXP/R	I	TTL	**RX** Input **P**rimary/**R**edundant serial input select. When LBEN(1) is LOW, this input selects PRX+/- as the serial input source when HIGH and RRX+/- as the serial input source when LOW.
71	PSDET	O	TTL	**P**rimary Analog **S**ignal **DET**ect. This output goes HIGH when the amplitude on PRX is greater than 200mV and LOW when the input is less than 100mV. PSDET is not defined when the input is between 100mV and 200mV. Output timing is same as R(7:0).
69	RSDET	O	TTL	**R**edundant Analog **S**ignal **DET**ect. This output goes HIGH when the amplitude on RRX is greater than 200mV, LOW when the input is less than 100 mV. RSDET is not defined when the input is between 100mV and 200mV. Output timing is same as R(7:0).
30 31	REFCLKP REFCLKN	I	PECL	**REFCLK** Differential **P**ositive and **N**egative PECL or Single-Ended TTL Inputs. This rising edge of this clock latches transmit data and control into the input register. It also provides the reference clock, at 1/10th or 1/20th of the baud rate to the PLL as selected by DUAL. If TTL, connect to REFCLKP but leave REFCLKN open. If PECL, connect both REFCLKP and REFCLKN.
43	REFOUT	O	TTL	**REF**erence Clock **OUT**put: This is an output from the clock synthesizer at the baud rate divided by ten.
13 14	CAP0 CAP1	A	Analog	Loop Filter **CAP**acitor for Clock Generation PLL. Nominally 0.1 µF, amplitude is less than 3V. See the Loop Filter Applications section for more details.
21	DUAL	I	TTL	**DUAL** Clock Mode. When LOW, REFCLK and RCLK/RCLKN are 1/10th the baud rate. When HIGH, they are 1/20th the baud rate.

Pin	*Name*	*I/O*	*Type*	*Pin Description*
29	FLOCK	I	TTL	**F**requency **LOCK**ed Mode. When HIGH indicates that the transmitting device's REFCLK is frequency-locked to the receiver's word clock. Controls rate matching (IDLE delete/duplicate) logic along with the WSI input as defined in Table 6.
27	BIST	I	TTL	**B**uilt-**I**n **S**elf **T**est Mode. When HIGH, the transmitter continuously sends a 256 byte incrementing data pattern, and the receiver signals correct reception of the test pattern with a LOW on TBERR.
28	ENDEC	I	TTL	**EN**coder/**DEC**oder Enable. When HIGH the VSC7212 is configured for 8 bit operation, internal 8B/10B encoding is enabled. When LOW, a 10-bit interface is used and internal 8B/10B encoding is bypassed.
38	RESETN	I	TTL	**RESETN** Input. When asserted LOW, the transmitter input skew buffer and receiver elastic buffer are recentered.
39	WSI	I	TTL	**W**ord **S**ync **I**nput. Used to control chip-to-chip alignment and IDLE character insertion/deletion as defined in Table 6.
45	WSO	O	TTL	**W**ord **S**ync **O**utput. Used to set initial chip-to-chip word alignment, and to maintain alignment by controlling IDLE character insertion/deletion.
79	TCK	I	TTL	JTAG Test Access Port Test Clock Input
78	TMS	I	TTL	JTAG Test Access Port Test Mode Select Input
77	TDI	I	TTL	JTAG Test Access Port Test Data Input
74	TDO	O	TTL	JTAG Test Access Port Test Data Output
80	TRSTN	I	TTL	JTAG Test Access Port Test Logic Reset Input
40 41	RSVD0 RSVD1	I	N/A	Reserved Inputs for future use. Set HIGH for compatibility reasons.
12	VDDA	P	VDD	Analog power supply to PLL.
15	VSSA	P	GND	Analog ground to PLL.
16,24,32 42,84,94	VDDD	P	VDD	Digital power supply.
6,11,19,33 44,83,93	VSSD	P	GND	Digital ground.
49,57,64 70	VDDT	P	VDD	TTL output power supply.
47,54,59 62,67,72	VSST	P	GND	TTL output ground.
3 8	VDDP VDDR	P	VDD	PECL Output power supply for PTX. PECL Output power supply for RTX. If use of an output is not necessary, leave the power supply pin open.
1,25,26 50,51,75 76,100	N/C			Not connected internally.

Package Thermal Considerations

The VSC7212 is packaged in a 100-pin, 14x14x1.0mm, cavity-down, thermally-enhanced TQFP. This package uses an industry-standard EIAJ footprint but has been enhanced to improve thermal dissipation. The construction of the package is shown in Figure 23.

Figure 23: TQFP Package Cross Section

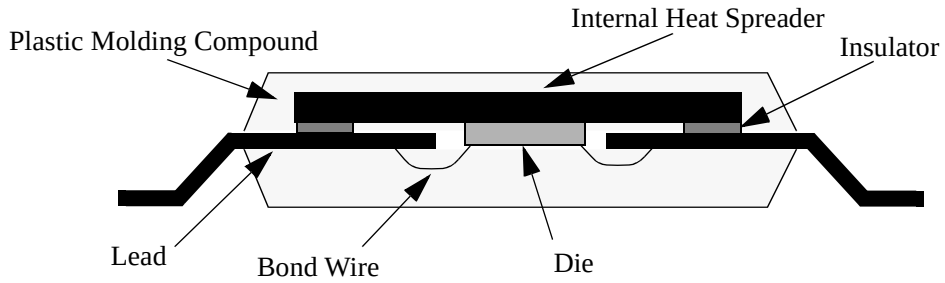


Table 17: Thermal Resistance

Symbol	*Description*	*TQFP*	*Units*
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads.	39.9	^{o}C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient with 100 LFM airflow	37.1	^{o}C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient with 200 LFM airflow	35.3	^{o}C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient with 400 LFM airflow	33.5	^{o}C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient with 600 LFM airflow	31.7	^{o}C/W

The VSC7212 is designed to operate with a case temperature up to 100^{o}C. The user must guarantee that the case temperature specification is not violated. With the thermal resistances shown above, the 14mm thermally-enhanced PQFP can operate in still air ambient temperatures of 52.1^{o}C [52.1^{o}C = 100^{o}C - 1.0W * 39.9]. If the ambient air temperature exceeds these limits then some form of cooling through a heatsink or an increase in airflow must be provided.

Moisture Sensitivity Level

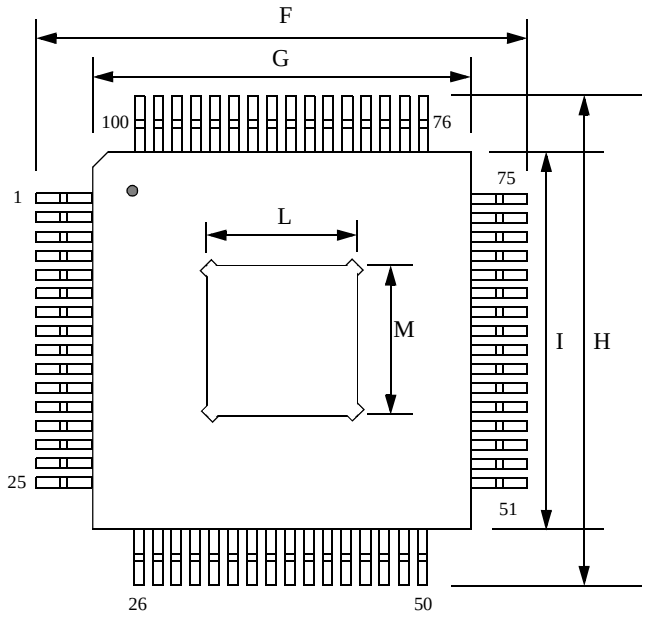
This device is rated at a Moisture Sensitivity Level 3 rating with maximum floor life of 168 hours at 30ºC, 60% relative humidity. Please refer to Application Note AN-20 for appropriate handling procedures.

Preliminary Data Sheet

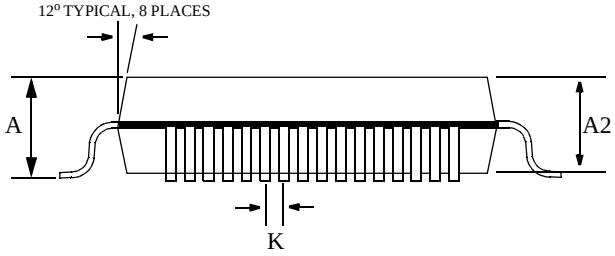
VSC7212

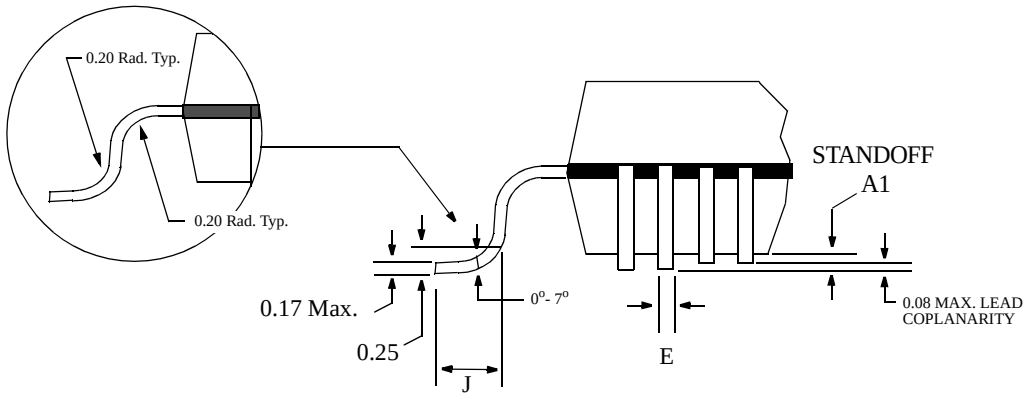
Gigabit Interconnect Chip

Package Information: 100-pin TQFP



Item	*10 mm*	*Tolerance*
A	1.20	MAX
A1	0.10	±0.05
A2	1.00	±0.05
E	0.22	±0.05
F	16.00	BASIC
G	14.00	BASIC
H	16.00	BASIC
I	14.00	BASIC
J	0.60	+0.15/-0.15
K	0.50	BASIC
L	4.0	BASIC
M	4.0	BASIC



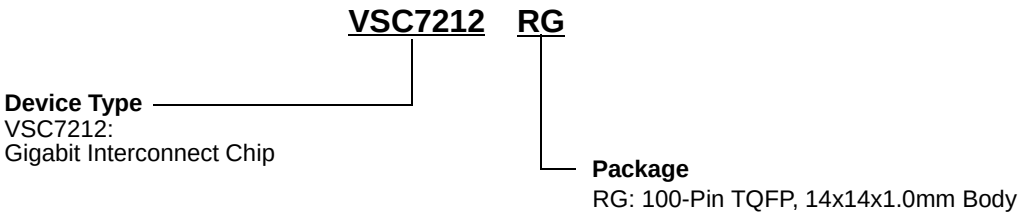


NOTES:
Drawing not to scale.

All units in mm unless otherwise noted.
Drawing does not show correct number of pins

Ordering Information

The part number for this product is formed by a combination of the device type and the package style:



Marking Information

The package is marked with three lines of text as in Figure 24:

Figure 24: Package Marking Information