VITESSE
SEMICONDUCTOR CORPORATION

Data Sheet

VSC8116

ATM/SONET/SDH 622/155Mb/s Transceiver Mux/Demux with Integrated Clock Generation

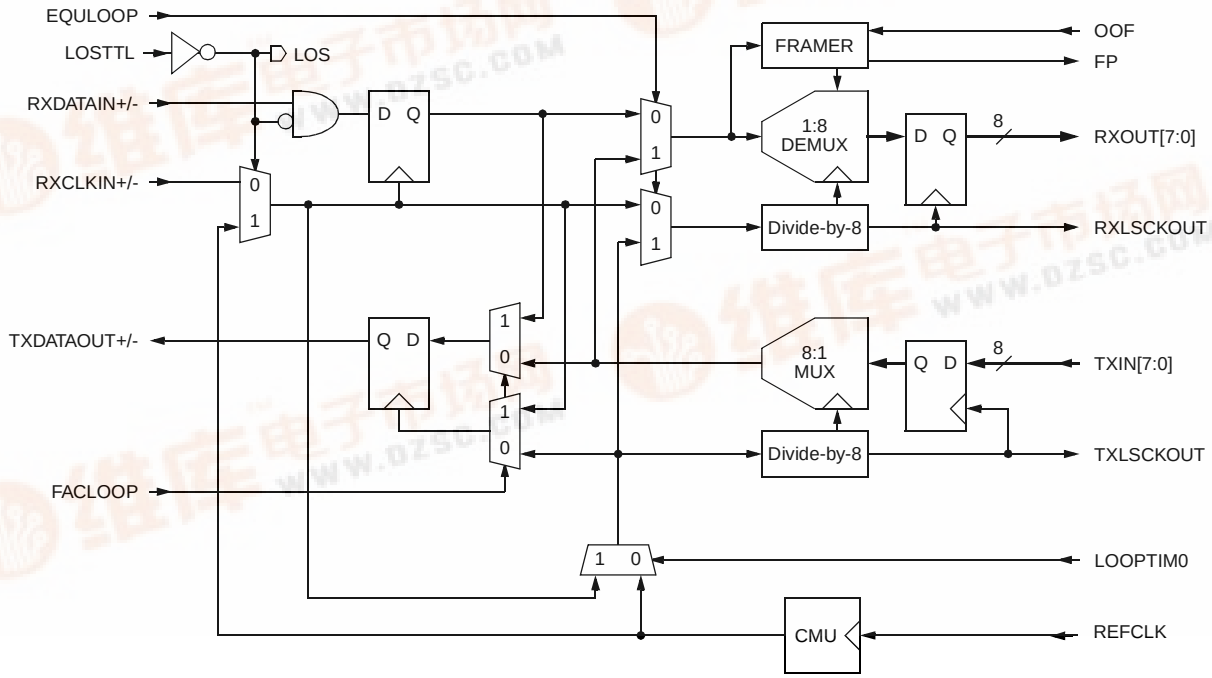
Features

- Operates at Either STS-3/STM-1 (155.52 Mb/s) or STS-12/STM-4 (622.08 Mb/s) Data Rates
- Compatible with Industry ATM UNI Devices
- On Chip Clock Generation of the 155.52 Mhz or 622.08 Mhz High Speed Clock
- Dual 8 Bit Parallel TTL Interface
- SONET/SDH Frame Detection and Recovery
- Loss of Signal (LOS) Control
- Provides Equipment, Facilities and Split Loop-back Modes as well as Loop Timing Mode
- Meets Bellcore, ITU and ANSI Specifications for Jitter Performance
- Single 3.3V Supply Voltage
- Low Power - 1.2 Watts Maximum
- 64 PQFP Package

General Description

The VSC8116 is an ATM/SONET/SDH compatible transceiver integrating an on-chip clock multiplication unit (PLL) for the high speed clock and 8 bit serial-to-parallel and parallel-to-serial data conversion. The high speed clock generated by the on-chip PLL is selectable for 155.52 or 622.08 MHz operation. The demultiplexer contains SONET/SDH frame detection and recovery. In addition, the device provides both facility and equipment loopback modes and loop timing modes. The part is packaged in a 64 PQFP with an integrated heat spreader for optimum thermal performance and reduced cost. The VSC8116 provides an integrated solution for ATM physical layers and SONET/SDH systems applications.

VSC8116 Block Diagram



Functional Description

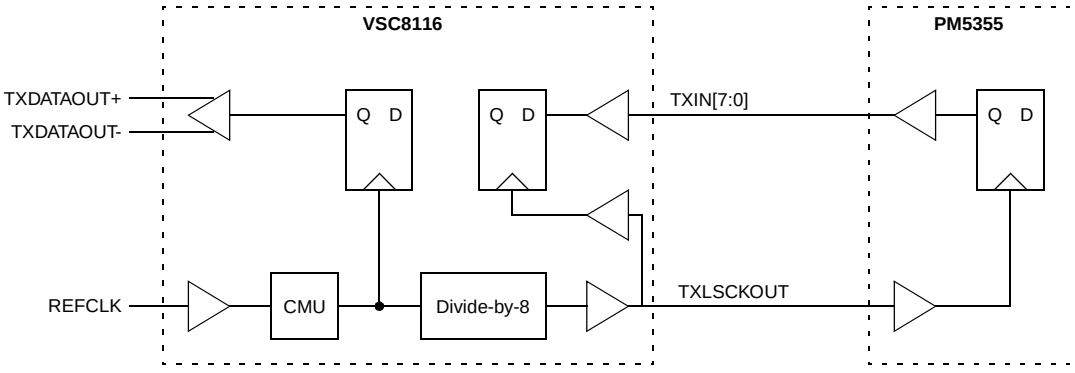
The VSC8116 is designed to provide a SONET/SDH compliant interface between the high speed optical networks and the lower speed User Network Interface (UNI) devices such as the PM5355 S/UNI-622 (or PM5312 STTX). The VSC8116 transmit section converts 8 bit parallel data at 77.76 Mb/s or 19.44 Mb/s to a serial bit stream at 622.08 Mb/s or 155.52 Mb/s, respectively. It also provides a Facility Loopback function which loops the received high speed data and clock directly to the transmit outputs. A Clock Multiplier Unit (CMU) is integrated into the transmit circuit to generate the high speed clock for the serial output data stream from input references frequency of 19.44 or 77.76 MHz. The CMU can be bypassed by using the receive clock in loop timing mode thus synchronizing the entire part to a single clock (RXCLKIN).

The receive section provides the serial-to-parallel conversion, converting 155 Mb/s or 622 Mb/s to an 8 bit parallel output at 19.44 Mb/s or 77.76 Mb/s, respectively. The receive section provides an Equipment Loopback function which will loop the low speed transmit data and clock back through the receive section to the 8 bit parallel data bus and clock outputs. The receive section also contains a SONET/SDH frame detector circuit which is used to provide frame recovery in the serial to parallel converter. The block diagram on page 1 shows the major functional blocks associated with the VSC8116.

Transmit Section

Byte-wide data is presented to TXIN [7:0] and is clocked into the part on the rising edge of TXLSCKOUT (refer to Figure 1). The data is then serialized (MSB leading) and presented at the TXDATAOUT+/- pins. The serial output stream is synchronized to the CMU generated clock which is a phase locked and frequency scaled version of the input reference clock. External control inputs CMUFREQSEL and STS12 select the multiply ratio of the CMU and either STS-3 (155 Mb/s) or STS-12 (622 Mb/s) transmission (See Table 2).

Figure 1: Data and Clock Transmit Block Diagram

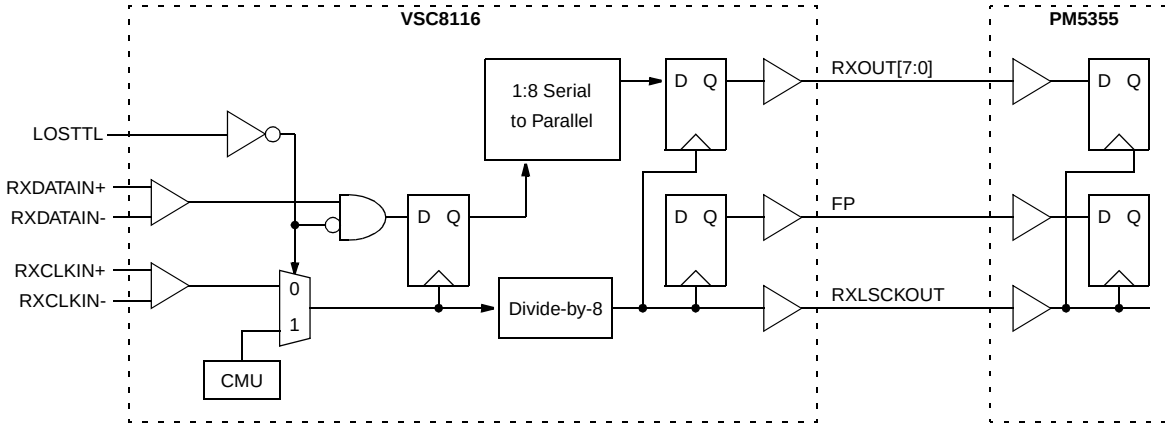


Receive Section

High speed Non-Return to Zero (NRZ) serial data at 155Mb/s or 622Mb/s are received by the RXDATAIN inputs. The corresponding clock is received by the RXCLKIN inputs. RXDATAIN is clocked in on the rising edge of RXCLKIN+. See Figure 2. The serial data is converted to byte-wide parallel data and presented on RXOUT[7:0] pins. A divide-by-8 version of the high-speed clock (RXLSCKOUT) should be used to synchronize the byte-serial RXOUT[7:0] data with the receive portion of the UNI device.

The receive section also includes frame detection and recovery circuitry which detects the SONET/SDH frame, aligns the received serial data on byte boundaries, and initiates a frame pulse on FP coincident with the byte aligned data. The frame recovery is initiated when OOF is held high which must occur at least 4 byte clock cycles before the A1A2 boundary. The OOF input control is a level-sensitive signal, and the VSC8116 will continually perform frame detection and recovery as long as this pin is held high even if 1 or more frames has been detected. Frame detection and recovery occurs when a series of three A1 bytes followed by three A2 bytes has been detected. The parallel output data on RXOUT[7:0] will be byte aligned starting on the third A2 byte. When a frame is detected, a single byte clock period long pulse is generated on FP which is synchronized with the byte-aligned third A2 byte on RXOUT[7:0]. The frame detector sends an FP pulse only if OOF is high or if a frame was detected while OOF was being pulled low.

Figure 2: Data and Clock Receive Block Diagram



Loss of Signal

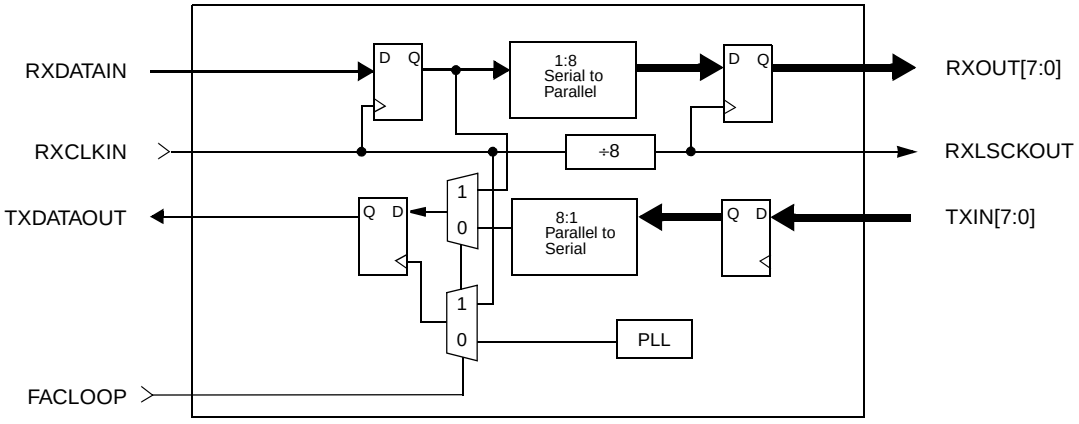
During a LOS condition, the VSC8116 forces the receive data low which is an indication for any downstream equipment that an optical interface failure has occurred. The receive section is clocked by the transmit section's

PLL clock multiplier. Optics have either a PECL or TTL output, usually called “SD” (Signal Detect) or “FLAG” indicating either a lack of or presence of optical power. Depending on the optics manufacture this signal is either active high or active low polarity. If the optics Signal Detect or FLAG output is a “TTL” signal, it should be connected to LOSTTL. If it’s a “PECL” signal it should be connected through a “PECL” to “TTL” translator (such as the Motorola “MC100ELT21”) which then drives LOSTTL. The follow on part to VSC8116 is the VSC8117, in this device the signal LOSTTL has been changed to LOSPECL, a PECL input.

Facility Loopback

The Facility Loopback function is controlled by the FACLOOP signal. When the FACLOOP signal is set high, the Facility Loopback mode is activated and the high speed serial receive data (RXDATAIN) is presented at the high speed transmit output (TXDATAOUT). See Figure 3. In Facility Loopback mode the high speed receive data (RXDATAIN) is also converted to parallel data and presented at the low speed receive data output pins (RXOUT [7:0]). The receive clock (RXCLKIN) is also divided down and presented at the low speed clock output (RXLSCKOUT).

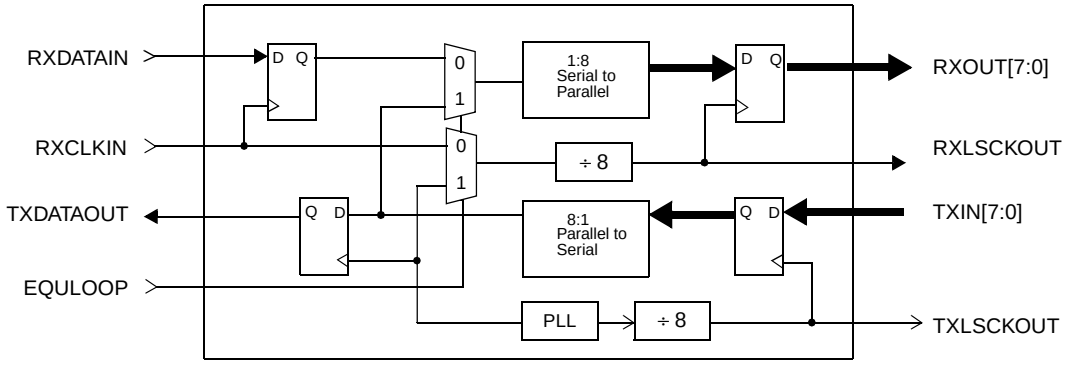
Figure 3: Facility Loopback Data Path



Equipment Loopback

The Equipment Loopback function is controlled by the EQULOOP signal. When the EQULOOP signal is set high, the Equipment Loopback mode is activated and the high speed transmit data generated from the parallel to serial conversion of the low speed data (TXIN [7:0]) is selected and converted back to parallel data in the receiver section and presented at the low speed parallel outputs (RXOUT [7:0]). See Figure 4. The internally generated 155MHz/622MHz clock is used to generate the low speed receive clock output (RXLSCKOUT). In Equipment Loopback mode the transmit data (TXIN [7:0]) is serialized and presented at the high speed output (TXDATAOUT).

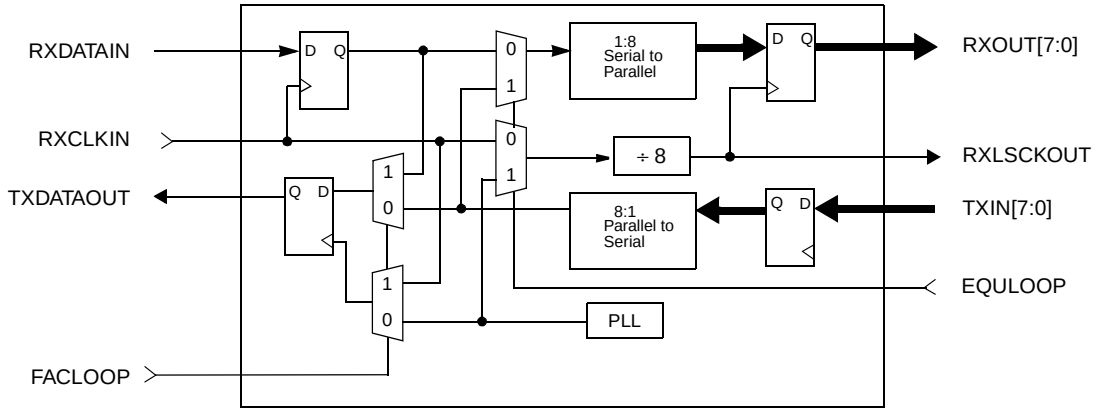
Figure 4: Equipment Loopback Data Path



Split Loopback

Equipment and facility loopback modes can be enabled simultaneously. See descriptions for equipment and facility loop modes above. The only change is, since they are both active, RXDATAIN will not be deserialized and presented to RXOUT[0:7], and TXIN[0:7] will not be serialized and present to TXDATAOUT.

Figure 5: Split Loopback Datapath



Loop Timing

LOOPTIM0 mode bypasses the CMU when the LOOPTIM0 input is asserted high. In this mode the CMU is bypassed by using the receive clock (RXCLKIN), and the entire part is synchronously clocked from a single external source.

Clock Multiplier Unit

The VSC8116 uses an integrated phase-locked loop (PLL) for clock synthesis of the 622MHz high speed clock used for serialization in the transmitter section. The PLL is comprised of a phase-frequency detector (PFD), an integrating operation amplifier and a voltage controlled oscillator (VCO) configured in classic feedback system. The PFD compares the selected divided down version of the 622MHz VCO (CMUFREQSEL selects divide-by ratios of 8 or 32, see Table 2) and the reference clock. The integrator provides a transfer function between input phase error and output voltage control. The VCO portion of the PLL is a voltage controlled ring-oscillator with a center frequency of 622MHz.

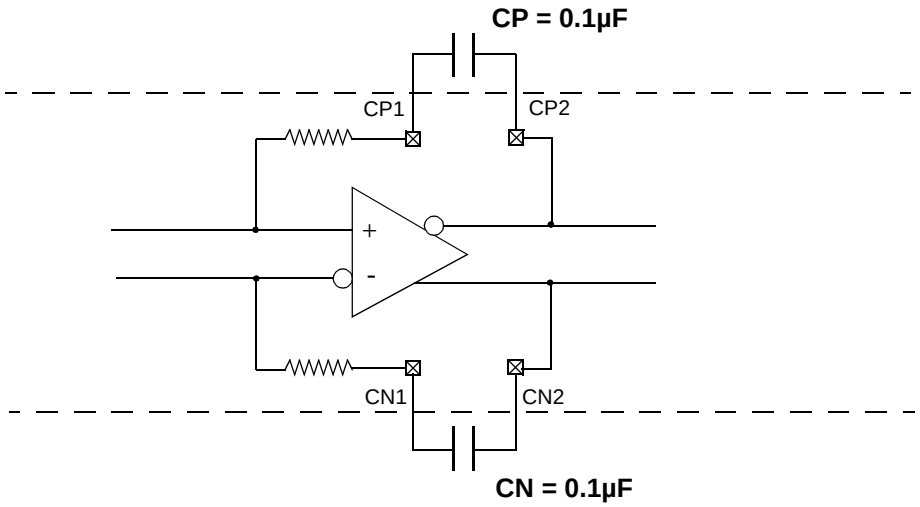
The reactive elements of the integrator are located off-chip and are connected to the feedback loop of the amplifier through the CP1, CP2, CN1 and CN2 pins. The configuration of these external surface mounted capacitors is shown in Figure 6. Table 1 shows the recommended external capacitor values for the configurable reference frequencies.

Good analog design practices should be applied to the board design for these external components. Tightly controlled analog ground and power planes should be provided for the PLL portion of the circuitry. The dedicated PLL power (VDDA) and ground (VSSA) pins should have quiet supply planes to minimize jitter generation within the clock synthesis unit. This is accomplished by either using a ferrite bead or a C-L-C choke (π filter) on the (VDDA) power pins. Note: Vitesse recommends a (π filter) C-L-C choke over using a ferrite bead. All ground planes should be tied together using multiple vias.

Table 1: Recommended External Capacitor Values

Reference Frequency [MHz]	*Divide Ratio*	*CP*	*CN*	*Type*	*Size*	*Tol.*
19.44	32	0.1	0.1	X7R	0603/0805	+/-10%
77.76	8	0.1	0.1	X7R	0603/0805	+/-10%

Figure 6: External Integrator Capacitor



Clock Multiplier Unit

Table 2: Reference Frequency Selection and Output Frequency Control

STS12	*CMUFREQSEL*	*Reference Frequency [MHz]*	*Output Frequency [MHz]*
1	1	19.44	622.08
1	0	77.76	622.08
0	1	19.44	155.52
0	0	77.76	155.52

Table 3: Clock Multiplier Unit Performance

Name	*Description*	*Min*	*Typ*	*Max*	*Units*
RCd	Reference clock duty cycle	40		60	%
RCj	Reference clock jitter (RMS) @ 77.76 MHz ref (1)			13	ps
RCj	Reference clock jitter (RMS) @ 19.44 MHz ref (1)			5	ps
RC_f	Reference clock frequency tolerance (2)	-20		+20	ppm
OCj	Output clock jitter (RMS) @ 77.76 MHz ref (3)			8	ps
OCj	Output clock jitter (RMS) @ 19.44 MHz ref (3)			15	ps
OCfrange	Output frequency	620		624	MHz
OCd	Output clock duty cycle	40		60	%

(1) These Reference Clock Jitter limits are required for the outputs to meet SONET system level jitter requirements (< 10 mUIrms)
(2) Needed to meet SONET output frequency stability requirements
(3) Measured

Note: Jitter specification is defined utilizing a 12KHz - 5MHz LP-HP single pole filter.

AC Timing Characteristics

Figure 7: Receive High Speed Data Input Timing Diagram

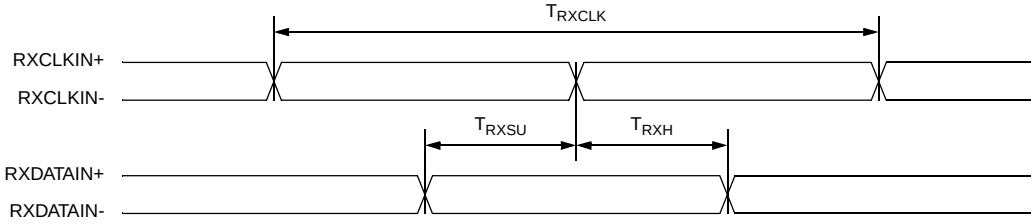


Table 4: Receive High Speed Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	1.608	-	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	250	-	-	ps
T_{RXH}	Serial data hold time with respect to RXCLKIN	250	-	-	ps

Table 5: Receive High Speed Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{RXCLK}	Receive clock period	-	6.43	-	ns
T_{RXSU}	Serial data setup time with respect to RXCLKIN	1.5	-	-	ns
T_{RXH}	Serial data hold time with respect to RXCLKIN	1.5	-	-	ns

Figure 8: Transmit Data Input Timing Diagram

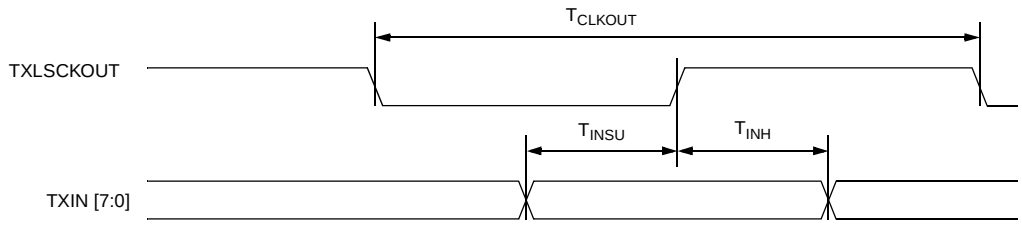


Table 6: Transmit Data Input Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{INSU}	Transmit data setup time with respect to TXLSCKOUT	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKOUT	1.0	-	-	ns

Table 7: Transmit Data Input Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
T_{INSU}	Transmit data setup time with respect to TXLSCKOUT	1.0	-	-	ns
T_{INH}	Transmit data hold time with respect to TXLSCKOUT	1.0	-	-	ns

Note: Duty cycle for TXLSCKOUT is 50% +/- 10% worst case

Figure 9: Receive Data Output Timing Diagram

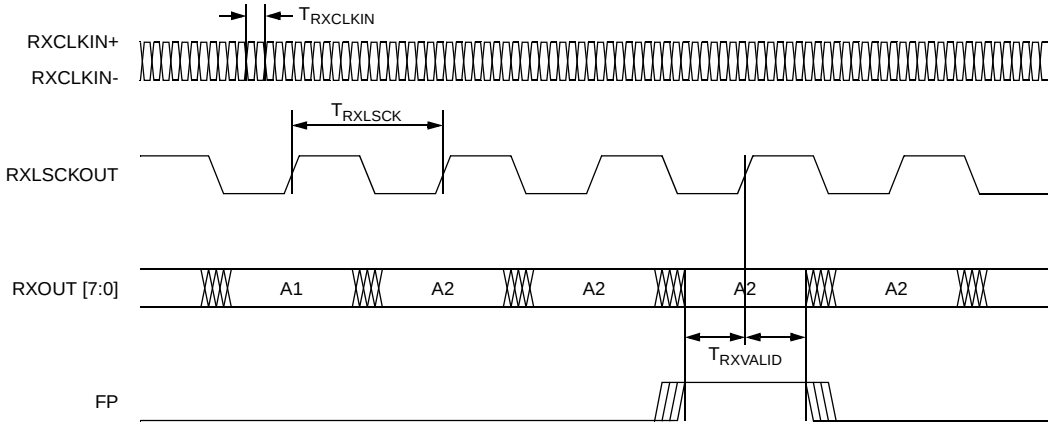


Table 8: Receive Data Output Timing Table *(STS-12 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	1.608	-	ns
T_{RXLSCK}	Receive data output byte clock period	-	12.86	-	ns
$T_{RXVALID}$	Time data on RXOUT [7:0] and FP is valid before and after the rising edge of RXLSCKOUT	4.0	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	12.86	-	ns

Table 9: Receive Data Output Timing Table *(STS-3 Operation)*

Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*
$T_{RXCLKIN}$	Receive clock period	-	6.43	-	ns
$T_{RXLSCKT}$	Receive data output byte clock period	-	51.44	-	ns
$T_{RXVALID}$	Time data on RXOUT [7:0] and FP is valid before and after the rising edge of RXLSCKOUT	22	-	-	ns
T_{PW}	Pulse width of frame detection pulse FP	-	51.44	-	ns

AC Characteristics

Table 10: PECL and TTL Outputs

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
$T_{R,TTL}$	TTL Output Rise Time	—	2	—	ns	10-90%
$T_{F,TTL}$	TTL Output Fall Time	—	1.5	—	ns	10-90%
$T_{R,PECL}$	PECL Output Rise Time	—	350	—	ps	20-80%
$T_{F,PECL}$	PECL Output Fall Time	—	350	—	ps	20-80%

DC Characteristics

Table 11: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (PECL)	—	—	V_{DDP} – 0.9V	V	—
V_{OL}	Output LOW voltage (PECL)	0.7	—	—	V	—
V_{OCM}	O/P Common Mode Range (PECL)	1.1	—	V_{DDP} – 1.3V	V	—
ΔV_{OUT75}	Differential Output Voltage (PECL)	600	—	1300	mV	75Ω to V_{DDP} – 2.0 V
ΔV_{OUT50}	Differential Output Voltage (PECL)	600	—	1300	mV	50Ω to V_{DDP} – 2.0 V
V_{IH}	Input HIGH voltage (PECL)	V_{DDP} – 0.9V	—	V_{DDP} – 0.3V	V	For single ended
V_{IL}	Input LOW voltage (PECL)	0	—	V_{DDP} – 1.72V	V	For single ended
ΔV_{IN}	Differential Input Voltage (PECL)	400	—	1600	mV	—
V_{ICM}	I/P Common Mode Range (PECL)	1.5 – $\Delta V_{IN}/2$	—	V_{DDP} – 1.0 – $\Delta V_{IN}/2$	V	—
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA

Table 11: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH voltage (TTL)	2.0	—	5.5	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	2.0V< V_{IN} < 5.5V, Typical@2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	-0.5V < V_{IN} < 0.8V

Power Dissipation

Table 12: Power Supply Currents (Outputs Open)

Parameter	*Description*	*Typ*	*(Max)*	*Units*
I_{DD}	Power supply current from V_{DD}	231	346	mA
P_D	Power dissipation	0.8	1.2	W

Absolute Maximum Ratings(1)

Power Supply Voltage (V_{DD}) Potential to GND ..... -0.5V to +4V
DC Input Voltage (PECL inputs) ..... -0.5V to V_{DD} +0.5V
DC Input Voltage (TTL inputs) ..... -0.5V to 5.5V
DC Output Voltage (TTL Outputs) ..... -0.5V to V_{DD} + 0.5V
Output Current (TTL Outputs) ..... +/-50mA
Output Current (PECL Outputs) ..... +/-50mA
Case Temperature Under Bias ..... -55^{o} to $+125^{o}$C
Storage Temperature ..... -65^{o}C to $+150^{o}$C
Maximum Input ESD (Human Body Model) ..... 1500 V

Note: Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{DD}) ..... +3.3V ±5 %
Commercial Operating Temperature Range* (*T*) ..... 0^{o} to 70^{o}C
Extended Operating Temperature Range* (*T*) ..... 0^{o} to 115^{o}C
Industrial Operating Temperature Range* (*T*) ..... -40^{o} to 85^{o}C
** Lower limit of specification is ambient temperature and upper limit is case temperature.*

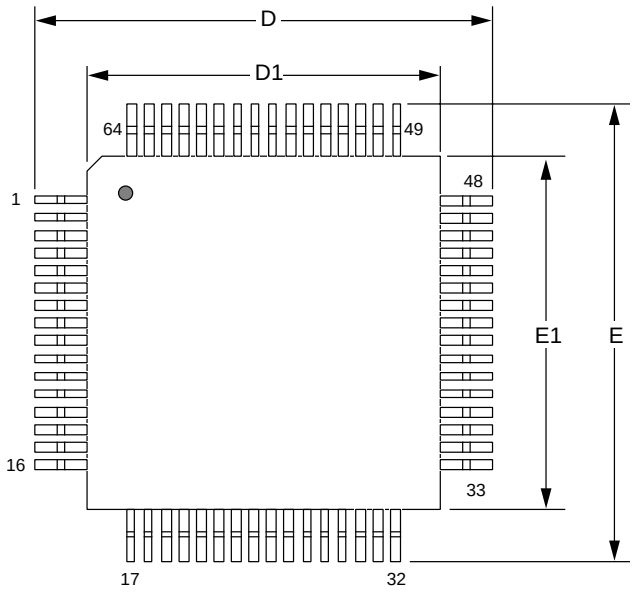
Package Pin Description

Signal	Pin	I/O	Level	Pin Description
RESET	1	I	TTL	Resets frame detection, dividers, controls; active high
LOOPTIM0	2	I	TTL	Enable loop timing operation; active HIGH
CMUFREQSEL	3	I	TTL	Reference clock frequency select, refer to table 2
VDD	4	P	+3.3V	+3.3V Power Supply
TXDATAOUT+	5	O	PECL	Transmit output, high speed differential data +
TXDATAOUT-	6	O	PECL	Transmit output, high speed differential data -
N/C	7	-	-	No connection
RXCLKIN+	8	I	PECL	Receive high speed differential clock input+
RXCLKIN-	9	I	PECL	Receive high speed differential clock input-
VDD	10	P	+3.3V	+3.3V Power Supply
OOF	11	I	TTL	Out Of Frame; Frame detection initiated with high level
N/C	12	-	-	No connection
RXDATAIN+	13	I	PECL	Receive high speed differential data input+
RXDATAIN-	14	I	PECL	Receive high speed differential data input-
VDD	15	P	+3.3V	+3.3V Power Supply
N/C	16	-	-	No connection
N/C	17	-	-	No connection
VDD	18	P	+3.3V	+3.3V Power Supply
RXOUT0	19	O	TTL	Receive output data bit0
RXOUT1	20	O	TTL	Receive output data bit1
VSS	21	P	GND	Ground
RXOUT2	22	O	TTL	Receive output data bit2
RXOUT3	23	O	TTL	Receive output data bit3
RXOUT4	24	O	TTL	Receive output data bit4
RXOUT5	25	O	TTL	Receive output data bit5
RXOUT6	26	O	TTL	Receive output data bit6
RXOUT7	27	O	TTL	Receive output data bit7
VSS	28	P	GND	Ground
RXLSCKOUT	29	O	TTL	Receive byte clock output
FP	30	O	TTL	Frame detection pulse
VDD	31	P	+3.3V	+3.3V Power Supply
N/C	32	-	-	No connection
LOSTTL	33	I	TTL	Loss of Signal Control - TTL input; active low
VDD	34	P	+3.3V	+3.3V Power Supply
VSS	35	P	GND	Ground
REFCLK	36	I	TTL	Reference clock input, refer to table 2
VSSA	37	P	GND	Analog Ground (CMU)

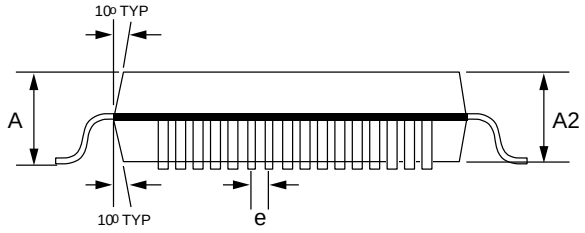
Signal	*Pin*	*I/O*	*Level*	*Pin Description*
N/C	38	-	-	No connection
C1P	39	O	ANALOG	CMU external capacitor (see Figure 6, and Table 1)
C1N	40	I	ANALOG	CMU external capacitor (see Figure 6, and Table 1)
C2N	41	I	ANALOG	CMU external capacitor (see Figure 6, and Table 1)
C2P	42	O	ANALOG	CMU external capacitor (see Figure 6, and Table 1)
VDDA	43	P	+3.3V	Analog Power Supply (CRU)
VSSA	44	P	GND	Analog Ground (CRU)
VSS	45	P	GND	Ground
VSS	46	P	GND	Ground
VDD	47	P	+3.3V	+3.3V Power Supply
VDD	48	P	+3.3V	+3.3V Power Supply
TXLSCKOUT	49	O	TTL	Transmit byte clock out
TXIN7	50	I	TTL	Transmit input data bit7
TXIN6	51	I	TTL	Transmit input data bit6
VSS	52	P	GND	Ground
TXIN5	53	I	TTL	Transmit input data bit5
TXIN4	54	I	TTL	Transmit input data bit4
TXIN3	55	I	TTL	Transmit input data bit3
TXIN2	56	I	TTL	Transmit input data bit2
TXIN1	57	I	TTL	Transmit input data bit1
TXIN0	58	I	TTL	Transmit input data bit0
STS12	59	I	TTL	155Mb/s or 622Mb/s mode select, refer to table 2
N/C	60	-	-	No connection
VDD	61	P	+3.3V	+3.3V Power Supply
EQULOOP	62	I	TTL	Equipment loopback, loops low speed byte wide transmit input data to receive output bus
FACLOOP	63	I	TTL	Facility loopback, loops high speed receive data and clock directly to transmit outputs.
N/C	64	-	-	No connection

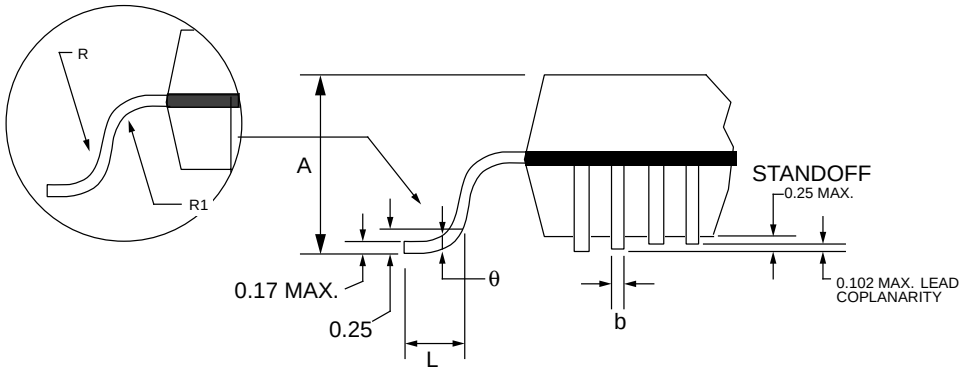
Package Information

64 Pin PQFP Package Drawings



Item	*mm*	*Tol.*
A	2.45	MAX
A2	2.00	+.10/-.05
D	13.20	±.25
D1	10.00	±.10
E	13.20	±.25
E1	10.00	±.10
L	0.88	±.15/-.10
e	0.50	BASIC
b	0.22	±.05
θ	0° - 7°	
R	.30	TYP
R1	.20	TYP





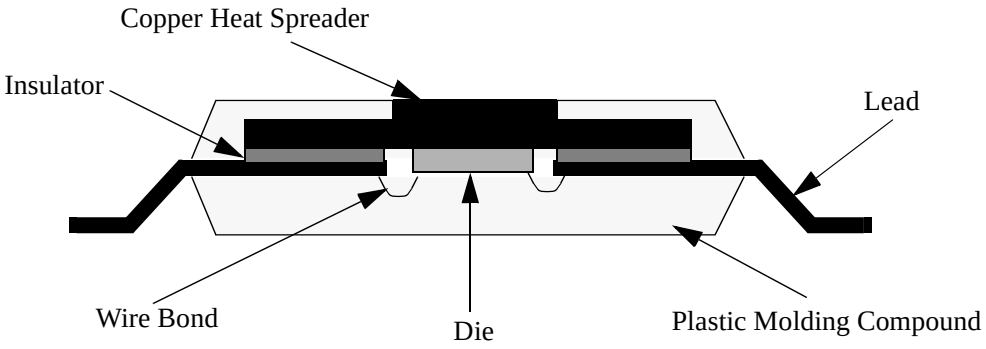
NOTES:

All drawings not to scale
All units in mm unless otherwise noted.
10 x 10 mm Package # 101-266-1
14 x 14 mm Package # 101-262-1

Package Thermal Characteristics

The VSC8116 is packaged into a thermally-enhanced plastic quad flatpack (PQFP). This package adheres to the industry-standard EIAJ footprint for a 10x10mm body but has been enhanced to improve thermal dissipation with the inclusion of an exposed Copper Heat Spreader. The package construction is as shown in Figure 10.

Figure 10: Package Cross Section



The thermal resistance for the VSC8116 package is improved through low thermal resistance paths from the die to the exposed surface of the heat spreader and from the die to the lead frame through the heat spreader overlap of the lead frame.

Table 13: 64-Pin PQFP Thermal Resistance

Symbol	*Description*	*Value*	*Units*
θ_{jc}	Thermal resistance from junction to case	2.5	^{o}C/W
θ_{ca}	Thermal resistance from case to ambient in still air including conduction through the leads for a non-thermally saturated board.	37	^{o}C/W
$\theta_{ca\text{-}100}$	Thermal resistance from case to ambient in 100 LPFM air	31	^{o}C/W
$\theta_{ca\text{-}200}$	Thermal resistance from case to ambient in 200 LPFM air	28	^{o}C/W
$\theta_{ca\text{-}400}$	Thermal resistance from case to ambient in 400 LPFM air	24	^{o}C/W
$\theta_{ca\text{-}600}$	Thermal resistance from case to ambient in 600 LPFM air	22	^{o}C/W

The VSC8116QB1 is designed to operate at a maximum case temperature of up to 115 ^{o}C. The user must guarantee that the maximum case temperature specification is not violated. Given the thermal resistance of the package in still air, the user can operate the VSC8116 in still air if the ambient temperature does not exceed 71^{o}C (71^{o}C = 115^{o}C - 1.2W * 37^{o}C/W). If operation above this ambient temperature is required, then an appropriate heatsink must be used with the part or adequate airflow must be provided.

Ordering Information

The order number for this product are:

Part Number	Device Type
VSC8116QP:	155Mb/s-622Mb/s Mux/Dmux with CMU in 64 Pin PQFP Commercial Temperature, 0°C ambient to 70°C case
VSC8116QP1	155Mb/s-622Mb/s Mux/Dmux with CMU in 64 Pin PQFP Extended Temperature, 0°C ambient to 115°C case
VSC8116QP2	155Mb/s-622Mb/s Mux/Dmux with CMU in 64 Pin PQFP Industrial Temperature, -40°C ambient to 85°C case

Notice

Vitesse Semiconductor Corporation reserves the right to make changes in its products specifications or other information at any time without prior notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to placing orders. The company assumes no responsibility for any circuitry described other than circuitry entirely embodied in a Vitesse product.

Warning

Vitesse Semiconductor Corporation's product are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

Application Notes

AC Coupling and Terminating High-speed PECL I/Os

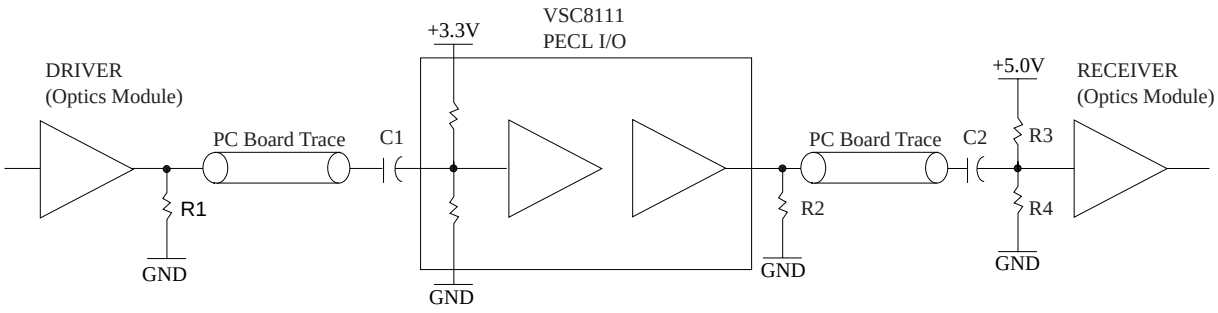
The high speed signals on the VSC8116 (RXDATAIN, RXCLKIN, TXDATAOUT, TXCLKOUT) use 3.3V PECL levels which are essentially ECL levels shifted positive by 3.3 volts. The PECL I/Os are referenced to the V_{DD} supply (VDD) and are terminated to ground. Since most optics modules use either ECL or 5.0V PECL levels, the high speed ports need to be either AC-coupled to overcome the difference in dc levels, or DC translated (DC level shift).

The PECL receiver inputs of the VSC8116 are internally biased at VDD/2. Therefore, AC-coupling to the VSC8116 inputs is accomplished by providing the pull-down resistor for the open-source PECL output and an AC-coupling capacitor used to eliminate the DC component of the output signal. This capacitor allows the PECL receivers of the VSC8116 to self-bias via its internal resistor divider network (see Figure 12).

The PECL output drivers are capable of sourcing current but not sinking it. To establish a LOW output level, a pull-down resistor, traditionally connected to VDD-2.0V, is needed when the output FET is turned off. Since VDD-2.0V is usually not present in the system, the resistor should be terminated to ground for convenience. The VSC8116 output drivers should be either AC-coupled to the 5.0V PECL inputs of the optics module, or translated (DC level shift). Appropriate biasing techniques for setting the DC-level of these inputs should be employed.

The DC biasing and 50 ohm termination requirements can easily be integrated together using a thevenin equivalent circuit as shown in Figure 11. The figure shows the appropriate termination values when interfacing 3.3V PECL to 5.0V PECL. This network provides the equivalent 50 ohm termination for the high speed I/Os and also provides the required dc biasing for the receivers of the optics module. Table 15 contains recommended values for each of the components.

Figure 11: AC Coupled High Speed I/O



Note: Only one side of a differential signal is shown.

Table 14: AC Coupling Component Values

Component	*Value*	*Tolerance*
R1	270 ohms	5%
R2	75 ohms	5%
R3	68 ohms	1%
R4	190 ohms	1%
C1, C2, C3, C4	.01uf High Frequency	10%

TTL Input Structure

The TTL inputs of the VSC8116 are 3.3V TTL which can accept 5.0V TTL levels within a given set of tolerances (see Table 11). The input structure, shown in Figure 12, uses a current limiter to avoid overdriving the input FETs.

Layout of the High Speed Signals

The routing of the High Speed signals should be done using good high speed design practices. This would include using controlled impedance lines (50 ohms) and keeping the distance between components to an absolute minimum. In addition, stubs should be kept at a minimum as well as any routing discontinuities. This will help minimize reflections and ringing on the high speed lines and insure the maximum eye opening. In addition the output pull down resistor R2 should be placed as close to the VSC8116 pin as possible while the AC-coupling capacitor C2 and the biasing resistors R3, R4 should be placed as close as possible to the optics input pin. The same is true on the receive circuit side. Using small outline components and minimum pad sizes also helps in reducing discontinuities.

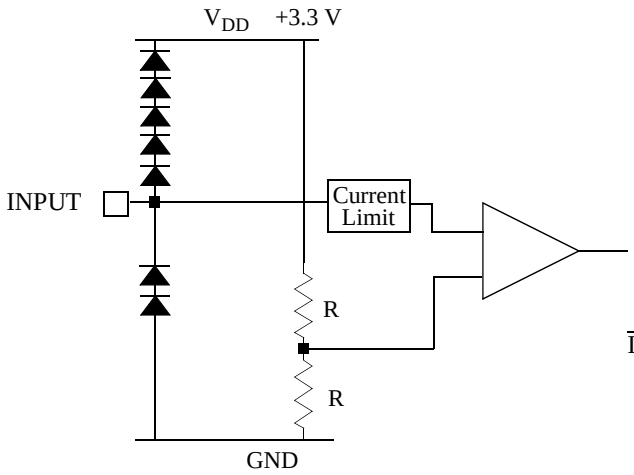
Ground Planes

The ground plane for the components used in the High Speed interface should be continuous and not sectioned in an attempt to provide isolation to various components. Sectioning of the ground planes tends to interfere with the ground return currents on the signal lines. In addition, the smaller the ground planes the less effective they are in reducing ground bounce noise and the more difficult to decouple. Sectioning of the positive supplies can provide some isolation benefits.

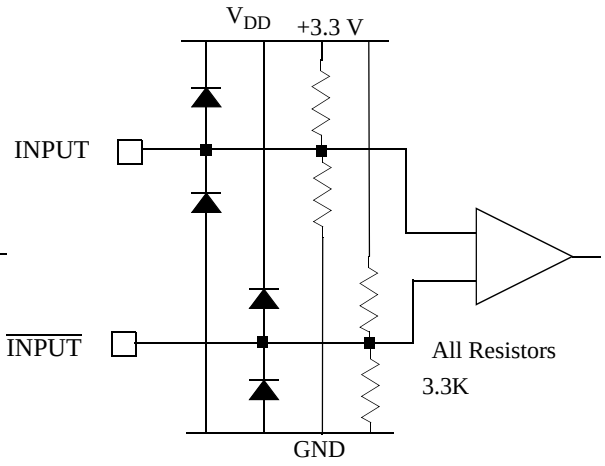
Analog Power Supplies

Good analog design practices should be applied to the board design for the analog ground and power planes. The dedicated PLL power (VDDA) and ground (VSSA) pins need to have quiet supply planes to minimize jitter generation within the clock synthesis unit. This is accomplished by either using a ferrit bead or a C-L-C choke (π filter).

Figure 12: Input Structures



REFCLK and TTL Inputs



High Speed Differential Input
(RXDATAIN+/RXDATAIN-)
(RXCLKIN+/RXCLKIN-)