VITESSE
SEMICONDUCTOR CORPORATION

Data Sheet

VSC8121

2.488GHz SONET/SDH Clock Generator

Features

- Monolithic Phase Locked Loop
- On-Chip LC Oscillator
- On-Chip Loop Filter
- TTL/CMOS Reference Clock
- Selectable Reference
- Jitter Meets SONET OC-48 and SDH STM-16 Requirements
- High-Speed CML Clock Output
- Single 3.3V Supply
- Compact 10mm x 10mm 44 Pin PQFP Package

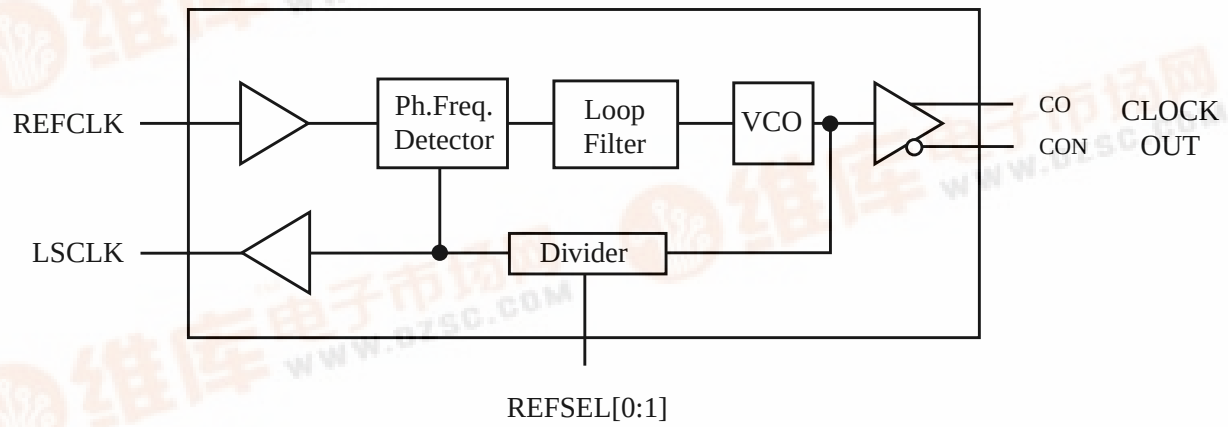
General Description

The VSC8121 is a monolithic Phase Locked Loop (PLL) based clock generator designed for telecommunications systems operating at 2.5Gb/s. The VSC8121 incorporates a reactance-based (LC) Voltage Controlled Oscillator (VCO) with low phase noise. The PLL's loop filter is on-chip.

The device has a differential 2.488GHz CML clock output (CO/CON) signal, a single-ended TTL low-speed clock (LSCLK) output equivalent in frequency to that of the reference clock, and a TTL reference clock input selectable for 51.84MHz, 77.76MHz or 155.52MHz. TTL inputs REFSEL[0:1] are used to make this selection.

A clean REFCLK signal is required since jitter below the PLL loop bandwidth, which is present on the REFCLK input, will appear on the output. Jitter on REFCLK at frequencies above the loop bandwidth will be attenuated by the PLL. The state of REFSEL[0:1] will select which frequency is expected on the REFCLK input.

VSC8121 Functional Block Diagram

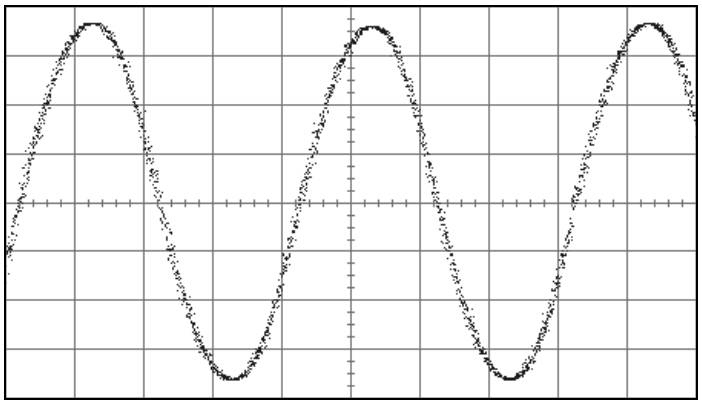


Applications Information

High-Speed Clock Output

The differential clock output waveforms produced by the VSC8121 are sinusoidal in nature, by design. This typically results in less noise generation than square pulses in most customer applications. Figure 1 shows a typical, single-ended clock output waveform produced by the device.

Figure 1: Typical Clock Output (CO) Waveform



CO and CON are high-speed CML outputs. As shown in Figure 2, the output driver consists of a differential pair designed to drive a 50Ω transmission line environment. Note that the output driver is back terminated to 50Ω on-chip to prevent reflections.

Careful layout of these signals is required for optimal performance. Figure 3 demonstrates various termination methods that may be employed, depending on the particular application. Either DC-coupling (termination #1 in Figure 3) or one of two AC coupling methods (terminations #2 and #3) may be used. As indicated, Vitesse recommends termination #2 for AC-coupling.

Figure 2: High-Speed Clock Output Diagram

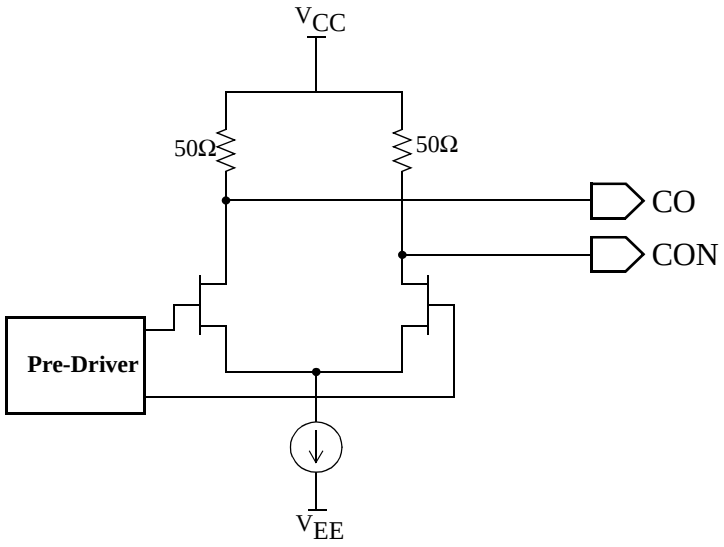
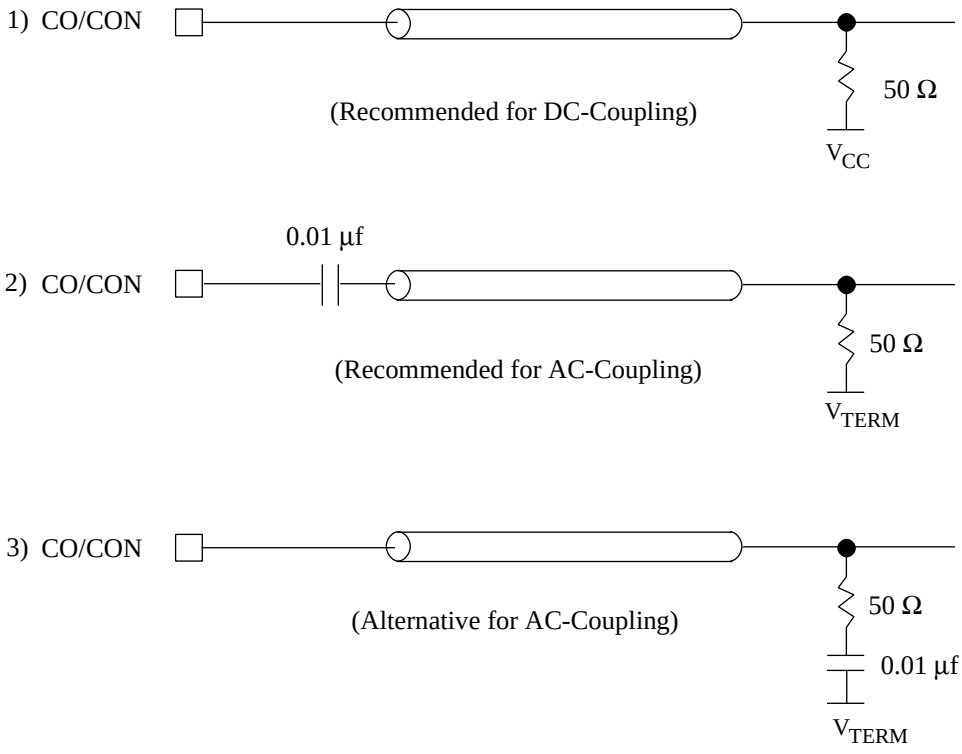


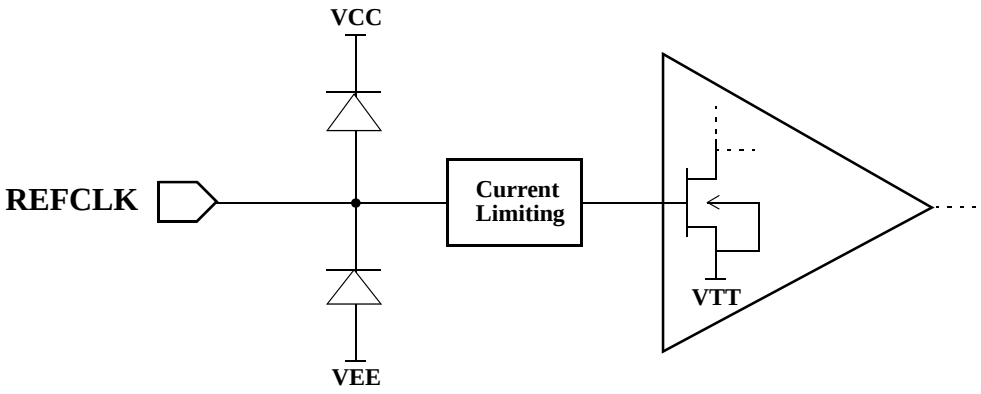
Figure 3: Example High-Speed CML Clock Output Terminations



Reference Clock Input

The input stage at the REFCLK input pin consists of ESD protection, followed by a current limiting circuit which precedes a driver responsible for providing the signal to the phase frequency detector. As pictured below in Figure 4, the driver has a high impedance, FET gate input. The additional resistance contributed by the current limiting circuit is relatively negligible.

Figure 4: Reference Clock Input Diagram



Care should be taken in selection of the reference clock. Time jitter on the reference clock which is within the PLL's loop bandwidth will appear on the 2.5GHz output. Telecom quality crystal oscillators from vendors such as Connor-Winfield or Vectron are suitable.

Table 1: Reference Clock Selection

REFSEL[1]	*REFSEL[0]*	*Selected Reference Frequency*	*Typical Loop Bandwidth*
0	0	51.84MHz	2500KHz
1	0	77.76MHz	3000KHz
Don't Care	1	155.52MHz	5500KHz

Die Usage

Vitesse optionally provides this device in unpackaged, die-only format for multi-chip module and related applications. For further informtion, please contact Vitesse.

AC Characteristics

Table 2: AC Characteristics

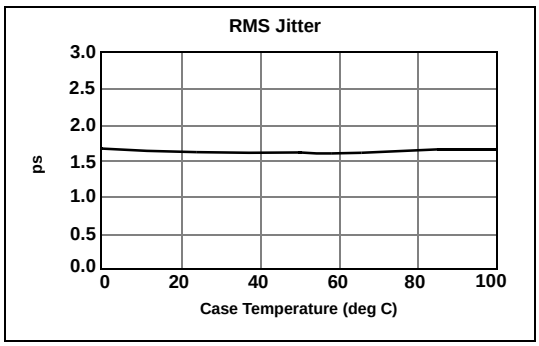
Parameter	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
T_{CLK}	High-speed output clock period	—	401.9	—	ps	
RC_d	Reference clock duty cycle	45	—	55	%	
RC_f	Reference clock frequency (selectable)	—	51.84, 77.76, or 155.52	—	MHz	
Δf_{RC}	Reference clock frequency tolerance	-100	—	+100	ppm(1)	
t_{jitter}	Jitter generation	—	1.75	3.6	ps RMS	12kHz to 20MHz. See Figure 5.

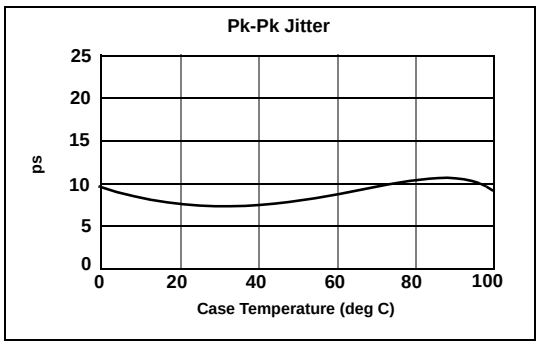
NOTE: (1) ppm refers to "parts per million." 100ppm (100/1000000) is equivalent to 0.01%. Therefore, the equivalent reference clock frequency range in MHz for +/-100ppm tolerance is as follows:

RC_f	*X 100ppm =*	*Acceptable Range*
51.84MHz	5.184KHz	51.83MHz to 51.85MHz
77.76MHz	7.776KHz	77.75MHz to 77.78MHz
155.52MHz	15.552KHz	155.51MHz to 155.54MHz

Note that +/-100ppm tolerance for reference clock frequency more than accommodates the SONET/SDH requirement that reference clock-supplying crystals function at +/-20ppm.)

Figure 5: RMS/Peak-to-Peak Jitter (12kHz - 20MHz), REF_CLK freq = 77.76MHz





DC Characteristics

Table 3: Low Speed I/O

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0 mA
V_{OL}	Output LOW voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0 mA
V_{IH}	Input HIGH voltage (TTL)	2.0	—	3.47	V	—
V_{IL}	Input LOW voltage (TTL)	0	—	0.8	V	—
I_{IH}	Input HIGH current (TTL)	—	50	500	µA	V_{IN} = 2.4V
I_{IL}	Input LOW current (TTL)	—	—	-500	µA	V_{IN} = 0.5V

Table 4: High-Speed Differential Outputs

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OD}	Output differential voltage	450	—	800	mV	
V_{OCM}	Output common-mode voltage	V_{CC} - 0.40	—	V_{CC} - 0.25	mV	Termination #1 (See Figure 3)
		V_{CC} - 0.80	—	V_{CC} - 0.50	mV	Termination #2 (See Figure 3)
		V_{CC} - 0.80	—	V_{CC} - 0.50	mV	Termination #3 (See Figure 3)

Note: Output jitter characteristics apply for differential outputs.

Table 5: Power Supply Currents

Parameter	Description	Min	Typ	Max	Units	Conditions
I_{CC}	Power supply current from V_{CC}			200	mA	Outputs Open
P_D	Power dissipation			0.7	W	Outputs Open

Absolute Maximum Ratings[1]

Power Supply Voltage (V_{CC}) Potential to GND ..... -0.5 V to +4.0 V
TTL Input Voltage Applied ..... -0.5 V to + 5.5V
Output Current (I_{OUT}) ..... 50 mA
Case Temperature Under Bias (T_C) ..... -55° to + 125°C
Storage Temperature (T_{STG}) ..... -65° to + 150°C

NOTE: (1) Caution: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{CC}) ..... +3.3V ±5%
Commercial Operating Temperature Range[1] (T) ..... 0°C to 85°C

NOTE: (1) Lower limit of specification is ambient temperature and upper limit is case temperature.

ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8121 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

Note: If used single-ended, the unused output should be terminated.

Package Pin Descriptions

Figure 6: Pin Diagram

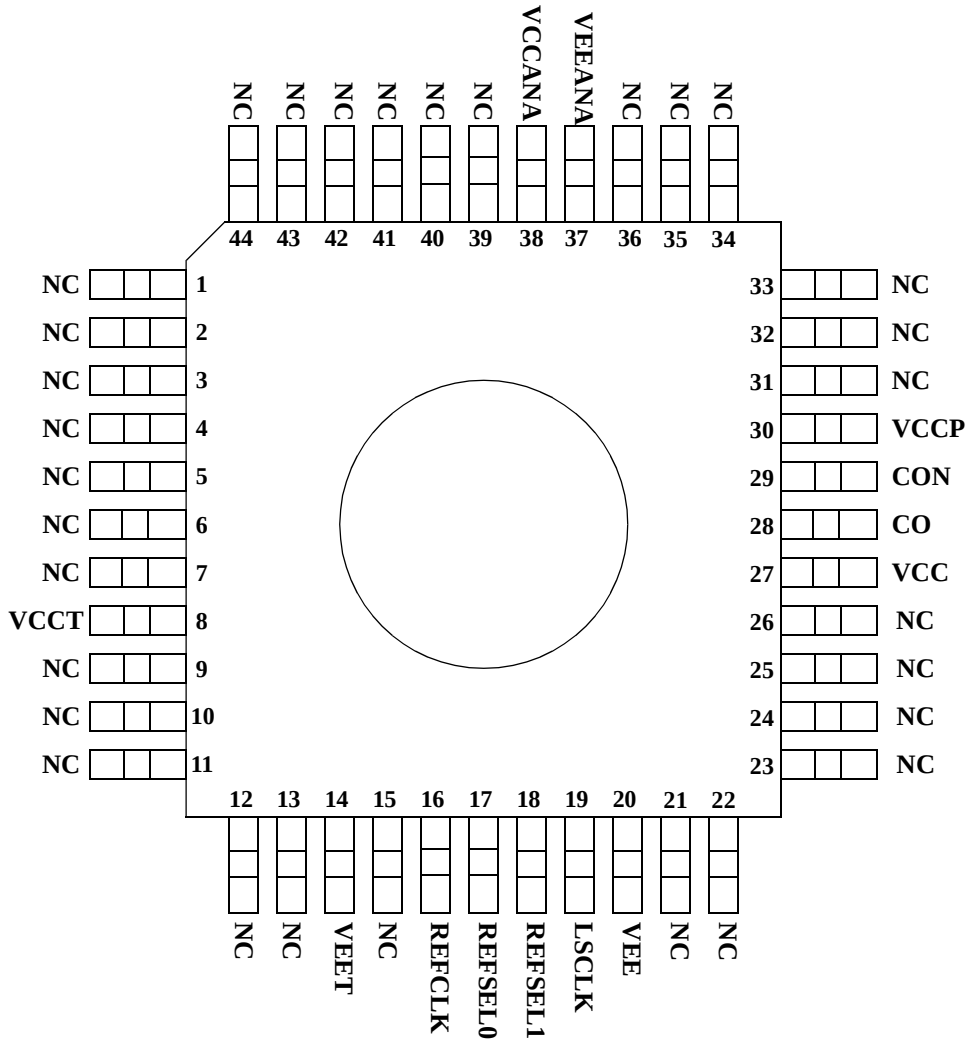


Table 6: Package Pin Identification

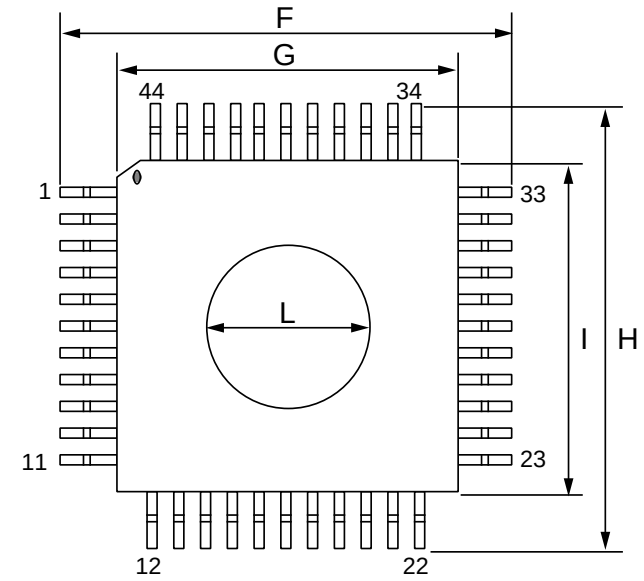
Signal Name	*Pin #*	*I/O*	*Level*	*Description*
NC	1	-	-	Do not connect, leave open(1)
NC	2	-	-	Do not connect, leave open(1)
NC	3	-	-	Do not connect, leave open(1)
NC	4	-	-	Do not connect, leave open(1)
NC	5	-	-	Do not connect, leave open(1)
NC	6	-	-	Do not connect, leave open(1)
NC	7	-	-	Do not connect, leave open(1)
V_{CCT}	8	Positive Supply	3.3V	For TTL I/O
NC	9	-	-	Do not connect, leave open(1)
NC	10	-	-	Do not connect, leave open(1)
NC	11	-	-	Do not connect, leave open(1)
NC	12	-	-	Do not connect, leave open(1)
NC	13	-	-	Do not connect, leave open(1)
V_{EET}	14	Negative Supply	GND	For TTL I/O
REFCLK	16	TTL Input	TTL	Reference Clock
REFSEL[0]	17	TTL Input	TTL	Selects Reference Frequency
REFSEL[1]	18	TTL Input	TTL	Selects Reference Frequency
LSCLK	19	TTL Output	TTL	Low Speed PLL Output
V_{EE}	20	Negative Supply	GND	
NC	21	-	-	Do not connect, leave open(1)
NC	22	-	-	Do not connect, leave open(1)
NC	23	-	-	Do not connect, leave open(1)
NC	24	-	-	Do not connect, leave open(1)
NC	25	-	-	Do not connect, leave open(1)
NC	26	-	-	Do not connect, leave open(1)
V_{CC}	27	Positive Supply	3.3V	
CO	28	Output	2.7 - 3.3V	High-Speed Clock Out
CON	29	Output	2.7 - 3.3V	High-Speed Clock Out Complement
V_{CCP}	30	Positive Supply	3.3V	Supply for High-Speed Outputs (2)
NC	31	-	-	Do not connect, leave open(1)
NC	32	-	-	Do not connect, leave open(1)
NC	33	-	-	Do not connect, leave open(1)
NC	34	-	-	Do not connect, leave open(1)
NC	35	-	-	Do not connect, leave open(1)
NC	36	-	-	Do not connect, leave open(1)
V_{EEANA}	37	Negative Supply	GND	For Analog Section
V_{CCANA}	38	Positive Supply	3.3V	For Analog Section(2)
NC	39	-	-	Do not connect, leave open(1)

Signal Name	Pin #	I/O	Level	Description
NC	40	-	-	Do not connect, leave open(1)
NC	41	-	-	Do not connect, leave open(1)
NC	42	-	-	Do not connect, leave open(1)
NC	43	-	-	Do not connect, leave open(1)
NC	44	-	-	Do not connect, leave open(1)

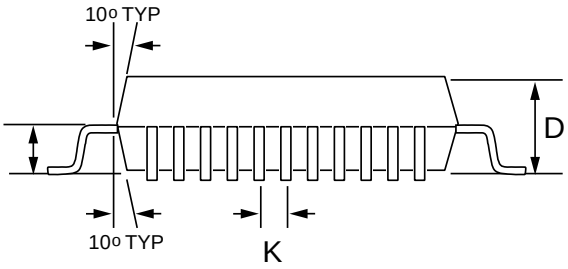
NOTE: (1) Leave unconnected. Terminating these pins to GND, VEE or otherwise may have an adverse effect on the performance of the device. (2) VCC pins 30 and 38 are internally connected to each other.

Package Information

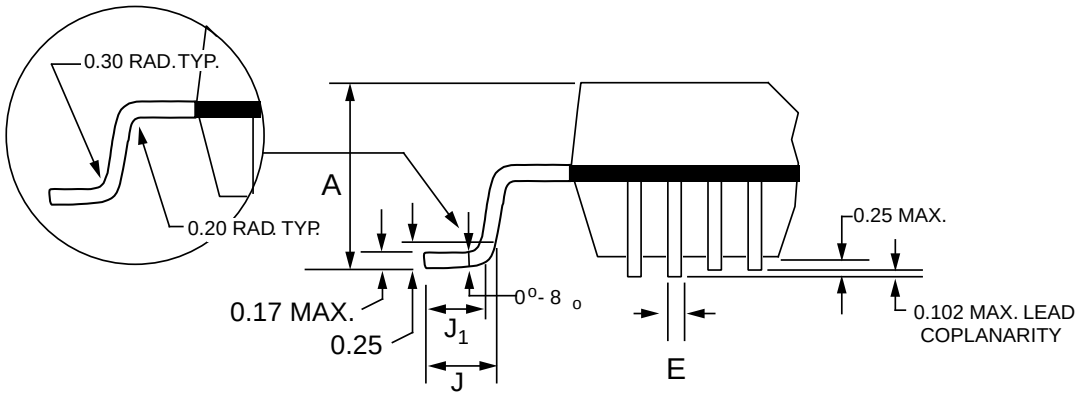
44-Pin PQFP Package Drawing



Item	*mm*	*Tol.*
A	2.45	MAX
D	2.00	+.10 / -.05
E	0.35	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	+.15 / -.10
J1	0.80	+.15 / -.10
K	0.80	BASIC
L	3.56	±.50 DIA.



Drawing not to scale.
Heat spreader up.
All units in mm unless otherwise noted.
Package #: 101-299-1
Issue #: 1



Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the Table 7.

Table 7: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{JC}	Thermal resistance from junction-to-case.	2.0
θ_{CA}	Thermal resistance from case-to-ambient with no airflow, including conduction through the leads.	35.0

Thermal Resistance With Airflow

Shown in Table 8 is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst-case power of the device multiplied by the thermal resistance.

Table 8: Thermal Resistance With Airflow

Airflow	θ_{CA} *(°C/W)*
100 lfpm	28
200 lfpm	25
400 lfpm	21
600 lfpm	18

Maximum Ambient Temperature Without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

θ_{CA} = Theta case to ambient at appropriate airflow
$T_{A(MAX)}$ = Ambient Air temperature
$T_{C(MAX)}$ = Case temperature (85ºC for VSC8121)
$P_{(MAX)}$ = Power (0.7W for VSC8121)

Table 9: Maximum Ambient Air Temperature Without Heatsink

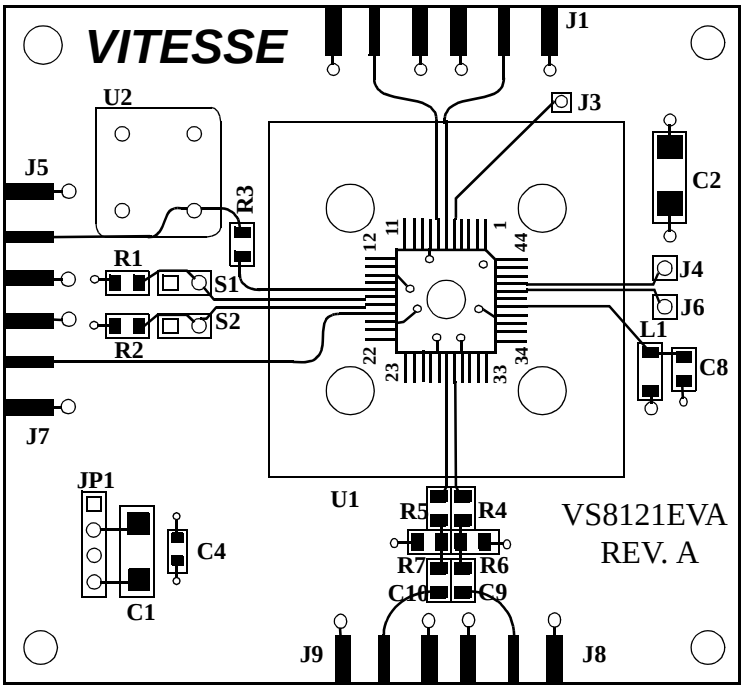
Airflow	$T_{A(MAX)}$ *°C*
None	60
100 lfpm	65
200 lfpm	68
400 lfpm	70
600 lfpm	72

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

VSC8121 Evaluation Board

An evaluation board is available from Vitesse which can be used to characterize the performance of the VSC8121 2.488GHz SONET/SDH Clock Generator. The following sections provide a layout for the board, general notes regarding usage and descriptions of input/output ports, as well as an example equipment setup. To learn more about how to order this board for your evaluation needs, please contact your local Vitesse Sales Office.

Figure 7: Top-view Layout of the VSC8121 Evaluation Board



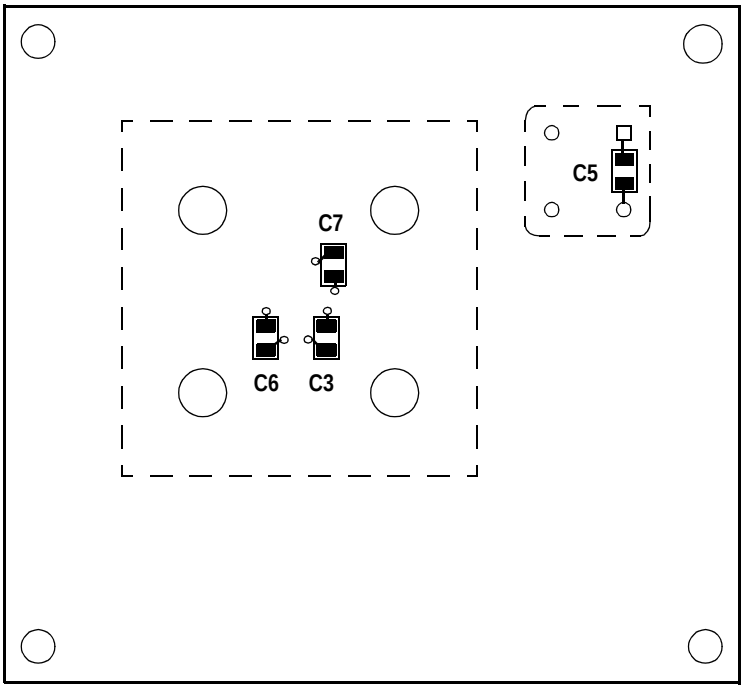
Board dimensions:
3” x 2.75” x 0.06”

Component Values:
R1 = 10kΩ
R2 = 10kΩ
R3 = 11Ω
R4 = 0Ω
R5 = 0Ω
R6 = leave open
R7 = leave open

C1 = 10µF
C2 = 10µF
C4 = 0.1µF
C8 = 0.1µF
C9 = 0.01µF
C10 = 0.01µF

L1 = TDK-CB50-1206 ferrite

Figure 8: Location of Additional Components on Back Side of the VSC8121 Evaluation Board



Component Values:
C3 = 0.1µF
C5 = 0.1µF
C6 = 0.1µF
C7 = 0.1µF

Equipment for Typical Set-up

VSC8121 Evaluation Board
Signal Generator or 155.52MHz Crystal Oscillator
Digital Oscilloscope
DC Power Supply

Power Supply Settings

VCC Set to 3.3V (Current draw will be approximately 180mA)

Reference Clock

To provide a reference clock to the VSC8121, either a Signal Generator or telecom-quality Crystal Oscillator can be used. The REFCLK level should be near 900mV(RMS) and, as listed in Table 1 of this specification, operate at either 51.84MHz, 77.76MHz, or 155.52MHz. The evaluation board is preconfigured to run with a 155.52MHz reference clock, but can be easily modified to accept one of the other two frequency choices.

Table 10: REFSEL [0,1] Switch Settings (S1, S2) For Selected Reference Frequency

REFSEL[0] (S1)	*REFSEL[1] (S2)*	*Selected Reference Frequency*
0	0	51.84MHz
0	1	77.76MHz
1	Don't Care	155.52MHz

As reiterated above, the selected reference frequency is determined by the TTL inputs REFSEL[0] and REFSEL[1]. The board can be made to operate with a REFCLK of either 51.84MHz or 77.76MHz by closing or opening the appropriate connections at locations S1 and S2. As indicated in Table 10, S1 controls REFSEL[0], and S2 controls REFSEL[1]. Closing one of these connections shorts the corresponding REFSEL pin to VEE. You may either place a permanent short across the desired pin, or place a switch in both locations to leave the option of toggling to different reference clock settings. (As an example, to configure the device to expect a 77.76MHz frequency, you would place a short or close the switch across S1 and leave S2 open.)

Recommended Evaluation Board Connections

Chabin to Banana Jack Connections

- **JP1** (2nd position) to positive terminal of VS1
- **JP1** (4th position) to negative terminal of VS1

(Optionally, microclip or other connectors can be used to route power as deemed practical by the customer)

SMA Cable Connections

- **J5** (REFCLK) to the RF Out port of the Signal Generator, -or- you may leave J5 unconnected and place a crystal oscillator in location U2 (see the Using A Crystal Oscillator section below)
- **J7** (LSCLK) to the external TRIGGER input of the Digital Oscilloscope
- **J8** (CON) to Ch 1 of the Digital Oscilloscope
- **J9** (CO) to Ch 2 of the Digital Oscilloscope

NOTE: Ports not listed are not required for normal operation of the device, and should be left unconnected.

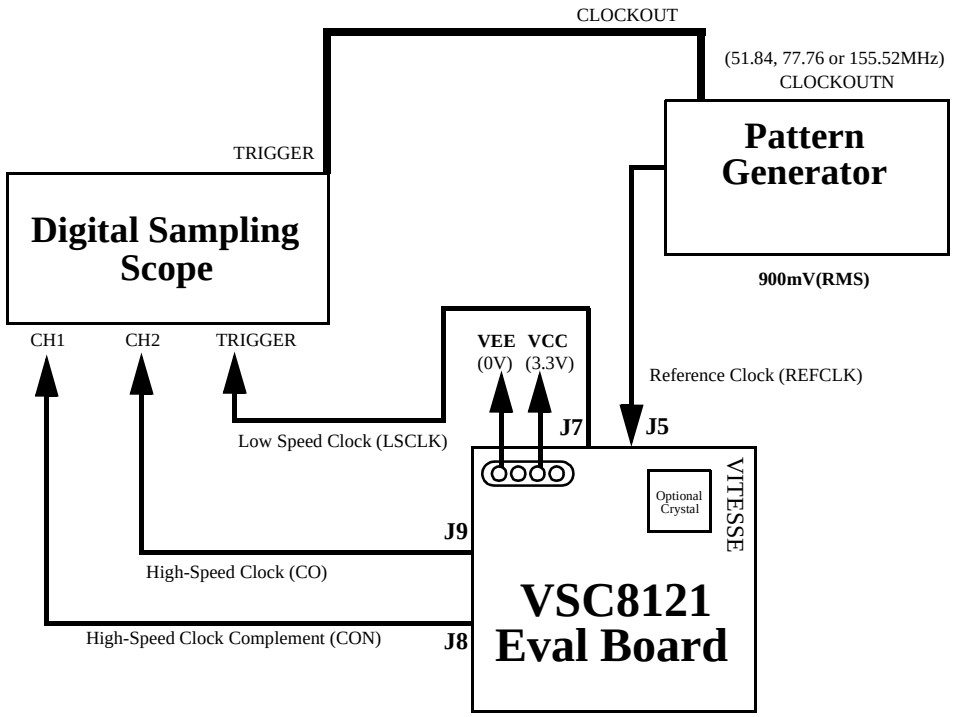
Using a Crystal Oscillator

The board provides an option for a crystal oscillator if it is not desired to drive the reference clock signal with a signal generator or other device. A telecom-quality 155.52MHz crystal is recommended, since the goal should be to introduce the least amount of jitter into the input as possible. Certain frequencies of jitter (those below the loop bandwidth of the PLL) introduced at the REFCLK input will appear directly at the output of the device.

Example Set-Up

The figure below shows one possible set-up using the VSC8121 Evaluation Board and recommended connections listed above. In this configuration, the device receives its reference clock input from an external signal generator supplying a 900mV(RMS) signal. As an alternative, a crystal oscillator may be used instead to provide this reference. The CO and CON (High-Speed Clock True and Complement) and LSCLK signals may then be viewed with the scope, as shown on channels 1 through 3. Alternatively, if only one output is being viewed by the scope, a 50ohm termination should be used on the remaining output to achieve more accurate measurements.

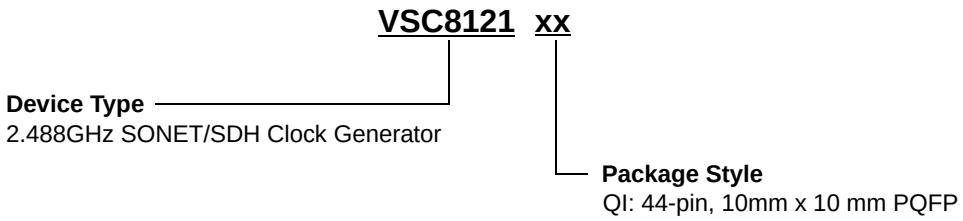
Figure 9: Example Equipment Set-up Using the VSC8121 Evaluation Board



The intent of this section is to answer the most common questions surrounding the use of the VSC8121 Evaluation Board. Please contact your local sales office if there are any additional details that Vitesse Semiconductor can provide to help you make more efficient use of your evaluation board.

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



Revision History

Item	Rev No.	Date	Section/Figure/ Table	Page	Description
1	4.1	2/4/00	General Description	1	Add CML text to the clock output, Deleted PECL output
2	4.1	2/4/00	Features	1	Changed to High-Speed clock output
3	4.1	2/4/00	Application Info	2	Add High-Speed CML outputs, Deleted PECL/ECL clock outputs
4	4.1	2/4/00	Figure 3	3	Changed to High-Speed CML Clock output terminations
5	4.1	2/4/00	Table 4	6	Changed to High-Speed Differential outputs, deleted the PECL/ECL outputs
6	4.1	2/4/00	Table 6	9,10	Added Level Column to I/O's
7	4.1	2/4/00	Table 7	12	Changed Theta Juntion to Case to 2.0
8	4.1	2/4/00	Figure	16	Changed CH3 to Trigger