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Data Sheet
VSC8122

Multi-Rate SONET/SDH
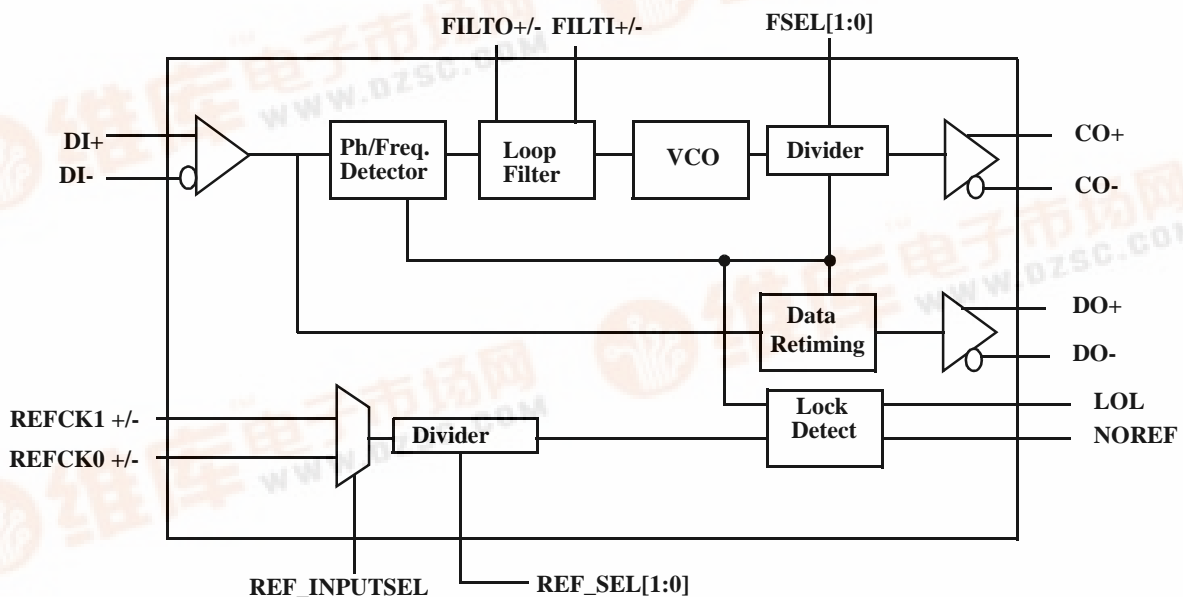*Clock and Data Recovery IC*

Features

- Multi-Rate OC-3, OC-12, OC-24, OC-48 Clock and Data Recovery
- Supports Gigabit Ethernet
- Differential Back Terminated I/O
- Maintains Clock Output in the Absence of Data
- Selectable Reference Clock

- Loss of Lock Indicator
- Exceeds SONET/SDH Requirements for Jitter Tolerance, Jitter Transfer and Jitter Generation.
- 3.3V Supply Operation
- 1W Typical Power
- 64-pin , 10x10mm PQFP Packaging

General Description

The VSC8122 is a single-chip clock recovery IC for use in SONET OC-48, OC-24, OC-12, OC-3, or Gigabit Ethernet systems operating at their respective 2.48832Gb/s, 1.24416Gb/s, 622.08Mbps, 155.52Mbps, or 1.25Gbps data rates. The VSC8122 complies with SONET jitter tolerance, jitter transfer and jitter generation specifications.

Alarm functions support typical telecom system applications. The Loss of Lock (LOL) output indicates when the device goes out of lock, which would most often occur in the event of a loss of valid data. The NOREF output flags when the reference input to the VSC8122 either is removed, or goes severely out of tolerance.

VSC8122 Block Diagram

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Functional Description

Data Input

The data input receiver is internally terminated by a center-tapped resistor network. For differential input AC coupling, the network is terminated to the appropriate termination voltage, V_{TERM} through a blocking capacitor, C_{AC} to ground. The input requires a differential signal with a peak-to-peak voltage on both the true and complement of a minimum of 250mV. These inputs are required to be AC-coupled to allow use with a variety of limiting amplifiers.
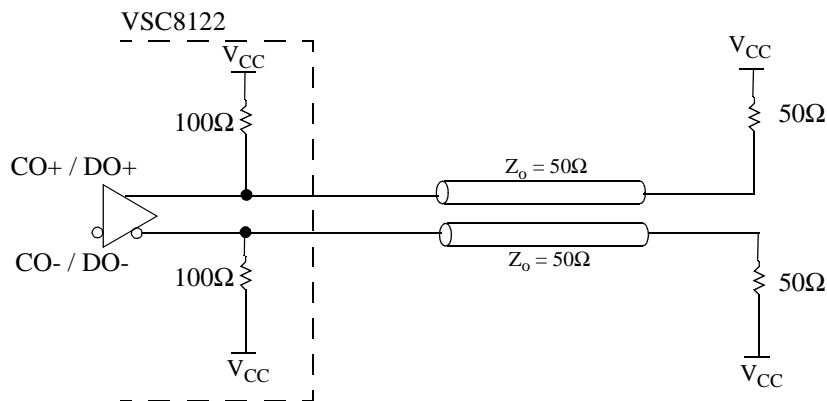
Figure 1: Input Termination (AC-Coupled)
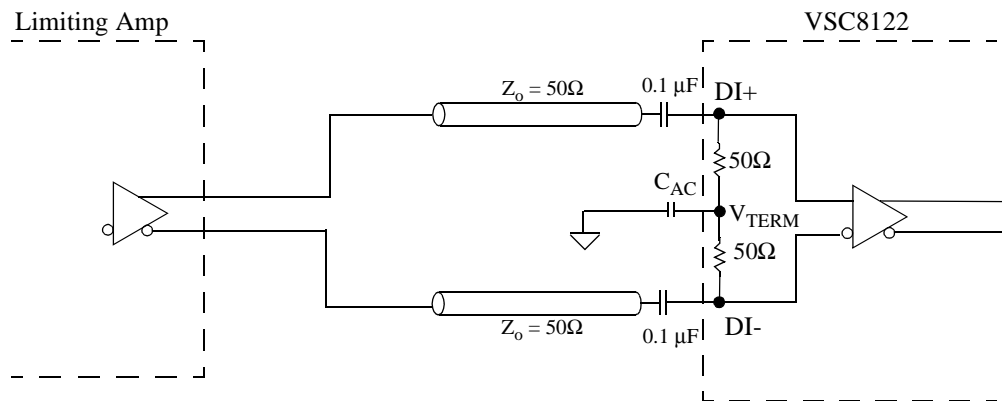

High-Speed Clock and Data Outputs

The VSC8122 high-speed clock and data outputs can be DC-terminated, 50Ω to V_{CC} as indicated in Figure 2.

Figure 2: High-Speed Clock and Data Output DC Termination

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Outputs can also be AC terminated as shown in Figure 3. The output differential voltage and common-mode voltage range are specified in Table 4, High-Speed Inputs and Outputs.

Figure 3: High-Speed Clock and Data Output AC Termination
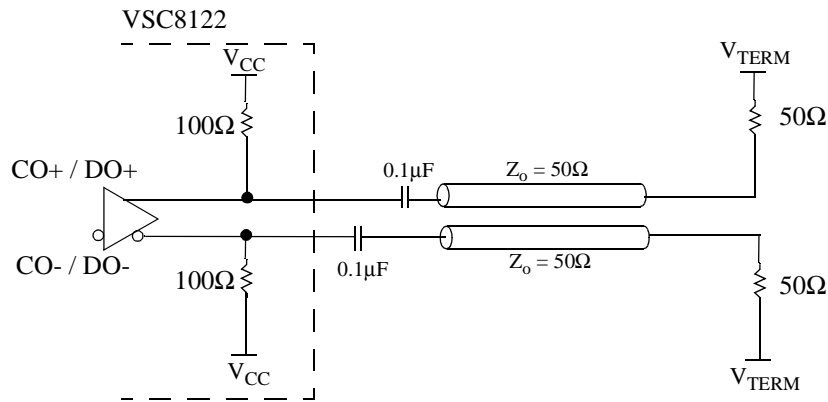
Clock Recovery

The VSC8122 has a selectable input data rate. Two pins (FSEL0 and FSEL1) select the data rate to be provided to the VSC8122.

Table 1: Input Data Rate Select

Input Data Rate	FSEL0	FSEL1
2.48832Gb/s or 2.5Gb/s	0	0
1.24416Gb/s or 1.25Gb/s	1	0
622.08Mb/s or 625Mb/s	0	1
155.52Mb/s or 156.25Mb/s	1	1

The incoming data is presented both to the clock recovery circuit and the data retiming circuit. When there is a phase error between the incoming data and the on-chip Voltage-Controlled Oscillator (VCO), the loop filter raises or lowers the control voltage of the VCO to null the phase difference.

The lock detector monitors the frequency difference between the REFCK (optionally divided by a prescaler) and the recovered clock divided by 128. In the event of the loss of an input signal, or if the input is switching randomly, the VCO will move in one direction. At the time the VCO differs by more than 1MHz from the REFCK based 2.48832GHz rate, the lock detector will assert the LOL output. LOL is designed to be asserted from between 2.3μs and 100μs after the interruption of data. The VCO will continue to be frequency-locked at approximately 1MHz off of the REFCK based 2.48832GHz rate.

When NRZ data is again presented at the data input, the phase detector will permit the VCO to lock to the incoming data. Hysteresis is provided which delays the deassertion of LOL until approximately 160μs following the restoration of valid data.
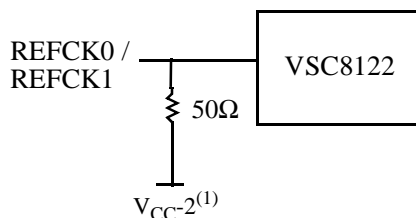
The NOREF output will go high to indicate that there is no signal on the REFCK input, or that the REFCK is more than approximately 25% above or below the expected value.

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Two sets of reference frequencies for the VSC8122 are shown in Table 2. SONET reference clock frequencies are as indicated, with Gigabit Ethernet frequencies listed in parenthesis. The two different sets of reference clocks are needed since the reference clock for SONET and Gigabit Ethernet applications will be slightly different. Internally, the VSC8122 requires a 19.44MHz reference (or 19.53MHz reference for Gigabit Ethernet). The customer can select to provide either the 19.44MHz reference (or 19.53MHz reference for Gigabit Ethernet), or the 2x, 4x or 8x of that reference at 38.88MHz (39.06MHz), 77.76MHz (78.13MHz) or 155MHz (156.25MHz). The REF_SEL[1:0] inputs will program the internal divider as required to use the selected REFCK frequency.

Two reference clock inputs are provided, REFCK1 and REFCK0, to allow "on-the-fly switching" between SONET and Gigabit Ethernet applications if desired. Since SONET and Gigabit Ethernet require different reference clock frequencies, the VSC8122 allows the user to toggle between the two reference clock frequencies (REFCK1 and REFCK0) to supply the appropriate input clock. REF_INPUTSEL is used to toggle between the two reference clock input frequencies; REF_INPUTSEL= "0" selects REFCK0 and REF_INPUTSEL= "1" selects REFCK1. Either reference clock input (REFCK1, REFCK0) can be used for SONET or Gigabit Ethernet reference frequencies. LVPECL levels are recommended for REFCK inputs (see Figure 4). If a reference clock is unused, it is recommended that one of its inputs be tied to V_{CC} through a 5.1kΩ resistor, the other one to GND through a 5.1kΩ resistor.

Figure 4: REFCK Input Levels

LVPECL Level REFCK Inputs (recommended)   NON- LVPECL Level REFCK Inputs
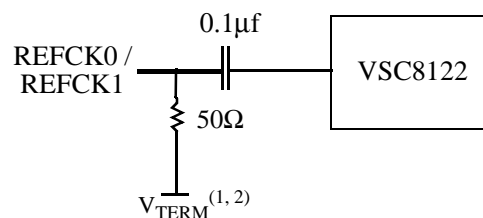
NOTES: (1) For differential REFCK input signals, 100Ω termination between true and complement REFCK signals can be substituted for the 50Ω to V_{TERM} termination on each line.

(2) With the input ac-coupled, V_{TERM} can be to any power supply required for the upstream device.

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Table 2: Reference Frequency

| Reference Frequency	REF_SEL0	REF_SEL1
19.44MHz (19.53MHz)	0	0
38.88MHz (39.06MHz)	1	0
77.76MHz (78.13MHz)	0	1
155.52MHz (156.25MHz)	1	1

Loop Filter

The Phase-Lock Loop (PLL) on the VSC8122 employs two external capacitors. The PLL design is fully differential, therefore the loop filter must also be fully differential. One capacitor should be connected between FILTAO and FILTAI, with the other connected between FILTAON and FILTAIN. Recommended capacitors are low-inductance 1.0μF (0603 or 0805) ceramic SMT X7R devices, 6.3 WVDC or greater, with tolerance of 10% or better.

AC Characteristics (Over recommended operating conditions)

Table 3: AC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
t_{pd}	Center of output data eye from rising edge of CO+	-75	—	+75	ps	
t_r, t_f	DO± rise and fall times	—	—	150	ps	20% to 80% into 50Ω load.
t_r, t_f	CO± rise and fall times	—	—	135	ps	20% to 80% into 50Ω load.
$Jitter_{gen}$	Jitter Generation (12kHz-20MHz)	—	—	3.6	ps - rms	Measured at the HS data output for jitter in the 12kHz - 20MHz band. Assume 1.2ps rms input data jitter.
$Jitter_{tol}$	Jitter Tolerance	—	—	—	—	Exceeds SONET/SDH mask
LBW	Loop Bandwidth	—	—	2.0	MHz	-3dB point of jitter transfer curve
$Jitter_{peak}$	Jitter Peaking	—	—	0.1	dB	

Figure 5: High-Speed Clock and Data Outputs
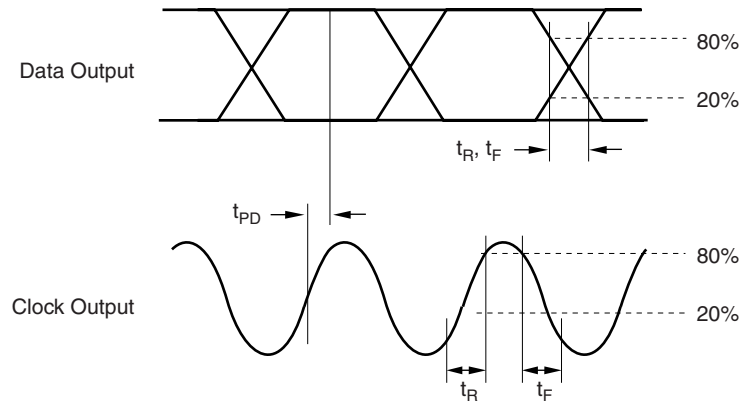
Table 4: High-Speed Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
ΔV_{OD}	Data output voltage swing	600	900	1000	mV	
ΔV_{OC}	Clock output voltage swing	500	700	1000	mV	
V_{CMO}	Common-mode range (DO/CO)	2.6	—	3.2	V	
V_{DIFF}	Serial input absolute voltage, single ended peak-to-peak swing (V_{IH}-V_{IL}) for DI +/-	250	—	1200	mV	AC-coupled
R_{IN}	Input resistance between DI+ and V_{TERM} or DI- and V_{TERM}	43	—	58	Ω	

Table 5: PLL Parameters

Parameters	Description	Min	Typ	Max	Units	Conditions
	REF_CLK Duty Cycle	45	—	55	%	
	REF_CLK Frequency Range	-100	—	+100	ppm	
V_{IH}	REF_CLK Input High Voltage	V_{CC}-1.165	—	V_{CC}-0.7	V	
V_{IL}	REF_CLK Input Low Voltage	V_{CC}-2.0	—	V_{CC}-1.475	V	

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DC Characteristics (Over recommended operating conditions)

Table 6: TTL Inputs and Outputs

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH voltage	2.4	—	—	V	$I_{OH} = -1.0mA$
V_{OL}	Output LOW voltage	—	—	0.5	V	$I_{OL} = 1.0mA$
V_{IH}	Input HIGH voltage	2.0	—	3.47	V	
V_{IL}	Input LOW voltage	0	—	0.8	V	
I_{IH}	Input HIGH current	—	50	500	µA	$V_{IN} = 2.4V$
I_{IL}	Input LOW current	—	—	500	µA	$V_{IN} = 0.5V$

Table 7: Power Supply

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{CC}	Supply voltage	3.14	3.3	3.47	V	$3.3V \pm 5\%$
P_D	Power dissipation	—	1.0	1.2	W	Outputs terminated
I_{CC}	Supply current	—	300	347	mA	Outputs terminated

Absolute Maximum Ratings [1]

Power Supply Voltage (V_{CC}) .... -0.5V to +3.8V
DC Input Voltage (differential inputs) .... -0.5V to V_{CC} +0.5V
DC Input Voltage (TTL inputs) .... -0.5V to +5.5V
DC Output Voltage (TTL outputs) .... -0.5V to V_{CC} + 0.5V
Output Current (TTL outputs) .... +/-50mA
Output Current (differential outputs) .... +/-50mA
Case Temperature Under Bias .... -55°C to +125°C

NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without caus-
ing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended
periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage, (V_{CC}) .... +3.3V$\pm$5%
Operating Temperature Range .... 0°C Ambient to +85°C Case Temperature
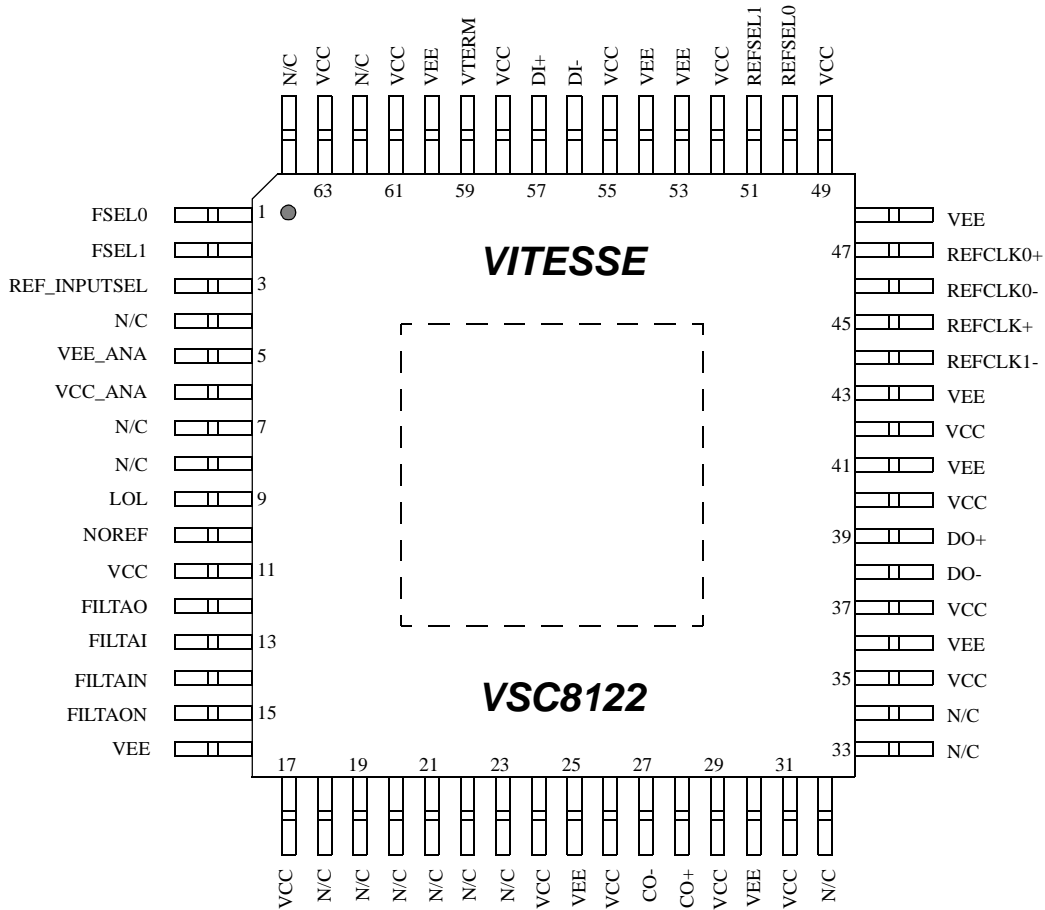
ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8122 is rated to the following ESD voltages based on the human body model:
1. All pins are rated at or above 1500V.

Package Pin Descriptions

Figure 6: Pin Diagram
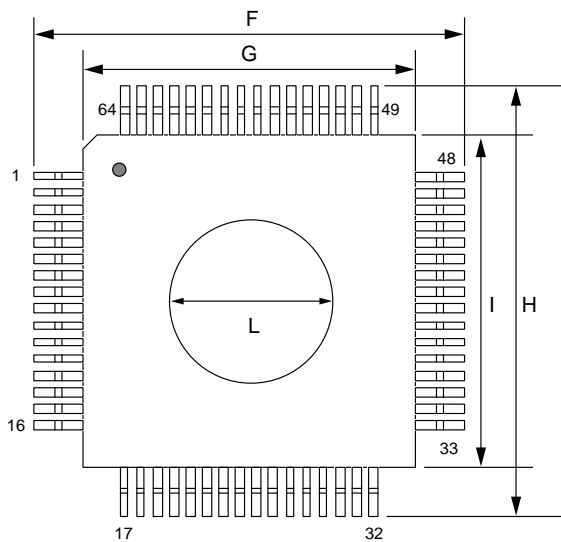
Top View

Table 8: Pin Identifications

Pin #	Name	I/O	Level	Description
1	FSEL0	I	TTL	Selectable input rate pin 0
2	FSEL1	I	TTL	Selectable input rate pin 1
3	REF_INPUTSEL	I	TTL	Toggle between REFCK1 and REFCK0
4	NC	—	—	No connect, leave unconnected[1]
5	VEE_ANA	I	GND typ.	Negative power supply pins for analog parts of CMU
6	VCC_ANA	I	+3.3V typ.	Positive power supply pins for analog parts of CMU
7	NC	—	—	No connect, leave unconnected
8	NC	—	—	No connect, leave unconnected
9	LOL	O	TTL	Loss of lock indication
10	NOREF	O	TTL	No reference output. Active HIGH for REFCK far off the expected frequency.
11	VCC	I	+3.3V typ.	Positive power supply
12	FILTAO	I	—	Loop filter pin - connect via capacitor to FILTAI
13	FILTAI	I	—	Loop filter pin - connect via capacitor to FILTAO
14	FILTAIN	I	—	Loop filter pin - connect via capacitor to FILTAON
15	FILTAON	I	—	Loop filter pin - connect via capacitor to FILTAIN
16	VEE	I	GND typ.	Negative power supply
17	VCC	I	+3.3V typ.	Positive power supply
18	NC	—	—	No connect, leave unconnected[1]
19	NC	—	—	No connect, leave unconnected[1]
20	NC	—	—	No connect, leave unconnected[1]
21	NC	—	—	No connect, leave unconnected[1]
22	NC	—	—	No connect, leave unconnected[1]
23	NC	—	—	No connect, leave unconnected[1]
24	VCC	I	+3.3V typ.	Positive power supply
25	VEE	I	GND typ.	Negative power supply
26	VCC	I	+3.3V typ.	Positive power supply
27	CO-	O	HS	High-speed clock output, complement
28	CO+	O	HS	High-speed clock output, true
29	VCC	I	+3.3V typ.	Positive power supply
30	VEE	I	GND typ.	Negative power supply
31	VCC	I	+3.3V typ.	Positive power supply
32	NC	—	—	No connect, leave unconnected[1]
33	NC	—	—	No connect, leave unconnected[1]
34	NC	—	—	No connect, leave unconnected[1]

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| Pin #	Name	I/O	Level	Description
35	VCC	I	+3.3V typ.	Positive power supply
36	VEE	I	GND typ.	Negative power supply
37	VCC	I	+3.3V typ.	Positive power supply
38	DO-	O	HS	High-speed data output, complement.
39	DO+	O	HS	High-speed data output, true
40	VCC	I	+3.3V typ.	Positive power supply
41	VEE	I	GND typ.	Negative power supply
42	VCC	I	+3.3V typ.	Positive power supply
43	VEE	I	GND typ.	Negative power supply
44	REFCK1-	I	LVPECL	Reference clock 1 input, complement
45	REFCK1+	I	LVPECL	Reference clock 1 input, true
46	REFCK0-	I	LCPECL	Reference clock 0 input, complement
47	REFCK0+	I	LVPECL	Reference clock 0 input, true
48	VEE	I	GND typ.	GND power supply
49	VCC	I	+3.3V typ.	Positive power supply
50	REF_SEL[0]	I	—	Reference clock rate select pin 0
51	REF_SEL[1]	I	—	Reference clock rate select pin 1
52	VCC	I	+3.3V typ.	Positive power supply
53	VEE	I	GND typ.	Negative power supply
54	VEE	I	GND typ.	Negative power supply
55	VCC	I	+3.3V typ.	Positive power supply
56	DI-	I	HS	High-speed data input, complement
57	DI+	I	HS	High-speed data input, true
58	VCC	I	+3.3V typ.	Positive power supply
59	VTERM	I	0V->3.3V	High-speed data input termination voltage (may be connected to ground through a series AC-coupling capacitor)
60	VEE	I	GND typ.	Negative power supply
61	VCC	I	+3.3V typ.	Positive power supply
62	NC	—	—	No connect, leave unconnected
63	VCC	I	+3.3V typ.	Positive power supply
64	NC	—	—	No connect, leave unconnected[1]

NOTE: (1) No connect (NC) pins must be left unconnected, or floating. Connecting any of these pins to either the positive or negative power supply rails may cause improper operation or failure of the device, or in extreme cases, cause permanent damage to the device.

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Package Information

64-pin PQFP Package Drawing

Item	10 mm	Tol.
A	2.45	MAX
D	2.00	+0.10
E	0.22	±.05
F	13.20	±.25
G	10.00	±.10
H	13.20	±.25
I	10.00	±.10
J	0.88	±.15
K	0.50	BASIC
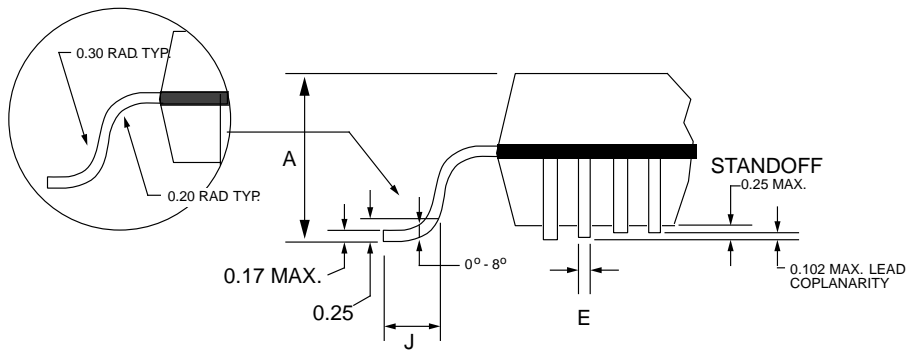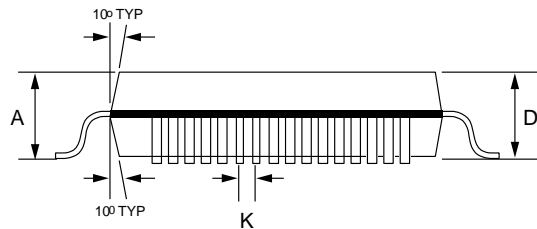
NOTES:
Drawing not to scale.
Heat spreader up on 10mm package only.
All units in mm unless otherwise noted.
Heat spreader is not electrically connected.

Package #: 101-XXX-X
Issue #: 1

Package #: 101-XXX-X
Issue #: 1

Package Thermal Considerations

This package has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in the following table:

Table 9: Thermal Resistance

Symbol	Description	$^oC/W$
θ-jc	Thermal resistance from junction to case.	1.5
θ-ca	Thermal resistance from case to ambient with no airflow, including conduction through the leads.	31.5

Thermal Resistance With Airflow

Shown in the table below is the thermal resistance with airflow. This thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst case power of the device multiplied by the thermal resistance.

Table 10: Thermal Resistance With Airflow

Airflow	θ-ca ($^oC/W$)
100 lfpm	25.8
200 lfpm	23.0
400 lfpm	19.3
600 lfpm	17.0

Maximum Ambient Temperature Without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

θ_{CA} = Theta case to ambient at appropriate airflow
$T_{A(MAX)}$ = Ambient Air temperature
$T_{C(MAX)}$ = Case temperature (85^oC for VSC8122)
$P_{(MAX)}$ = Power (1.2W for VSC8122)

Table 11: Maximum Ambient Air Temperature Without Heatsink

Airflow	$T_{A(MAX)}\ ^oC$
Still air	47.2
100 lfpm	54.0
200 lfpm	57.4
400 lfpm	61.8
600 lfpm	64.6

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

Ordering Information

The order number for this product is formed by a combination of the device number, and package type.

VSC8122 QP

Device Type
VSC8122: OC-3/12/48 (STM-1/4/16)
Clock and Data Recovery

Package Style
QP: 64-pin, 10 x 10 mm PQFP

Notice