



## Advance Product Information VSC8151

2.488Gb/s SONET/SDH  
STS-48/STM-16 Section Terminator

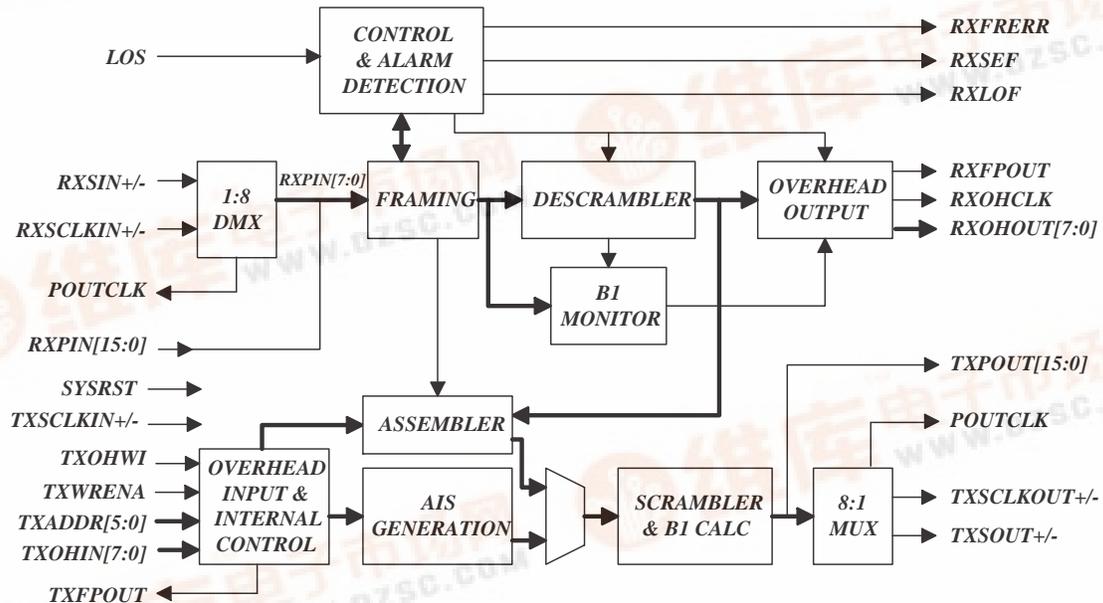
### Features

- Integrated 2.488Gb/s Transceiver
- SONET/SDH Transport Overhead Output
- SONET/SDH Transport Overhead Modification
- B1 Error Detection, Re-calculation, and Insertion
- Support for Multiple SONET/SDH Rates
- LOF/SEF Alarm Generation
- Section & Line AIS Insertion
- 50Ω Source Terminated 2.488Gb/s I/O

### General Description

The VSC8151 is a 2.488Gb/s Section Termination device which both monitors and modifies the section and line overhead of a received SONET/SDH signal, and can generate AIS-L maintenance signals for trouble sectionalization. These features allow all section termination requirements to be supported for Operations, Administration, Management, and Provisioning (OAM&P) functions in SONET/SDH terminal and optical networking applications. An integrated 2.488Gb/s serial transceiver isolates the SONET/SDH signal interface, allowing protocol information to be exchanged with programmable logic using a low-speed TTL interface.

### VSC8151 Functional Block Diagram



NOTE: References (R#-#) or (O#-#) refer to the SONET requirement or option specification listed in Bellcore document GR-253 CORE Issue 2, Rev. 2, January 1999.

### Functional Overview

The VSC8151 is divided into two logic sections, a monitoring section and a modification section, each interfaced externally through both 2.5Gb/s serial interfaces as well as 16-bit parallel interfaces. Incoming

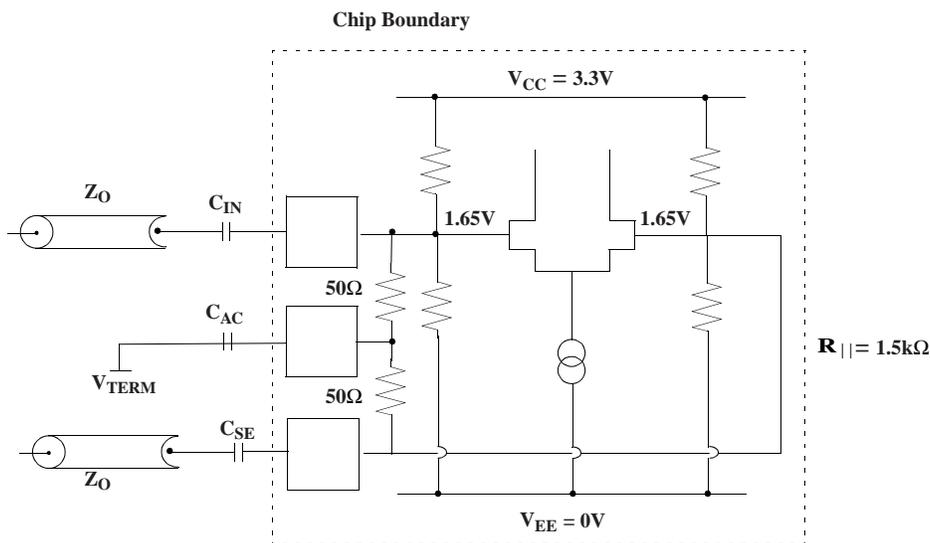
SONET/SDH data is demultiplexed, framed, descrambled, and the 27 bytes of the section and line overhead are output. The BIP parity of the incoming signal is calculated and compared with the received B1 and B2 bytes for calculating received parity errors. The byte aligned data, calculated B1/B2 parity, and frame boundary location are then passed to the modification section where new overhead bytes are inserted. The modified data is rescrambled, and B1/B2 parity recalculated (if desired) prior to serialization and output. An internal state machine generates a section alarm inhibit signal (AIS) with user defined transport overhead that can be alternatively transmitted in place of the received signal.

## 2.5G Serial and Parallel Input Interfaces

The demux receives differential clock and data signals at the appropriate SONET/SDH rate and demultiplexes the data for framing. These inputs are internally terminated by a center-tapped resistor network and include biasing resistors to facilitate AC coupling. For differential input DC coupling, the network is terminated to the appropriate termination voltage  $V_{Term}$  providing a  $50\Omega$  to  $V_{Term}$  termination for both true and complement inputs. For differential input AC coupling, the network is terminated to  $V_{Term}$  via a blocking capacitor.

The common mode reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip resistor divider. The external reference should have a nominal value equivalent to the common mode switch point of the DC coupled signal, and can be connected to either side of the differential gate.

**Figure 1: High Speed Serial Clock and Data Inputs**



$C_{IN}$  TYP = 100 pF (clock), 100nF (data)

$C_{SE}$  TYP = 100 pF (clock), 100nF (data) for single ended applications.

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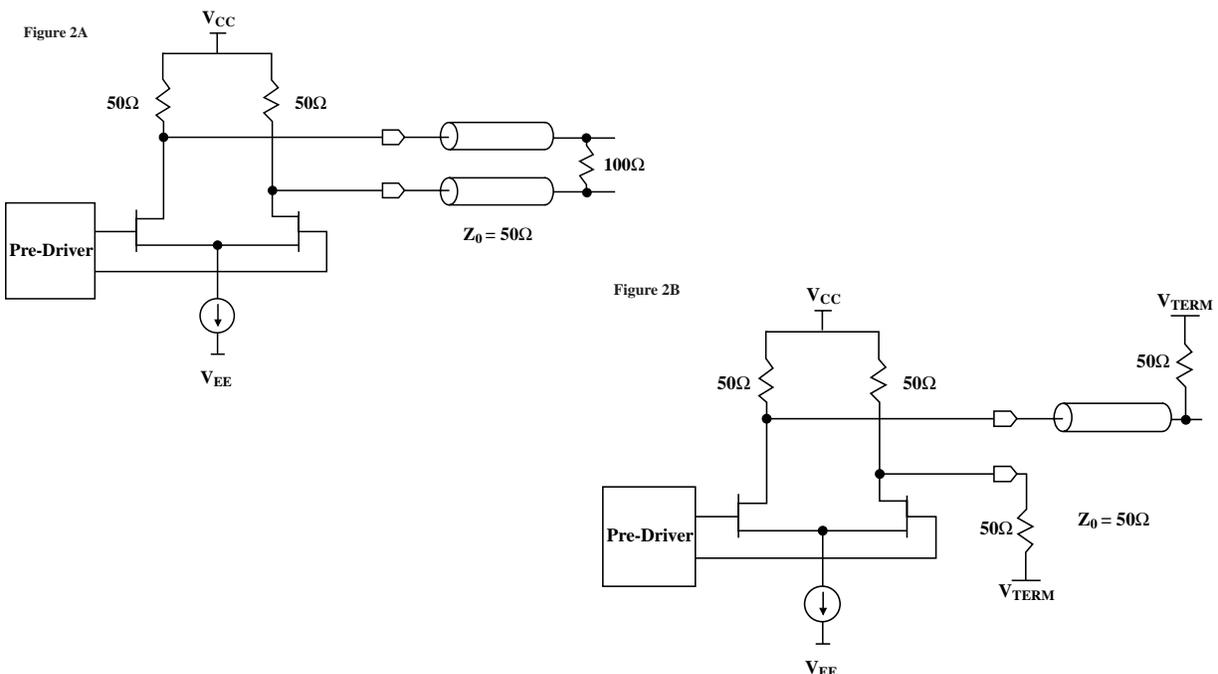
The serial demux can be bypassed and the 16-bit single-ended PECL bus RXPIN[15:0] can be used to input SONET/SDH data for applications where the data has already been deserialized by a previous device. This mode is selected by asserting the EQULOOP input (active high). Input setup and hold requirements are specified with respect to the falling edge of POUTCLK; the user is responsible for meeting loop timing requirements between the VSC8151 and previous device. The user must still provide a line rate clock to the serial clock input RXSLKIN+/- to provide a high-speed output clock to the mux and the means to create the divide-by-16 POUTCLK.

### 2.5G Serial and Parallel Output Interfaces

The high speed clock and data output driver consists of a differential pair designed to drive a 50Ω transmission line. The transmission line should be terminated with a 100Ω resistor at the load between true and complement outputs. No connection to a termination voltage is required. The output driver is source terminated to 50Ω on-chip, providing a snubbing of any reflections. If used single-ended, one way to terminate the output driver is differentially at the load with a 100Ω resistor between true and complement outputs. See Figure 2A. Another option is to terminate the used output at the load with 50 ohm to  $V_{TERM}$  and the unused output with 50 ohm to  $V_{TERM}$  at the source. See Figure 2B.

In some applications, it may be desirable to turn off the high speed outputs (TXSOUT, TXSCLKOUT) to reduce power. To disable the high speed clock output, tie pin 22 to  $V_{CC}$  (3.3V) instead of GND. To disable the high speed data output, tie pin 17 to  $V_{CC}$  (3.3V) instead of GND. Turning off each output will reduce maximum current consumption by 107mA for the clock output, and 122mA for the data output.

Figure 2: High Speed Output Driver & Termination



The serial mux output can be bypassed and the 16-bit single-ended PECL bus TXPOUT[15:0] can be used to output modified SONET/SDH data or AIS to another device. These outputs are enabled by setting the DP bit in the MISC register appropriately, and should be disabled if not being used. It is possible to use both the 16-bit parallel output bus and the 2.5Gb/s serial output simultaneously. The POUTCLK output is used to provide a bus output clock for RXFPOUT and is a divide-by-16 version of TXSCLKIN.

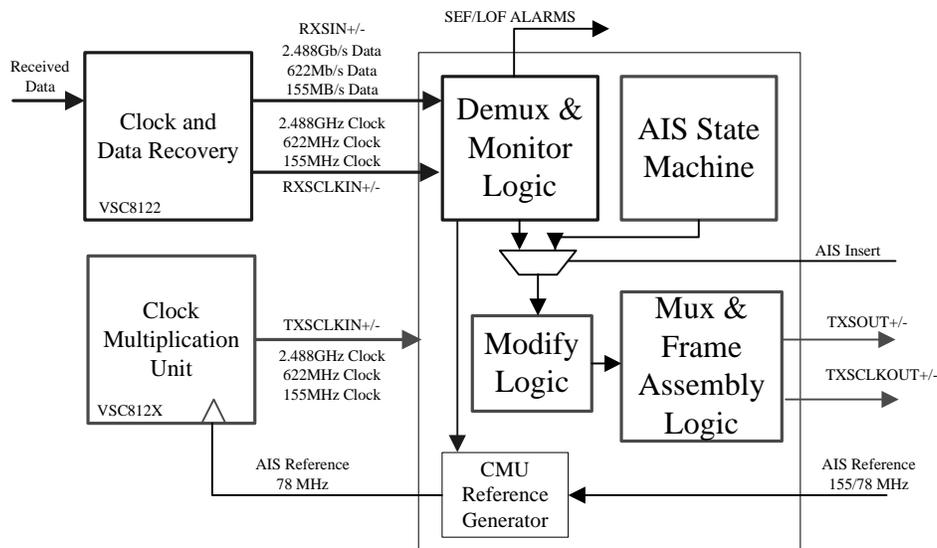
### 2.5G Output Clocking Domains

The 2.5GHz clock input to the VSC8151 mux (TXSCLKIN) acts as the permanent transmit clock for the VSC8151. An internal clock domain boundary exists between the monitor and the transmit sections of the device, allowing the AIS transmit portion to function completely independently of the receive portion. This allows a CDR to track whatever data is being received and allows the VSC8151 to monitor in-frame status of the signal continuously.

During a LOS condition, the CDR clock output may drift outside of the SONET/SDH transmission standard of +/-20PPM. By providing the option of using an external clock multiplication unit (CMU), one can maintain a standard of +/-20PPM even during AIS states. This backup CMU receives its timing reference from either a local AIS reference or the divided clock from the received RXSCLKIN +/-, depending whether AIS transmit mode is selected or not.

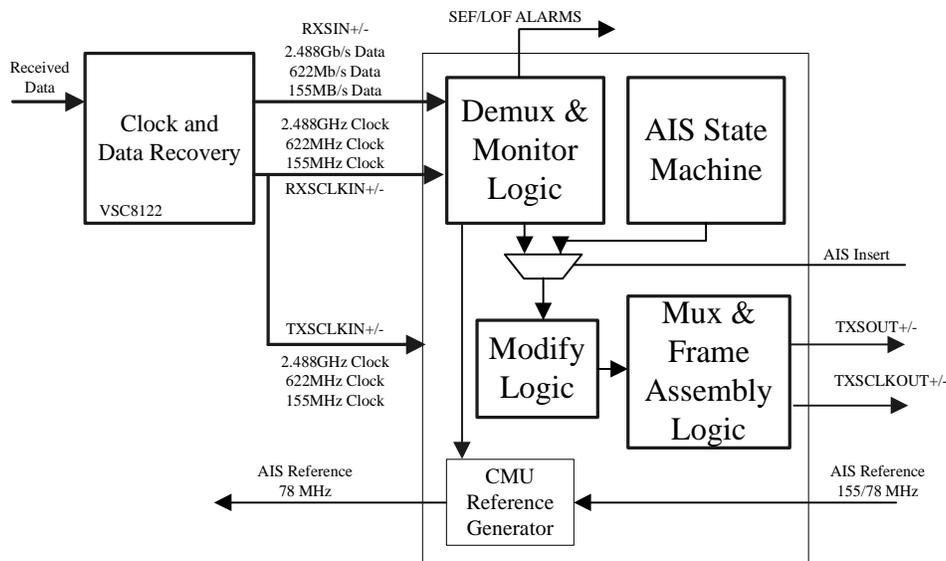
The user controls the source of the reference clock output through settings in the VSC8151 register file. The user will change these settings at the same time AIS is asserted or when imminent loss of RXSCLKIN clock quality exists. The AIS reference output can be switched from a divided down RXSCLKIN signal to a copy of one of the external references, ensuring that a proper reference clock remains for the transmit multiplexer. (See Table 2: VSC8151 Configuration Registers, Definition 13)

**Figure 3: VSC8151 using CMU as Transmit Timing Source**



If the user chooses to use the CDR as a timing source even during AIS mode, the output of the CDR can be connected single ended to both RXSCLKIN and TXSCLKIN, or a multi-drop connection can be made differentially.

**Figure 4: VSC8151 using CDR as Transmit Timing Source**



## SONET/SDH Monitoring Circuitry Overview

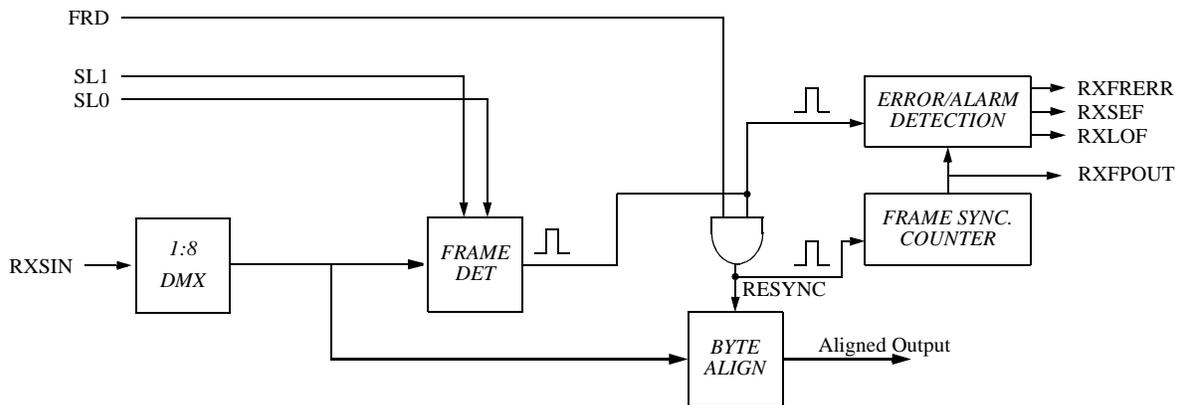
The monitoring circuitry provides SONET/SDH compliant framing and framing alarms, as well as detecting B1 and B2 parity errors and transport overhead byte output.

### Framing

The frame acquisition algorithm determines the in-frame/out-of-frame status of the receiver. Out-of-frame is defined as a state where the frame boundaries of the received SONET/SDH signal are unknown, i.e. after system reset or if for some reason the receiver loses synchronization, e.g. due to 'bit slips'. In-frame is defined as a state where the frame boundaries are known.

The receiver monitors the frame synchronization by checking for the presence of a portion of the A1/A2 framing pattern every 125µs. If one or more bit errors are detected in the expected A1/A2 framing pattern output RXFRERR (active high) will be asserted (See Figure 5). If framing pattern errors are detected for four consecutive frames a Severely Errored Frame (SEF) alarm will be asserted on output RXSEF (active high) (R5-223).

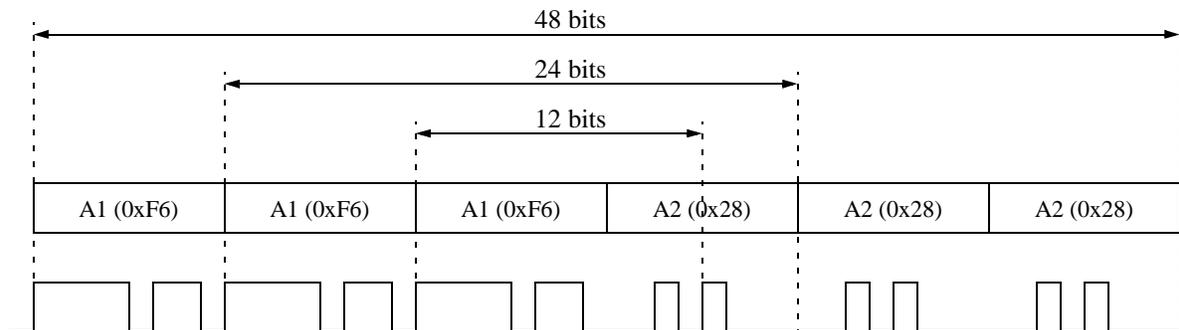
**Figure 5: Functional Block Diagram of Frame Acquisition Circuit**



The frame boundary detection/verification is based on 12, 24 or 48 bits of the A1/A2 overhead (See Figure 6) depending on the setting of the FRDET register (See Table 2). Frame acquisition procedures are controlled by the settings of the FRDET register. Reframing can be controlled manually or reframing can automatically be initiated by the presence of an SEF signal. Using SEF as an indicator that reframe is necessary will achieve realignment within 250uS or the receipt of two error free framing patterns (R5-225)

A frame detect based on 24 bits will result in an SEF alarm at an average of no more than once every 6 minutes assuming a BER of 10<sup>-3</sup> (R5-224). A frame detect based on 48 bits or 12 bits will result in a mean time between SEF detects of 0.43 minutes and 103 minutes respectively.

**Figure 6: Frame Detection Patterns**



### Loss of Signal

The LOS (Loss of Signal, active high) input should be asserted whenever the interfacing module no longer generates a valid electrical signal on the high speed clock and/or data lines of the VSC8151. If the clock signal is present when the LOS input is asserted the VSC8151 will assert SEF and other outputs will become invalid. If the input clock is not present, then the transition of the LOS input will not be detected and the part is effectively frozen. Asserting LOS will force SEF (Severely Errored Frame) and LOF (Loss of Frame) high, and force all 0's to be output from the device, regardless of the input.

#### Loss of Frame

A Loss of Frame (LOF) defect is declared (RXLOF active high) when a Severely Errored Frame (SEF) condition persists for 3ms (R6-59). The LOF state detection is based on an integrating timer to prevent sporadic errors from asserting LOF, such as a periodic 1ms error. An LOF defect is cancelled after an in-frame condition (SEF low) persists for 3ms (R6-61) because an integrating timer approach has been implemented (O6-62).

#### Multiple SONET/SDH Rate Functionality

The VSC8151 supports three SONET/SDH rates: STS-48/STM-16, STS-12/STM-4, and STS-3/STM-1. The user is responsible for rate-provisioning the device by setting the RATESEL register (See Table 2). The device requires clocks RXSCLKIN+/- and TXSCLKIN+/- to match the selected data rate in order for internal circuitry to function correctly. The RATESEL register changes the expected frame length of the received signal and selects the characteristics of the outgoing traffic or AIS signal. LOF integration timing remains 3ms regardless of selected SONET/SDH rate.

#### Descrambler

Framed SONET/SDH bytes are descrambled using a frame synchronous descrambler with generating polynomial  $1 + X^6 + X^7$  and a sequence length of 127. The scrambling algorithm is reset to an all 1's state immediately following the Z0 byte (last channel of first row, third column). The A1, A2, and J0/Z0 bytes are not descrambled (R5-6). The descrambler can be disabled by setting the MISC register appropriately.

#### B1 Error Monitoring

The bit-interleaved parity (BIP-8) error detection code (B1) will be calculated for every received frame before descrambling and compared to the descrambled B1 value in the following frame (R3-16). The results of this calculation are used to generate a B1 parity mask that is output using the overhead output interface. The calculated B1 parity used to do this comparison can be substituted in the received data stream and output. This effectively 'corrects' the B1 byte and prevents the same B1 errors from being detected downstream.

#### B2 Error Monitoring

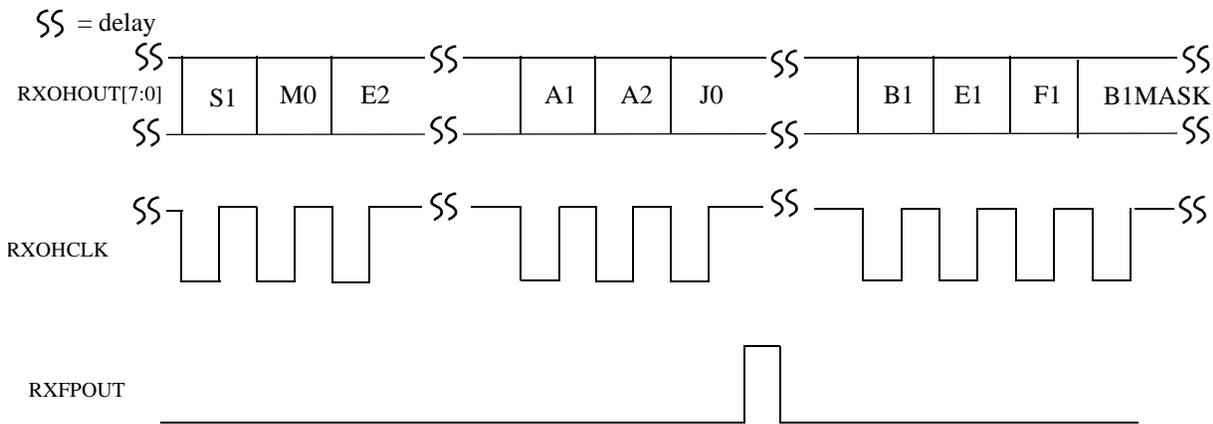
Incoming B2 errors for the first STS-1 are monitored and detected. This circuitry is not designed to supply B2 error rate monitoring but exists to provide support for modification of the overhead bytes of the line overhead. Incoming B2 parity must be determined because modification of the line overhead requires that the B2 byte for the first STS-1 be re-calculated. If the line overhead is not being modified by the user then the B2 error monitoring still takes place and the B2 errormask is output.

#### Overhead Output

The 9 bytes of the SONET section overhead and the 18 bytes in the first channel of the line overhead (See Figure 7) are made available to the user through the overhead output interface RXOHOUT[7:0], RXOHCLK, and RXFPOUT. Two additional bytes containing the results of the B1 and B2 parity error detection are also output. These 29 bytes are output from the RXOHOUT port, each accompanied by a pulse of RXOHCLK. The 27 overhead bytes are output in the order they are received, with a pulse of RXFPOUT appearing after the J0 byte. RXFPOUT is used to provide a reference point for the 29 byte output sequence of overhead bytes and clocks

(See Figure 7). It is suggested that RXOHCLK be used to clock an external counter with RXFPOUT providing a counter reset. This allows the counter value to be correlated to a specific output byte and to be used as a write address for a register file.

**Figure 7: Functional Overhead Output Timing**



The additional two bytes are parity error masks that indicate the number of received B1 and B2 errors. These bytes contain a parity error-mask of the results of the BIP calculation. Incoming parity errors are designated by a '1' in the corresponding bit position. A B1 or B2 error mask byte of 00H indicates no received parity errors for that frame, and a byte of 13H would indicate 3 of 8 bits were errored. The B1 error mask appears immediately after the F1 user byte is output and the B2 error mask appears immediately after the K2 APS byte is output.

The RXOHOUT[7:0] output is undefined when SEF is high. RXFPOUT and RXOHCLK are functions of the received data being properly framed and will also be indeterminate during a SEF or LOS condition.

## SONET/SDH Modification Circuitry Overview

The modification circuitry receives frame aligned data from the monitoring circuitry or from an internal state machine that generates a section AIS signal. The transport overhead of either signal can be modified by the user, including the insertion of recalculated B1 parity. These features encompass the requirements for performing section termination, as well as allowing the modification of line overhead bytes such as K1/K2 and the line DCC bytes.

## Overhead Write Interface

The 9 bytes of the section overhead and the 18 bytes of the first channel of the line overhead can be replaced with user defined bytes or allowed to pass through the part unchanged. The overhead write interface makes use of an internal 32 byte register file for storing the 27 overhead modifier bytes as well as providing internal configuration registers. TXWRENA, TXADDR[5:0], TXOHWI, and TXOHIN[7:0] are the write interface inputs.

Data present on the TXOHIN[7:0] bus is written to the internal register addressed by TXADDR[5:0] on the rising edge of TXWRENA. Assertion of TXOHWI (active high) during the overhead byte write cycle inhibits the modification of the addressed overhead byte.

#### **A1/A2 Boundary Modification**

Only the first A1 and A2 bytes of the SONET/SDH can be modified. The A1 byte can be replaced with user defined data without affecting the framing algorithms of subsequent VSC8151 devices. An F6H byte can be re-substituted before exiting the subsequent VSC8151, effectively creating an in-band 64kb/s messaging channel. The A2 byte could be replaced by the user to intentionally corrupt the A1/A2 boundary and output a data stream that causes downstream network equipment to lose frame lock and enter alarm states.

#### **BIP-8 Recalculation & Modification**

The TXOHIN[7:0] information written to the B1 and B2 address location does not replace the outgoing BIP byte. The 8 bits form an XOR mask that will intentionally induce BIP errors into the outgoing data stream. A TXOHIN[7:0] word such as B2H would corrupt the BIP byte at bits 1, 4, 5, 7, and a downstream device will observe four parity errors. A TXOHIN[7:0] word of 00H will induce no parity errors, but will replace the BIP byte with a recalculated value. Setting the TXOHWI bit at the B1 or B2 location will prevent the BIP byte from being modified or corrected.

Note that if there is any modification to the transport overhead it is necessary for the B1 byte to be corrected in order to prevent downstream parity errors. The B2 byte needs to be corrected if any changes are made to the line overhead for the same reason.

Errors can be intentionally induced to the B2 channel to compensate for the lack of complete B2 error monitoring. Modifying the line overhead requires that the B2 byte in the first STS-1 be corrected, but this has the effect of artificially lowering the observed B2 error rate at subsequent line termination equipment (LTE). Correcting the B2 byte in the first STS-1 position will result in a 1/48th, 1/12th, or 1/3rd reduction depending on the provisioned SONET/SDH rate. Monitoring received B2 errors on the RXOHOUT[7:0] B2 errormask and re-writing this errormask to the B2 address will keep the outgoing B2 error rate consistent with the received B2 error rate.

#### **Alarm Indication Signal (AIS) Overhead Modification**

Transport overhead modification procedures are identical for AIS transmission mode. TXFPOUT is sourced from the frame counters resident within the receive framing circuitry during non-AIS transmission mode. During an AIS condition valid SONET/SDH data is no longer being received, resulting in the part entering a LOF or LOS state. Counters in the receive framing block will be invalid during this time, therefore when AIS is asserted the TXFPOUT signal is sourced from a redundant set of frame counters present within the AIS generation state machine. The frame counters for AIS block are separate from the receive framing circuitry, and as a result the TXFPOUT signal will be in an unknown state during a AIS mode transition, but will become periodic again after 125us. User logic should anticipate a late or early TXFPOUT pulse when switching in and out of AIS mode.

### **Line Overhead Modification**

It is understood that the ability to modify a portion of the line overhead is not permitted in a section termination function. The ability to do so has been included in order to leave such decisions at the users discretion.

### **Scrambler**

The outgoing data bytes are scrambled with a generating polynomial of  $1 + X^6 + X^7$  and sequence length of 127, prior to being multiplexed and output as a serial signal. The A1, A2, and J0/Z0 bytes are not scrambled. The scrambler can be disabled by setting a bit in the MISC configuration register.

### **A1/A2 Boundary Refresh**

The FWAx control in the register file forces the 8151 to re-write the entire A1/A2 boundary and to refresh the F6H and 28H bytes while in frame. This feature allows the device to continue to output a valid A1/A2 boundary if input data suddenly disappears, and AIS has not been initiated. In the event that the incoming data disappears, a valid A1/A2 will still appear in the historical frame boundary location, allowing downstream devices to remain in frame until AIS can be initiated.

### **AIS Generation**

The VSC8151 can be configured to output a section level AIS stream in lieu of passing SONET/SDH data received from the RXSIN and RXSCLKIN inputs. This is typically done during LOS or LOF conditions to relay information about the failure by utilizing the section DCC bytes and keep the downstream sections in-frame and monitored while fault isolation to takes place.

Setting the AISMODE configuration register replaces the received data stream with an internally generated AIS-L signal appropriate for section terminating equipment. This signal contains user-defined section overhead and an all-1's pattern for the remainder of the bytes (*R6-163*), conveniently generating AIS for all higher SONET/SDH alarm levels. The section and line overhead bytes can be modified during AIS in the same manner that they may in a non-AIS mode.

During the AIS state, the relative A1/A2 boundary can be preserved so that downstream devices will not be forced to reframe on a new signal. By using the A1/A2 boulder refresh (previous paragraph), the user can initiate a seamless AIS transition without forcing downstream nodes to enter SEF and frame search state.

### **Initialization & Configuration**

Upon power up of the VSC8151, the user should apply a positive pulse to the system reset pin (SYSRST) for at least 32 high speed (2.4GHz) clock cycles (12.8ns). Pulsing SYSRST resets all the counters, synchronizers and state machines used by the 8151.

The device must also be configured upon startup by properly setting the TEST, RATE\_SEL, FRMDET, AIS\_MODE, and MISC registers (See Table 2) using the overhead write interface. TEST must be initialized to an 00H pattern for proper operation. The TXOHWI bit should be set appropriately for all 27 overhead modification registers. No default state exists for all configuration and overhead registers, they must be initialized upon startup. The PT bit of the MISC register has the effect of making the VSC8151 non-intrusive and function as if in a monitor only mode by internally asserting all TXOHWI bits.

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**Table 1: VSC8151 Register File Mapping**

Register Name	Address TXOHA[4:0]	Data & Overhead Write Inhibit TXOHD[7:0], OHWI
OHS0	5h00	SONET #1 STS-1 A1 Modifier
OHS1	5h01	SONET #1 STS-1 A2 Modifier
OHS2	5h02	SONET #1 STS-1 J0 Modifier
OHS3	5h03	B1 Error Mask
OHS4	5h04	SONET #1 STS-1 E1 Modifier
OHS5	5h05	SONET #1 STS-1 F1 Modifier
OHS6	5h06	SONET #1 STS-1 D1 Modifier
OHS7	5h07	SONET #1 STS-1 D2 Modifier
OHS8	5h08	SONET #1 STS-1 D3 Modifier
OHL0	5h09	SONET #1 STS-1 H1 Modifier
OHL1	5h0A	SONET #1 STS-1 H2 Modifier
OHL2	5h0B	SONET #1 STS-1 H3 Modifier
OHL3	5h0C	B2 Error Mask
OHL4	5h0D	SONET #1 STS-1 K1 Modifier
OHL5	5h0E	SONET #1 STS-1 K2 Modifier
OHL6	5h0F	SONET #1 STS-1 D4 Modifier
OHL7	5h10	SONET #1 STS-1 D5 Modifier
OHL8	5h11	SONET #1 STS-1 D6 Modifier
OHL9	5h12	SONET #1 STS-1 D7 Modifier
OHL10	5h13	SONET #1 STS-1 D8 Modifier
OHL11	5h14	SONET #1 STS-1 D9 Modifier
OHL12	5h15	SONET #1 STS-1 D10 Modifier
OHL13	5h16	SONET #1 STS-1 D11 Modifier
OHL14	5h17	SONET #1 STS-1 D12 Modifier
OHL15	5h18	SONET #1 STS-1 S1 Modifier
OHL16	5h19	SONET #1 STS-1 M0/1 Modifier
OHL17	5h1A	SONET #1 STS-1 E2 Modifier

**Table 2: VSC8151 Configuration Registers**

Register Name	Address TXOHA[4:0]	Data ( TXOHD[7:0] )							
		7	6	5	4	3	2	1	0
TEST	5h1B	0	0	0	0	0	0	0	0
RATE_SEL	5h1C	X	X	X	X	FWAx	NS	OC12	OC3
FRMDET	5h1D	X	X	X	X	FRD1	FRD0	SL1	SL0
AIS_MODE	5h1E	X	X	X	X	MXC1	MXC0	B2G	AIS
MISC	5h1F	X	X	X	X	DS	DD	PT	DP

Note: TEST register must be initialized to 00H

### Configuration Register Definitions

1. OC12 | OC3 Multi-rate configuration control
 

0   0	=	STS-48 / STM-16 Mode
0   1	=	STS-3 / STM-1 Mode
1   0	=	STS-12 / STM4 Mode
1   1	=	Invalid
  
2. FRD0      Allows manual control of framing behavior. FRD0 state controls whether the device is actively searching for a frame boundary. Manual control will only function if FRD1 is set to a '1'.
 

0	=	Do not perform frame boundary acquisition
1	=	Attempt frame boundary acquisition
  
3. FRD1      Determines whether reframing is automatically performed or controlled by the setting of the FRD0 register. Automatic reframing uses the status of the SEF output to determine whether reframing needs to take place, forcing frame acquisition as long as SEF is detected.
 

0	=	Frame acquisition is performed upon detection of SEF
1	=	Frame Acquisition is controlled manually
  
4. SL1 | SL0   Controls detection width of A1/A2 boundary
 

0   0	=	Search for 12 bit pattern: h'F62
0   1	=	Search for 48 bit pattern: h'F6F6F6282828
1   0	=	Search for 24 bit pattern: h'F6F628
1   1	=	Do not search for start of frame.
  
5. AIS      AIS Insertion mode
 

0	=	Retransmit received data
1	=	Replace received data with internally generated AIS
  
6. B2G      =      In AIS mode if this bit is set to a "1", B2 calculation on #1 STS-1 frame is performed. If this bit is set to "0", the B2 field of the #1 STS-1 AIS frame is set to 8'hFF.
  
7. DP      Disable 16-bit PECL output bus RXPOUT[15:0]. The user should leave these outputs un-terminated to reduce power consumption and noise if they are disabled.
 

0	=	Enable RXPOUT[15:0]
1	=	Disable RXPOUT[15:0].
  
8. PT      Pass Through Mode.
 

0	=	Normal Operation
1	=	Disable modification of overhead bytes & BIP recalculation

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9. DD      Disable descrambling  
                  0      =      Normal Operation  
                  1      =      Disable descrambling of incoming data
10. DS      Disable scrambling  
                  0      =      Normal Operation  
                  1      =      Disable scrambling of outgoing data
11. NS      Non-SONET: Allows device to pass non-SONET data such as Gigabit Ethernet. *NOTE: If non-SONET data is being transmitted, Frame Detect must be disabled. (When NS="1", set FRD1="1" and FRD0="0").*  
                  0      =      SONET data transmitted  
                  1      =      non-SONET data transmitted
12. FWAx    Forced write of A1/A2 boundary. FWAx = "1" forces all A1 and A2 to be re-written (as described in the **A1/A2 boundary refresh section**)  
                  0      =      Normal Operation  
                  1      =      Forced re-write of A1/A2
13. MXC[1:0] VSC8151 CMU reference generator output clock selection (see Figure 3)

<i>MXC1</i>	<i>MXC0</i>	<i>CKREFP/N, CKREFT Reference Generator Outputs</i>
0	0	CMU Ref Gen Outputs = Referenced from RXSCLKIN/32 (Transport Mode)
0	1	CMU Ref Gen Outputs = Referenced from external 77MHz PECL AIS Refclk (I_RCAIS)
1	0	CMU Ref Gen Outputs = Referenced from external 155MHz PECL AIS Refclk (I_RCAIS)
1	1	CMU Ref Gen Outputs = Based off external TTL AIS Refclk (I_RCVCO) 77MHz

## AC Timing Characteristics

Figure 8: Overhead Output Timing Diagram

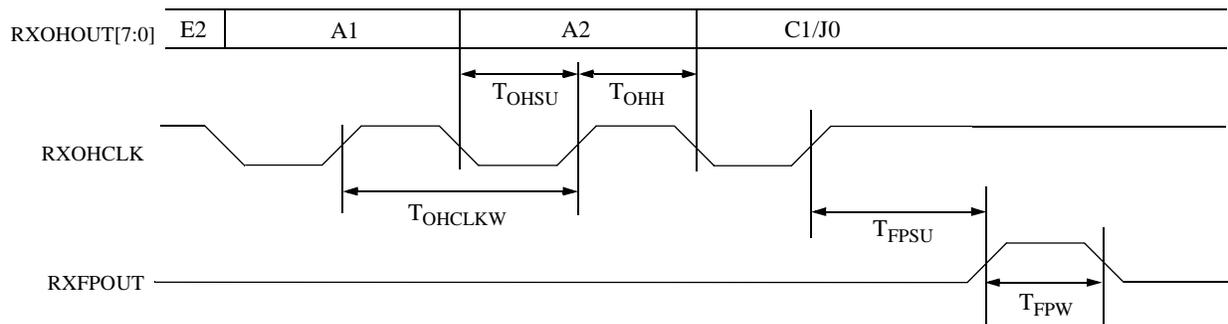


Table 3: Overhead Output Timing (STS-48/STM-16 Mode)

Parameter	Description	Min	Typ	Max	Units
$T_{OHSU}$	Overhead output setup time with respect to RXOHCLK	70.5	—	—	ns
$T_{OHH}$	Overhead output hold time with respect to RXOHCLK	70.5	—	—	ns
$T_{OHCLKW}$	Overhead output clock period	—	154	—	ns
$T_{FPSU}$	Frame pulse setup time with respect to RXOHCLK	88	—	—	ns
$T_{FPW}$	Frame pulse width	51.34	—	51.44	ns

Note: Generated Waveforms are synchronous and assume a 2.488GHz RXSCLKIN signal.

Table 4: Overhead Output Timing (STS-12/STM-4 Mode)

Parameter	Description	Min	Typ	Max	Units
$T_{OHSU}$	Overhead output setup time with respect to RXOHCLK	73.5	—	—	ns
$T_{OHH}$	Overhead output hold time with respect to RXOHCLK	73.5	—	—	ns
$T_{OHCLKW}$	Overhead output clock period	—	154	—	ns
$T_{FPSU}$	Frame pulse setup time with respect to RXOHCLK	104	—	—	ns
$T_{FPW}$	Frame pulse width	51.34	—	51.44	ns

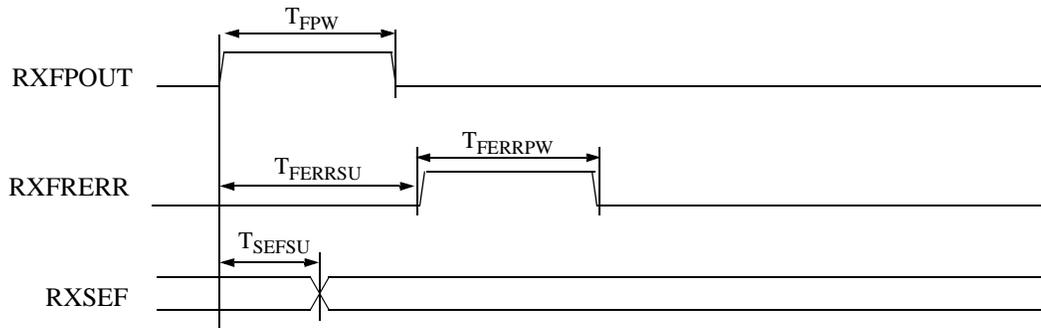
Note: Generated Waveforms are synchronous and assume a 622MHz RXSCLKIN signal.

Table 5: Overhead Output Timing (STS-3/STM-1 Mode)

Parameter	Description	Min	Typ	Max	Units
$T_{OHSU}$	Overhead output setup time with respect to RXOHCLK	102	—	—	ns
$T_{OHH}$	Overhead output hold time with respect to RXOHCLK	102	—	—	ns
$T_{OHCLKW}$	Overhead output clock period	—	154	—	ns
$T_{FPSU}$	Frame pulse setup time with respect to RXOHCLK	155	—	—	ns
$T_{FPW}$	Frame pulse width	51.34	—	51.44	ns

Note: Generated Waveforms are synchronous and assume a 155MHz RXSCLKIN signal.

**Figure 9: Framing and B1 Error Output Timing**



Note: Waveforms not to scale

**Table 6: Framing and B1 Error Output Timing (STS-48/STM-16 Mode)**

Parameter	Description	Min	Typ	Max	Units
$T_{FPW}$	Frame Pulse Width	—	51.4	—	ns
$T_{FERRSU}$	Frame Boundary Error delay with respect to RXFPOUT	—	61.2	—	ns
$T_{FERRPW}$	Frame Boundary Error pulse width high	—	25.7	—	ns
$T_{SEFSU}$	SEF transition delay time with respect to RXFPOUT	—	48.3	—	ns

Note: Generated Waveforms are synchronous and assume a 2.488GHz RXSCLKIN signal.

**Table 7: Framing and B1 Error Output Timing (STS-12/STM-4 Mode)**

Parameter	Description	Min	Typ	Max	Units
$T_{FPW}$	Frame Pulse Width	—	51.4	—	ns
$T_{FERRSU}$	Frame Boundary Error delay with respect to RXFPOUT	—	64.4	—	ns
$T_{FERRPW}$	Frame Boundary Error pulse width high	—	51.4	—	ns
$T_{SEFSU}$	SEF transition delay time with respect to RXFPOUT	—	51.4	—	ns

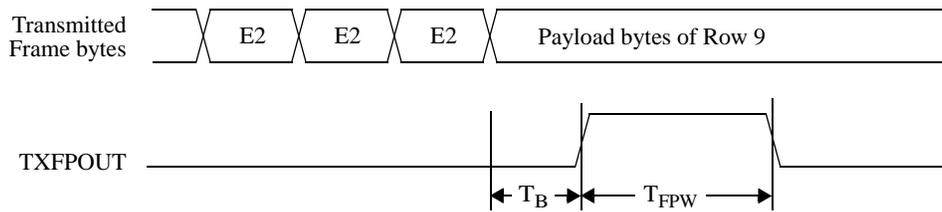
Note: Generated Waveforms are synchronous and assume a 622MHz RXSCLKIN signal.

**Table 8: Framing and B1 Error Output Timing (STS-3/STM-1 Mode)**

Parameter	Description	Min	Typ	Max	Units
$T_{FPW}$	Frame Pulse Width	—	51.4	—	ns
$T_{FERRSU}$	Frame Boundary Error delay with respect to RXFPOUT	—	0	—	ns
$T_{FERRPW}$	Frame Boundary Error pulse width high	—	51.4	—	ns
$T_{SEFSU}$	SEF transition delay time with respect to RXFPOUT	—	103	—	ns

Note: Generated Waveforms are synchronous and assume a 155MHz RXSCLKIN signal.

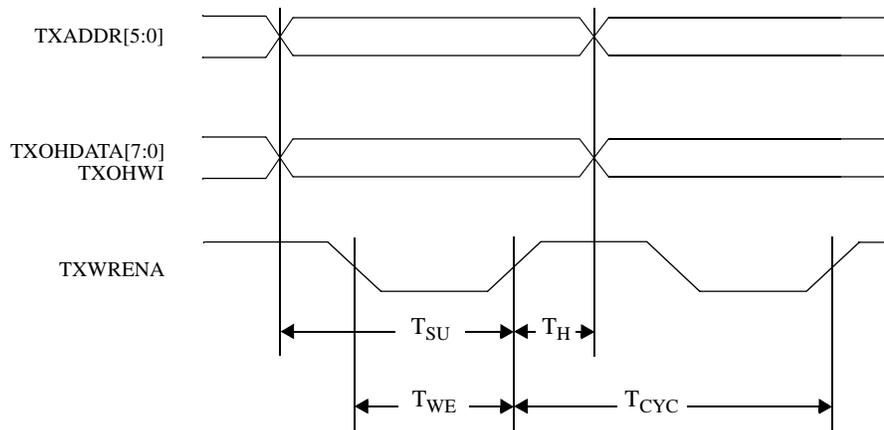
**Figure 10: Transmit Frame Pulse Timing Diagram**



**Table 9: Transmit Frame Pulse Timing**

Parameter	Description	Min	Typ	Max	Units
$T_{FPW}$	Transmit Frame Pulse Width	—	51.2	—	ns
$T_B$ (OC-48)	Transmitted Byte Cycle Time	—	3.2	—	ns
$T_B$ (OC-12)	Transmitted Byte Cycle Time	—	12.8	—	ns
$T_B$ (OC-3)	Transmitted Byte Cycle Time	—	51.2	—	ns

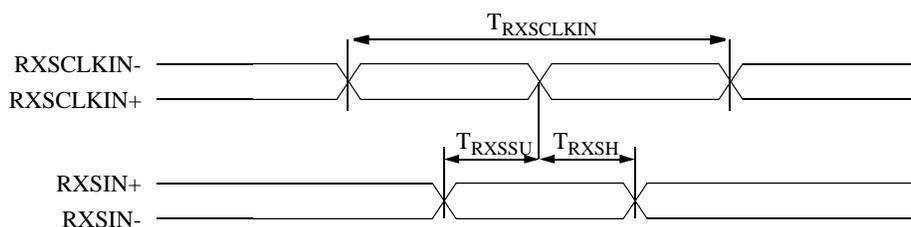
**Figure 11: On Chip Register File Access Port Timing Diagram**



**Table 10: On Chip Register File Access Port Timing**

Parameter	Description	Min	Typ	Max	Units
$T_{SU}$	Setup time for data/address	50	—	—	ns
$T_H$	Hold time for data/address	50	—	—	ns
$T_{WE}$	Write enable low	50	—	—	ns
$T_{CYC}$	Write cycle time	375	—	—	ns

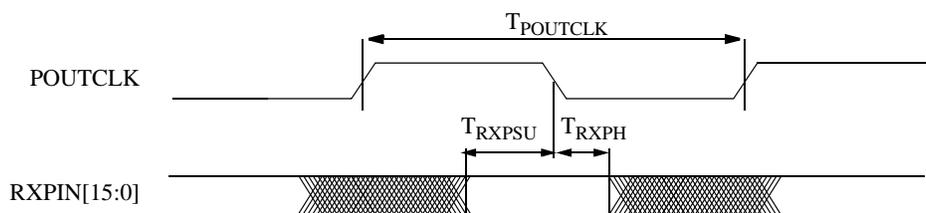
**Figure 12: Serial Data Input Timing Diagram**



**Table 11: Serial Data Input Timing**

Parameter	Description	Min	Typ	Max	Units
$T_{RXSCLKIN}$	Serial Receive clock period	401.9	—	—	ps
$T_{RXSSU}$	Serial Receive input data RXSIN setup time with respect to falling edge of RXSCLKIN+	100	—	—	ps
$T_{RXSH}$	Serial Receive input data RXSIN hold time with respect to falling edge of RXSCLKIN+	75	—	—	ps

**Figure 13: Parallel Data Input Timing Diagram**

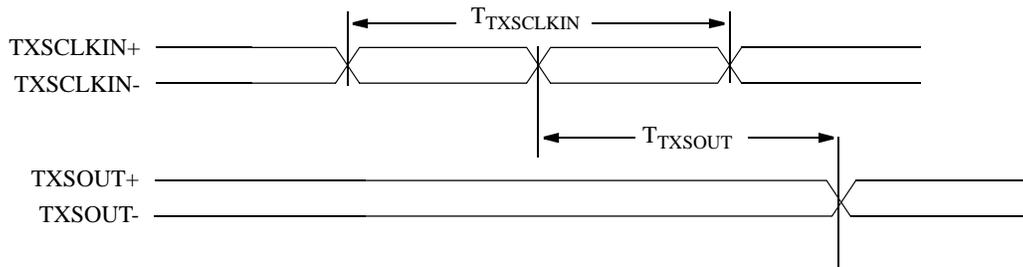


**Table 12: Parallel Data Input Timing**

Parameter	Description	Min	Typ	Max	Units
$T_{POUTCLK}$	Parallel output clock period	103.2	—	6.45	ns
$T_{RXPSU}$	Parallel receive input data RXPIN setup time with respect to falling edge of POUTCLK output	2.4	—	—	ns
$T_{RXPH}$	Parallel receive input data RXPIN hold time with respect to falling edge of POUTCLK output	1.0	—	—	ns

Note: Parallel output clock is synchronously generated 50/50 1/16th the frequency of the serial clock input (RXSCLKIN)

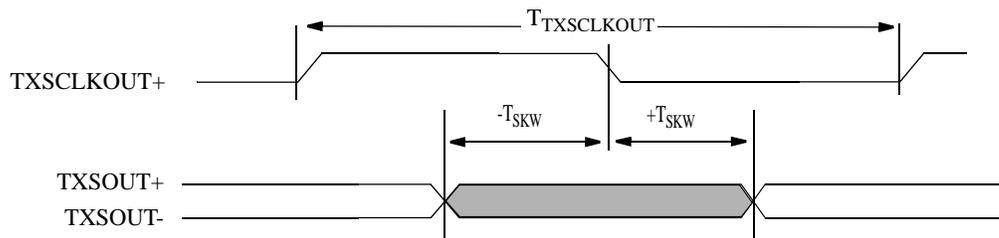
**Figure 14: Serial Data Output Timing Diagram**



**Table 13: Serial Data Output Timing**

Parameter	Description	Min	Typ	Max	Units
$T_{TXSCLKIN}$	Serial Receive clock period	401.9	—	—	ps
$T_{TXSOUT}$	Propagation delay from rising edge of TXSCLKIN+/- to output edge of TXSOUT+/-	430	—	630	ps

**Figure 15: Serial Data Output Timing Skew**



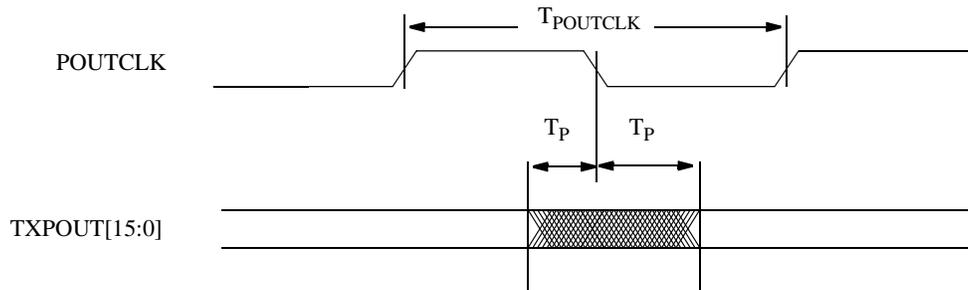
**Table 14: Serial Data Output Skew**

Parameter	Description	Min	Typ	Max	Units
$T_{TXSCLKOUT}$	Serial transmit clock period	401.9	—	—	ps
$T_{TSKW}$	Propagation delay from falling edge of TXSCLKOUT+ to output edge of TXSOUT+/-	—	—	100	ps

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**Figure 16: Parallel Data Output Timing Diagram**



**Table 15: Parallel Data Output Timing**

<i>Parameter</i>	<i>Description</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>
$T_{POUTCLK}$	Parallel output clock period	103.2	—	6.45	ns
$T_P$	Propagation delay from falling edge of POUTCLK to output edge of TXPOUT[15:0]	-500	—	500	ps

*Note: Parallel output clock is synchronously generated 50/50 1/16th the frequency of the serial clock input (RXSCLKIN)*

## DC Characteristics

**Table 16: High-Speed Differential Inputs and Outputs (HSPECL)**

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{ODATA}$	Data Output differential voltage (Peak to Peak, Single-ended)	550	—	1200	mV	Load = 100 Ohms across TXSOUT+/- at load
$V_{OCLK}$	Clock Output differential voltage (Peak to Peak, Single-ended)	450	—	1200	mV	Load = 100 Ohms across TXCLKOUT+/- at load
$V_{OCM}$	Output common-mode voltage	2100	—	3000	mV	Load = 100 Ohms across diff pair
$R_O$	Output Impedance	40	—	60	ohms	Guaranteed, not tested.
$V_{ID}$	Input differential voltage	450	—	—	mV	AC Coupled, internally biased to VTTL/2

**Table 17: Low-Speed Parallel LVPECL Inputs and Outputs**

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH voltage	$V_{TTL}-1020$	—	$V_{TTL}-700$	mV	—
$V_{OL}$	Output LOW voltage	$V_{TTL}-2000$	—	$V_{TTL}-1620$	mV	—
$V_{IH}$	Input HIGH voltage	$V_{TTL}-1165$	—	$V_{TTL}-700$	mV	—
$V_{IL}$	Input LOW voltage	$V_{TTL}-2000$	—	$V_{TTL}-1475$	mV	—
$I_{IH}$	Input HIGH current	—	—	200	$\mu A$	$V_{IN} = V_{IH} (max)$
$I_{IL}$	Input LOW current	-50	—	—	$\mu A$	$V_{IN} = V_{IL} (min)$

Note: (1) External Reference ( $V_{REF}$ ) =  $V_{TTL} - 1.32V \pm 25mV$ .

(2) Load =  $50\Omega$  to  $V_{TTL} - 2.0V$ .

(3) External VREF current is  $50\mu A$  per Input.

**Table 18: TTL Inputs and Outputs**

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH voltage	2.4	—	—	V	$I_{OH} = -8mA$
$V_{OL}$	Output LOW voltage	0	—	0.4	V	$I_{OL} = 8mA$
$V_{IH}$	Input HIGH voltage	2.0	—	$V_{TTL} + 1.0V$	V	—
$V_{IL}$	Input LOW voltage	0	—	0.8	V	—
$I_{IH}$	Input HIGH current	-	—	500	$\mu A$	$V_{IN} = 2.4V$
$I_{IL}$	Input LOW current	-50	—	—	$\mu A$	$V_{IN} = 0.4V$

**Table 19: Power Supply Currents (+2V/+3.3V Supplies, Outputs Open)**

Parameter	Description	(Max)	Units
$I_{TTL}$	Power supply current from $V_{TTL}$	380	mA
$I_{MM}$	Power supply current from $V_{MM}$	1100	mA
$P_D$	Power dissipation	3.6	W

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### Absolute Maximum Ratings

Power Supply Voltage ( $V_{CC}$ ) Potential to GND .....	-0.5 V to +4.3 V
Power Supply Voltage ( $V_{MM}$ ) Potential to GND .....	-0.5 V to +3.0 V
TTL Input Voltage Applied .....	-0.5 V to + 5.5V
ECL Input Voltage Applied .....	+0.5 V to $V_{TT}$ -0.5 V
Output Current ( $I_{OUT}$ ).....	50 mA
Case Temperature Under Bias ( $T_C$ ) .....	-55° to + 125°C
Storage Temperature ( $T_{STG}$ ) .....	-65° to + 150°C

*Note: Caution: Stresses listed under “Absolute Maximum Ratings” may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.*

### Recommended Operating Conditions

Power Supply Voltages ( $V_{CC}$ ).....	+3.3V ±5 %
Power Supply Voltages ( $V_{MM}$ ).....	+2.0V ±5 %
Commercial Operating Temperature Range* ( $T$ ).....	0° to 85°C

*Notes: (1)Lower limit of specification is ambient temperature and upper limit is case temperature.  
(2)Customer must use air cooled/heatsink environment to meet thermal requirements of the package.  
(3)Suggested power up of 8151 is +2.0V supply first, then +3.3V supply.*

### ESD Ratings

Proper ESD procedures should be used when handling this product. The VSC8151 is rated to the following ESD voltages based on the human body model:

1. All pins are rated at or above 1500V.

## Package Pin Descriptions

Table 20: Pin Identification

Signal	Pin	I/O	Level	Pin Description
VREF	1	PWR	+1.98V	PECL Input reference. No connect if RXPIN[15:0] is not used.
VCC	2	PWR	+3.3V	
VEE	3	PWR	GND	
VMM	4	PWR	+2.0V	
NC	5	—	—	Leave Unconnected
CKREFP	6	O	PECL	Output Clock for external AIS CMU (true)
CKREFN	7	O	PECL	Output Clock for external AIS CMU (complement)
VTERM (RXSCLKIN)	8	I	0 -> 3.3V	High Speed Clock Input Termination Voltage (Demux)
VCC	9	PWR	+3.3V	
VCC	10	PWR	+3.3V	
VEE	11	PWR	GND	
VEE	12	PWR	GND	
VCC	13	PWR	+3.3V	
TXSOUT -	14	O	HSECL	Serial Data Output, complement
VCC	15	PWR	+3.3V	2.5Gb/s PECL Output Driver Supply Pin
TXSOUT +	16	O	HSECL	Serial Data Output, true
DOPWR	17	I	GND / +3.3V	Serial data output power down (tie to V <sub>CC</sub> to power down, GND otherwise)
VCC	18	PWR	+3.3V	2.5Gb/s PECL Output Driver Supply Pin
TXSCLKOUT-	19	O	HSECL	Serial Clock Output, complement
TXSCLKOUT+	20	O	HSECL	Serial Clock Output, true
VCC	21	PWR	+3.3V	
CLKOPWR	22	I	GND / +3.3V	Serial clock output power down (tie to V <sub>CC</sub> to power down, GND otherwise)
VCC	23	PWR	+3.3V	2.5Gb/s PECL Output Driver Supply Pin
RXSCLKIN +	24	I	HSECL	Serial Clock Input for Demux, true
RXSCLKIN -	25	I	HSECL	Serial Clock Input For Demux, complement
VEE	26	PWR	GND	
TXSCLKIN-	27	—	—	Serial Clock Input for Mux, complement
TXSCLKIN+	28	—	—	Serial Clock Input for Mux, true
RXSIN +	29	I	HSECL	Serial Data Input, true
RXSIN -	30	I	HSECL	Serial Data Input, complement
VTERM (TXSCLKIN)	31	I	0 -> 3.3V	High Speed Clock Input Termination Voltage (for Mux)
VTERM (RXSIN)	32	I	0 -> 3.3V	High Speed Data Input Termination Voltage

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**Table 20: Pin Identification**

<i>Signal</i>	<i>Pin</i>	<i>I/O</i>	<i>Level</i>	<i>Pin Description</i>
NC	33	—	—	Leave Unconnected
NC	34	—	—	Leave Unconnected
NC	35	—	—	Leave Unconnected
NC	36	—	—	Leave Unconnected
VMM	37	PWR	+2.0V	
VEE	38	PWR	GND	
VCC	39	PWR	+3.3V	
EQULOOP	40	I	TTL	RXPIN[15:0] parallel bus input enable. Tie low to use serial input
NC	41	—	—	Leave Unconnected
NC	42	—	—	Leave Unconnected
RXPIN15	43	I	PECL	16 bit PECL input bus
RXPIN14	44	I	PECL	16 bit PECL input bus
RXPIN13	45	I	PECL	16 bit PECL input bus
RXPIN12	46	I	PECL	16 bit PECL input bus
RXPIN11	47	I	PECL	16 bit PECL input bus
RXPIN10	48	I	PECL	16 bit PECL input bus
VCC	49	PWR	+3.3V	
VMM	50	PWR	+2.0V	
RXPIN9	51	I	PECL	16 bit PECL input bus
RXPIN8	52	I	PECL	16 bit PECL input bus
VEE	53	PWR	GND	
RXPIN7	54	I	PECL	16 bit PECL input bus
RXPIN6	55	I	PECL	16 bit PECL input bus
VMM	56	PWR	+2.0V	
RXPIN5	57	I	PECL	16 bit PECL input bus
RXPIN4	58	I	PECL	16 bit PECL input bus
VMM	59	PWR	+2.0V	
RXPIN3	60	I	PECL	16 bit PECL input bus
RXPIN2	61	I	PECL	16 bit PECL input bus
VCC	62	PWR	+3.3V	
RXPIN1	63	I	PECL	16 bit PECL input bus
RXPIN0	64	I	PECL	16 bit PECL input bus
VMM	65	PWR	+2.0V	
NC	66	—	—	Leave Unconnected
RXFPOUT	67	O	TTL	Received Frame Pointer (Pulse High)
VEE	68	PWR	GND	
SEF	69	O	TTL	Severely Errored Frame Indicator (Active High)
RXOHCLK	70	O	TTL	Receive Overhead Output Clock

**Table 20: Pin Identification**

<i>Signal</i>	<i>Pin</i>	<i>I/O</i>	<i>Level</i>	<i>Pin Description</i>
VEE	71	PWR	GND	
VCC	72	PWR	+3.3V	
I_RCVCO	73	I	TTL	TTL Reference Input (Set with MXC[1:0]) (77MHz)
NC	74	—	—	Leave Unconnected
I_RCAIS	75	I	PECL	PECL Reference Input (Set with MXC[1:0])
NC	76	—	—	Leave Unconnected
NC	77	—	—	Leave Unconnected
NC	78	—	—	Leave Unconnected
NC	79	—	—	Leave Unconnected
NC	80	—	—	Leave Unconnected
LOS	81	I	TTL	Loss of Signal
VCC	82	PWR	+3.3V	
VEE	83	PWR	GND	
VMM	84	PWR	+2.0V	
VCC	85	PWR	+3.3V	
VEE	86	PWR	GND	
RXFRERR	87	O	TTL	Received Frame Error
TXFP0UT	88	O	TTL	Transmit Frame Pointer
RXOH0UT4	89	O	TTL	Received Overhead Bus
RXOH0UT5	90	O	TTL	Received Overhead Bus
RXOH0UT6	91	O	TTL	Received Overhead Bus
RXOH0UT7	92	O	TTL	Received Overhead Bus
RXOH0UT0	93	O	TTL	Received Overhead Bus
RXOH0UT1	94	O	TTL	Received Overhead Bus
VEE	95	PWR	GND	
RXOH0UT2	96	O	TTL	Received Overhead Bus
RXOH0UT3	97	O	TTL	Received Overhead Bus
VCC	98	PWR	+3.3V	
LOF	99	O	TTL	Loss of Frame
CKREFT	100	O	TTL	Output Clock for external AIS CMU (Set with MXC[1:0])
NC	101	—	—	Leave Unconnected
TXP0UT15	102	O	PECL	16 bit PECL output bus
VCC	103	PWR	+3.3V	
TXP0UT14	104	O	PECL	16 bit PECL output bus
TXP0UT13	105	O	PECL	16 bit PECL output bus
VCC	106	PWR	+3.3V	
TXP0UT12	107	O	PECL	16 bit PECL output bus
NC	108	—	—	Leave Unconnected

## Advance Product Information

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**Table 20: Pin Identification**

<i>Signal</i>	<i>Pin</i>	<i>I/O</i>	<i>Level</i>	<i>Pin Description</i>
TXADDR0	109	I	TTL	TX Regfile Address
TXADDR1	110	I	TTL	TX Regfile Address
TXADDR2	111	I	TTL	TX Regfile Address
TXADDR3	112	I	TTL	TX Regfile Address
TXWRENA	113	I	TTL	TX Regfile Write Enable
TXADDR4	114	I	TTL	TX Regfile Address Input
VMM	115	PWR	+2.0V	
VCC	116	PWR	+3.3V	
VMM	117	PWR	+2.0V	
VEE	118	PWR	GND	
VCC	119	PWR	+3.3V	
TXOHWI	120	I	TTL	TX Regfile Write Inhibit
TXOHIN7	121	I	TTL	TX Regfile Data Input
TXOHIN6	122	I	TTL	TX Regfile Data Input
TXOHIN5	123	I	TTL	TX Regfile Data Input
TXOHIN4	124	I	TTL	TX Regfile Data Input
TXOHIN3	125	I	TTL	TX Regfile Data Input
TXOHIN2	126	I	TTL	TX Regfile Data Input
TXOHIN1	127	I	TTL	TX Regfile Data Input
TXOHIN0	128	I	TTL	TX Regfile Data Input
VCC	129	PWR	+3.3V	
VCC	130	PWR	+3.3V	
TXPOUT11	131	O	PECL	16 bit PECL output bus
TXPOUT10	132	O	PECL	16 bit PECL output bus
VEE	133	PWR	GND	
TXPOUT9	134	O	PECL	16 bit PECL output bus
TXPOUT8	135	O	PECL	16 bit PECL output bus
VMM	136	PWR	+2.0V	
TXPOUT7	137	O	PECL	16 bit PECL output bus
TXPOUT6	138	O	PECL	16 bit PECL output bus
VCC	139	PWR	+3.3V	
TXPOUT5	140	O	PECL	16 bit PECL output bus
TXPOUT4	141	O	PECL	16 bit PECL output bus
VCC	142	PWR	+3.3V	
TXPOUT3	143	O	PECL	16 bit PECL output bus
TXPOUT2	144	O	PECL	16 bit PECL output bus
VMM	145	PWR	+2.0V	
TXPOUT1	146	O	PECL	16 bit PECL output bus

**Table 20: Pin Identification**

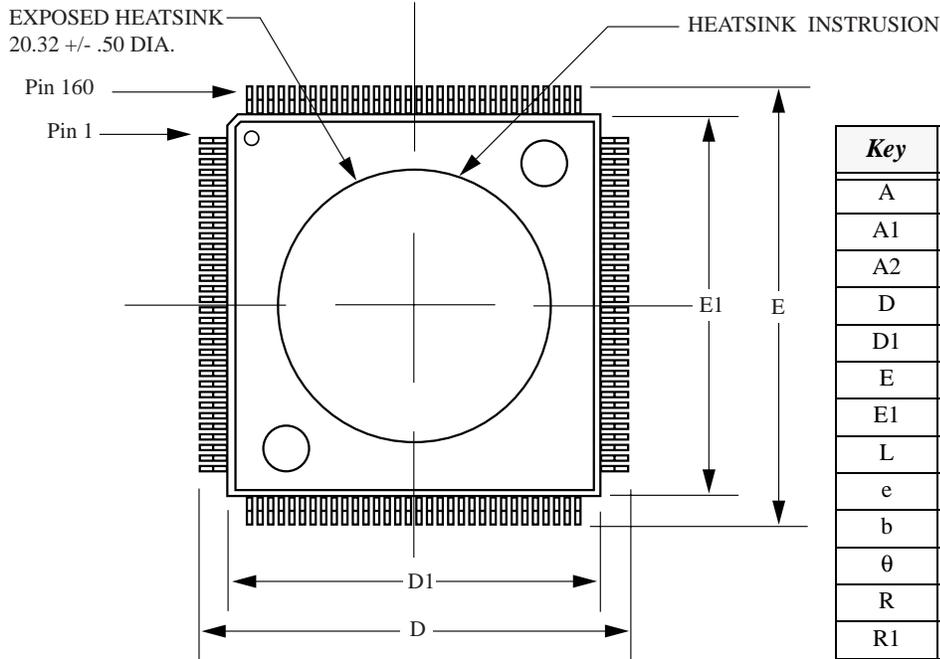
<i>Signal</i>	<i>Pin</i>	<i>I/O</i>	<i>Level</i>	<i>Pin Description</i>
TXPOUT0	147	O	PECL	16 bit PECL output bus
VEE	148	PWR	GND	
POUTCLK	149	O	PECL	16 bit PECL bus clock
NC	150	—	—	Leave Unconnected
VCC	151	PWR	+3.3V	
VCC	152	PWR	+3.3V	
NC	153	—	—	Leave Unconnected
NC	154	—	—	Leave Unconnected
TEST	155	I	GND	Test Input (TTL CLK)
TEST	156	I	GND	Test Input (TTL SEL)
NC	157	—	—	Leave Unconnected
SYSRST	158	I	TTL	System Reset
NC	159	—	—	Leave Unconnected
TEST	160	I	GND	Test Input

## Advance Product Information

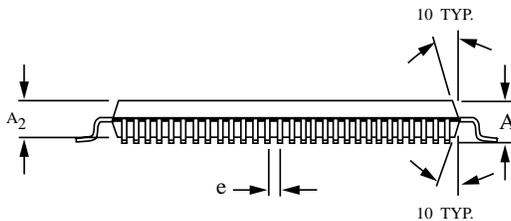
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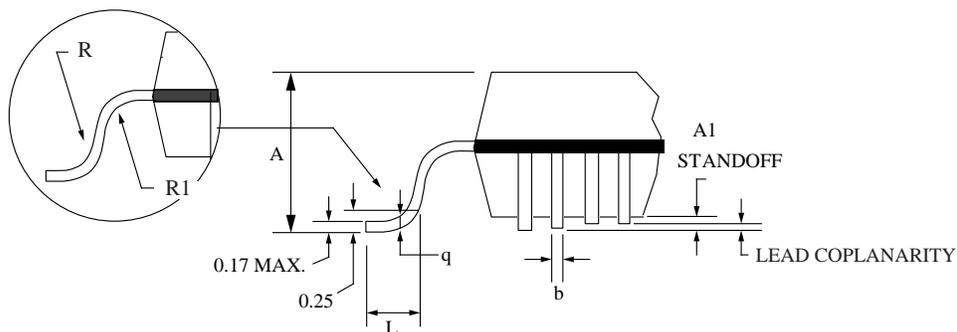
### Package Information



Key	mm	Tolerance
A	4.10	MAX
A1	0.25	MIN
A2	3.49	±0.10
D	31.20	±0.20
D1	28.00	±0.10
E	31.20	±0.20
E1	28.00	±0.10
L	0.88	+0.15/-0.10
e	0.65	BASIC
b	0.30	±0.05
θ	0-7°	
R	.30	TYP
R1	.20	TYP



Notes:  
(1) Drawing not to scale  
Package #101-285-5, Issue #1



160 Plastic Quad Flat Pack

Notes: 1) Drawing is not to scale  
2) All dimensions in mm  
3) Package represented is also used for the 144, 184, & 208 PQFP packages. Pin count drawn does not reflect the 160 package.

## Package Thermal Characteristics

The VSC8151 is packaged in an 160 pin, 28mm x 28mm thermally enhanced PQFP (EDQUAD) with an exposed heatsink. These packages use industry-standard JEDEC footprints, but have been enhanced to improve thermal dissipation. The construction of the packages are as shown in Figure 13. A heat sink may be necessary depending on the ambient temperature and airflow available in your system. Commercially available heatsinks are available to improve  $\theta_{ca}$  so that the case temperature is kept within the 85C specification.

Figure 17: Package Cross Section

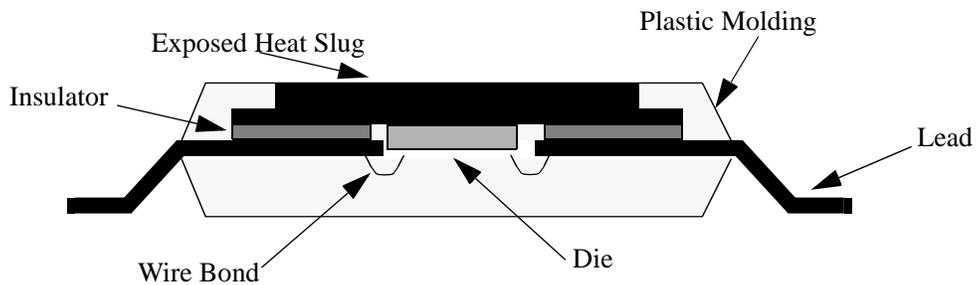


Table 21: 160-Pin Enhanced PQFP Thermal Resistance

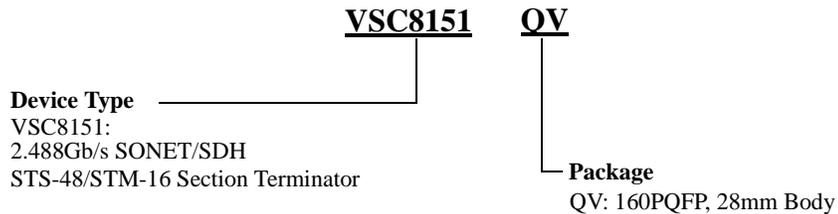
Symbol	Description	Value	Units
$\theta_{ca-0}$	Thermal resistance from case to ambient, still air	24	$^{\circ}\text{C}/\text{W}$
$\theta_{ca-1}$	Thermal resistance from case to ambient, 1 m/sec air	14	$^{\circ}\text{C}/\text{W}$
$\theta_{ca-2}$	Thermal resistance from case to ambient, 2 m/sec air	11	$^{\circ}\text{C}/\text{W}$
$\theta_{ca-4}$	Thermal resistance from case to ambient, 3 m/sec air	10	$^{\circ}\text{C}/\text{W}$

## Advance Product Information VSC8151

2.488Gb/s SONET/SDH  
STS-48/STM-16 Section Terminator

### Ordering Information

The order number for this product is formed by a combination of the device number, and package type.



### Notice

This document contains information about a new product during its early sampling phase. The information in this document is based on design targets, simulation results or early prototype test results. Characteristic data and other specifications are subject to change without notice. Therefore the reader is cautioned to confirm that this datasheet is current prior to design or order placement.

### Warning

Vitesse Semiconductor Corporation's products are not intended for use in life support appliances, devices or systems. Use of a Vitesse product in such applications without the written consent is prohibited.

2.488Gb/s SONET/SDH  
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**VSC8151**

