

TC74LVX125F, TC74LVX125FN, TC74LVX125FT

QUAD BUS BUFFER

The TC74LVX125 is a high speed CMOS QUAD BUS BUFFER fabricated with silicon gate C²MOS technology. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low voltage and battery operated systems.

This device requires the 3-state control input \bar{G} to be set high to place the output into the high impedance.

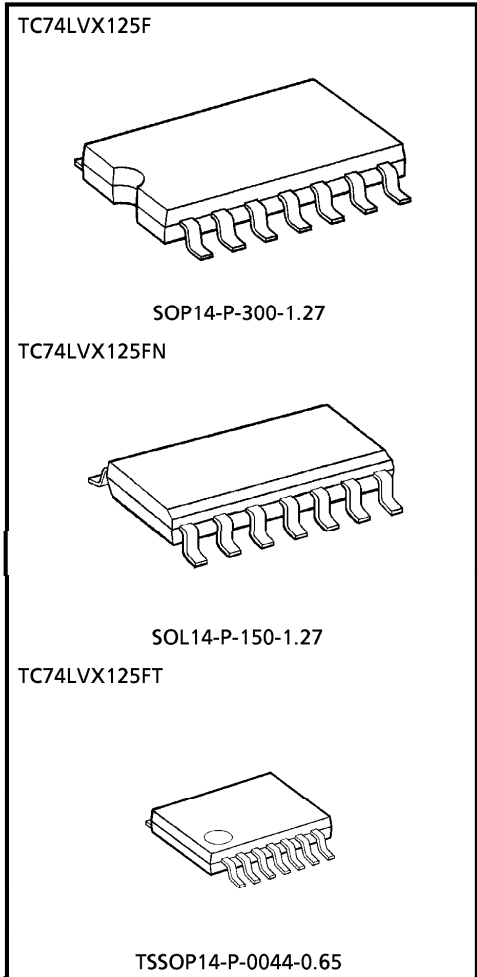
An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up.

This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

- High speed : $t_{pd} = 4.4ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) ($T_a = 25^\circ C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
 $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{pLH} \approx t_{pHL}$
- Low noise : $V_{OLP} = 0.5V$ (Max.)
- Pin and function compatible with 74HC125

(Note) The JEDEC SOP (FN) is not available in Japan.

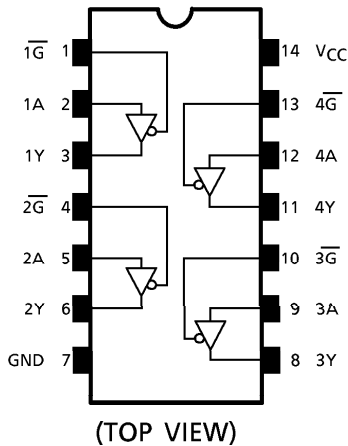


Weight
 SOP14-P-300-1.27 : 0.18g (Typ.)
 SOL14-P-150-1.27 : 0.12g (Typ.)
 TSSOP14-P-0044-0.65 : 0.06g (Typ.)

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PIN ASSIGNMENT

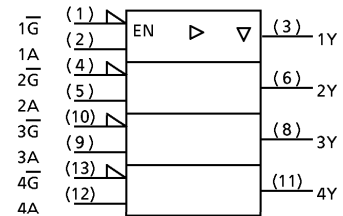


TRUTH TABLE

INPUTS		OUTPUTS
\overline{G}	A	Y
H	X	Z
L	L	L
L	H	H

X : Don't care
Z : High Impedance

IEC LOGIC SYMBOL



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7.0	V
DC Input Voltage	V_{IN}	-0.5~7.0	V
DC Output Voltage	V_{OUT}	-0.5~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} /Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	-65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

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- The information contained herein is subject to change without notice.

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM-BOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT			
						MIN.	TYP.	MAX.	MIN.	MAX.				
Input Voltage	"H" Level	V _{IH}			2.0	1.5	—	—	1.5	—	V			
					3.0	2.0	—	—	2.0	—				
					3.6	2.4	—	—	2.4	—				
	"L" Level	V _{IL}			2.0	—	—	0.5	—	0.5				
					3.0	—	—	0.8	—	0.8				
					3.6	—	—	0.8	—	0.8				
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}		I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V		
					I _{OH} = -50 μA	3.0	2.9	3.0	—	2.9	—			
					I _{OH} = -4mA	3.0	2.58	—	—	2.48	—			
	"L" Level	V _{OL}			V _{IN} = V _{IH} or V _{IL}		I _{OL} = 50 μA	2.0	—	0.0	0.1		—	0.1
							I _{OL} = 50 μA	3.0	—	0.0	0.1		—	0.1
							I _{OL} = 4mA	3.0	—	—	0.36		—	0.44
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND				3.6	—	—	±0.25	—	±2.5	μA	
Input Leakage Current		I _{IN}	V _{IN} = 5.5V or GND				3.6	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND				3.6	—	—	4.0	—	40.0	μA	

AC characteristics (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t _{pLH}		2.7	15	—	5.8	10.1	1.0	13.5	ns
				50	—	8.3	13.6	1.0	17.0	
	3.3 ± 0.3		15	—	4.4	6.2	1.0	8.5		
			50	—	6.9	9.7	1.0	12.0		
Output Enable Time	t _{pZL}	R _L = 1kΩ	2.7	15	—	5.3	9.3	1.0	12.5	ns
				50	—	7.8	12.8	1.0	16.0	
	3.3 ± 0.3		15	—	4.0	5.6	1.0	7.5		
			50	—	6.5	9.1	1.0	11.0		
Output Disable Time	t _{pLZ}	R _L = 1kΩ	2.7	50	—	10.0	15.7	1.0	19.0	ns
			3.3 ± 0.3	50	—	8.3	11.2	1.0	13.0	
Output To Output Skew	t _{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t _{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C _{IN}	(Note 2)			—	4	10	—	10	pF
Output Capacitance	C _{OUT}				—	6	—	—	—	pF
Power Dissipation Capacitance	C _{PD}	(Note 3)			—	14	—	—	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

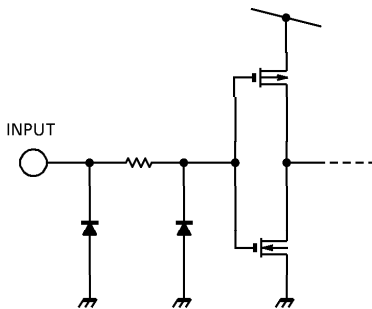
Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4 \text{ (per bit)}$$

Noise characteristics (Ta = 25°C, Input tr = tf = 3ns, CL = 50pF)

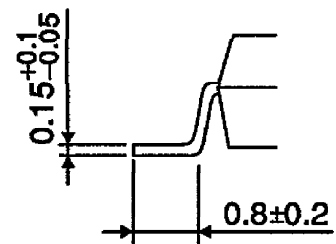
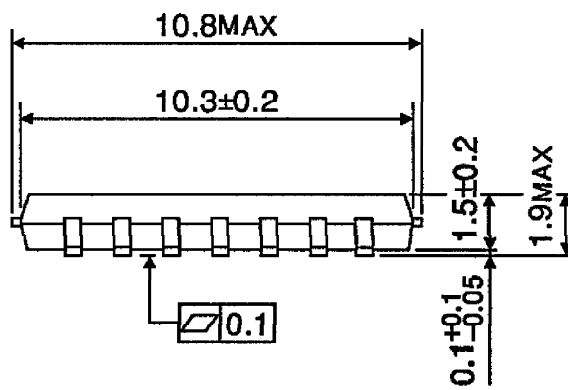
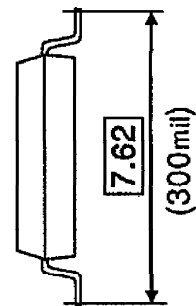
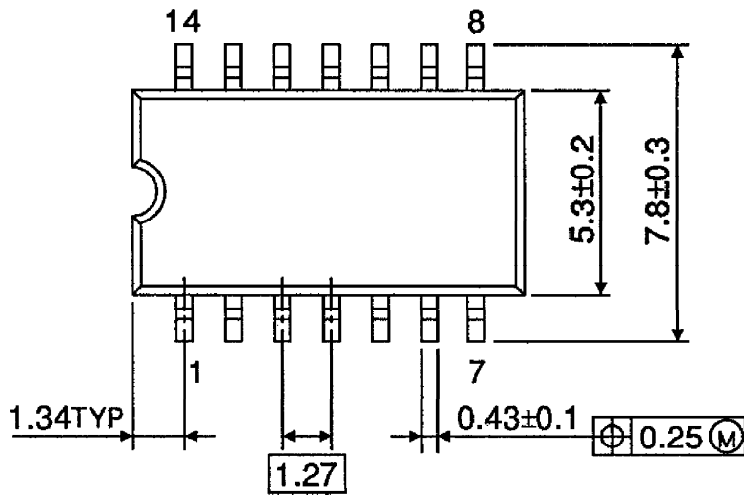
PARAMETER	SYMBOL	TEST CONDITION	$\overline{V_{CC}}$ (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	-0.3	-0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SOP14-P-300-1.27

Unit : mm

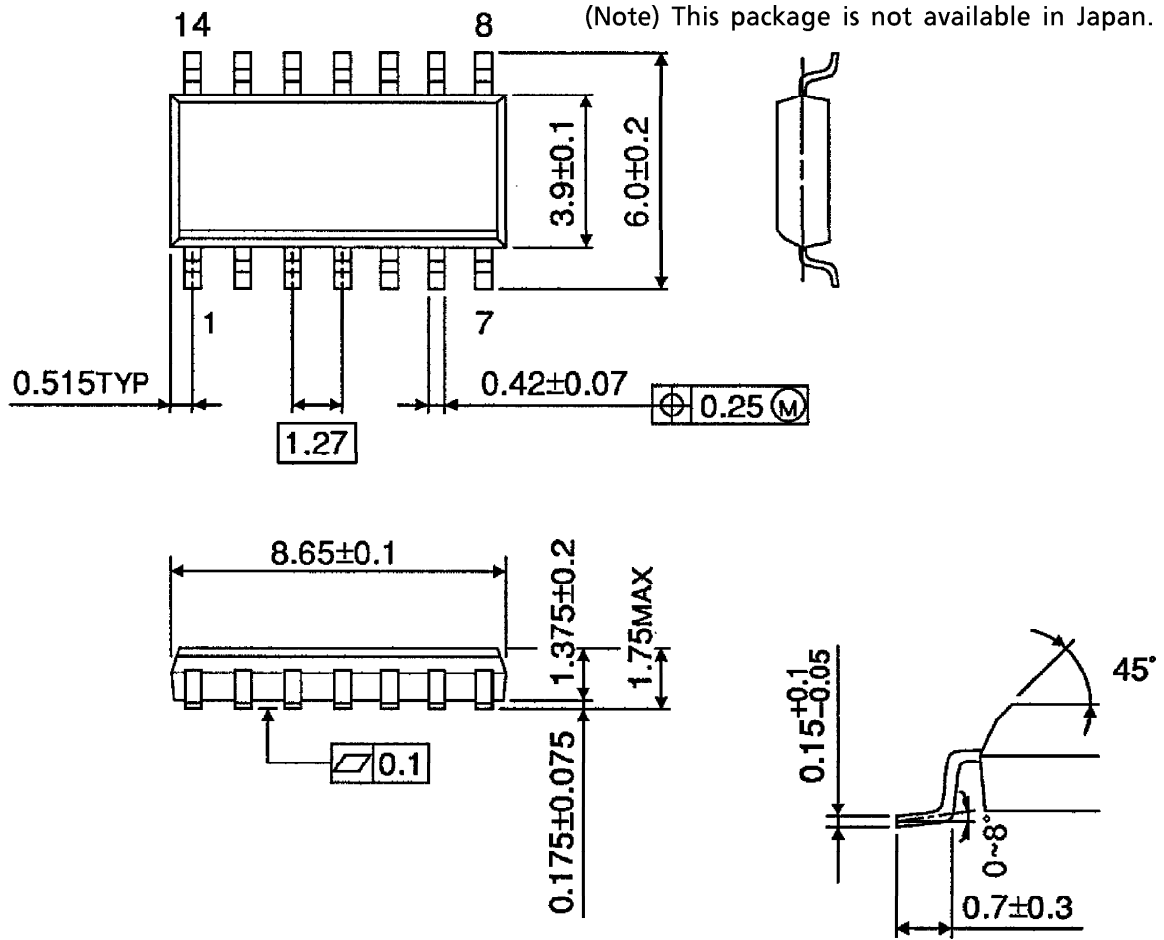


Weight : 0.18g (Typ.)

OUTLINE DRAWING
SOL14-P-150-1.27

Unit : mm

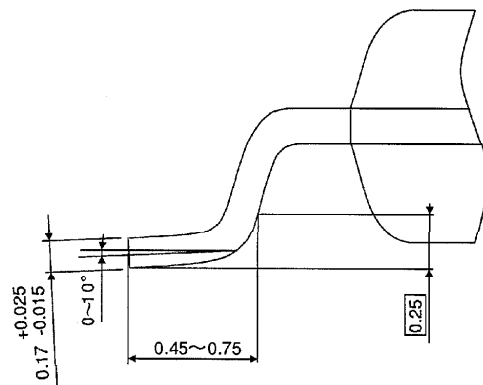
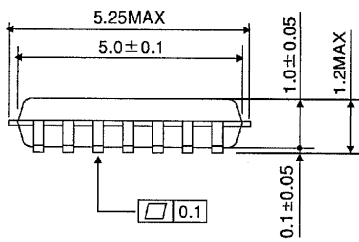
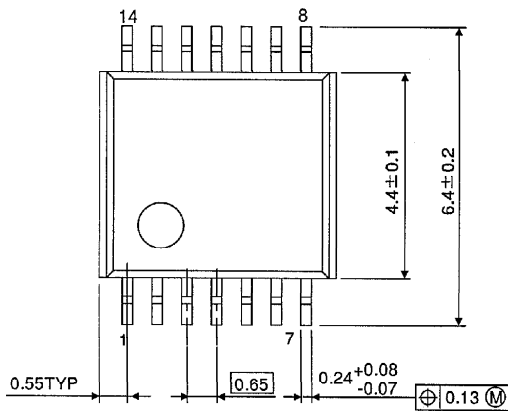
(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)

OUTLINE DRAWING
TSSOP14-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)

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