

TC74LVX174F, TC74LVX174FN, TC74LVX174FT

HEX D-TYPE FLIP FLOP WITH CLEAR

The TC74LVX174 is a high speed CMOS HEX D-FLIP FLOP fabricated with silicon gate C²MOS technology.

Designed for use in 3.3 Volt systems, they achieve high speed operation while maintaining the CMOS low power dissipation. This device is suitable for low voltage and battery operated systems.

Information signals applied to D inputs are transferred to the Q output on the positivegoing edge of the clock pulse.

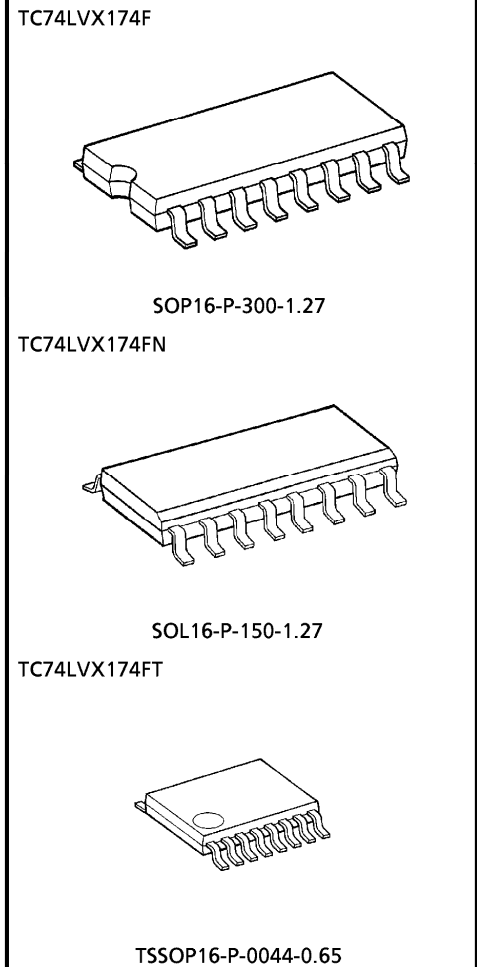
When the $\overline{\text{CLR}}$ input is held low, the Q output are in the low logic level independent of the other inputs.

An input protection circuit ensures that 0 to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

FEATURES

- High speed : $f_{\text{MAX}} = 180\text{MHz}$ (Typ.) ($V_{\text{CC}} = 3\text{V}$)
- Low power dissipation : $I_{\text{CC}} = 4\mu\text{A}$ (Max.) ($T_a = 25^\circ\text{C}$)
- Input voltage level : $V_{\text{IL}} = 0.8\text{V}$ (Max.) ($V_{\text{CC}} = 3\text{V}$)
 $V_{\text{IH}} = 2.0\text{V}$ (min.) ($V_{\text{CC}} = 3\text{V}$)
- Power down protection is provided on all inputs.
- Balanced propagation delays : $t_{\text{pLH}} \approx t_{\text{pHL}}$
- Low noise : $V_{\text{OLP}} = 0.5\text{V}$ (Max.)
- Pin and function compatible with 74HC174

(Note) The JEDEC SOP (FN) is not available in Japan.



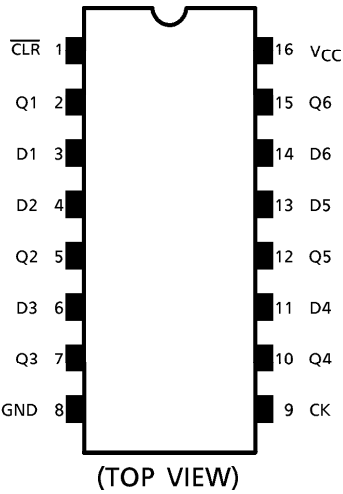
Weight

SOP16-P-300-1.27	: 0.18g (Typ.)
SOL16-P-150-1.27	: 0.12g (Typ.)
TSSOP16-P-0044-0.65	: 0.06g (Typ.)

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PIN ASSIGNMENT

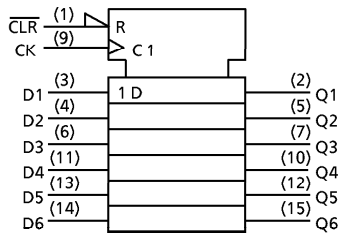


TRUTH TABLE

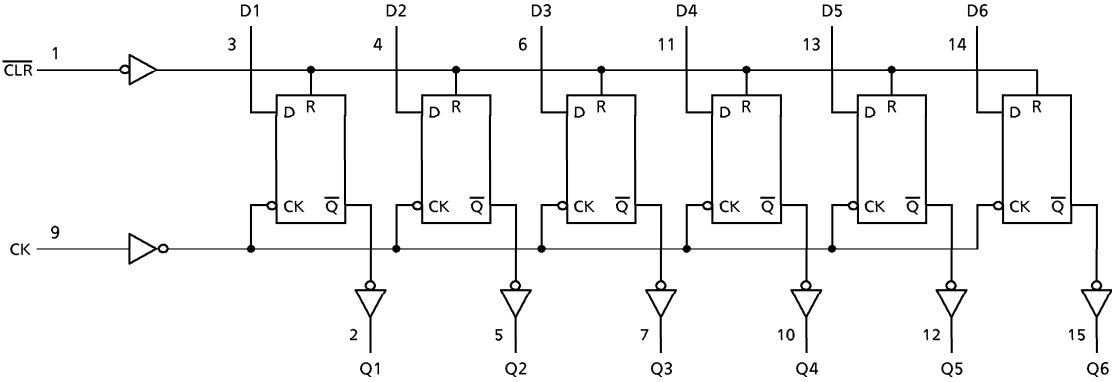
INPUTS			OUTPUTS	FUNCTION
CLR	D	CK	Q	
L	X	X	L	CLEAR
H	L		L	—
H	H		H	—
H	X		Qn	NO CHANGE

X : Don't Care

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7.0$	V
DC Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
DC Output Voltage	V_{OUT}	$-0.5 \sim V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	-20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} /Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage	V_{IN}	0~5.5	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYM- BOL	TEST CONDITION		V _{CC} (V)	Ta = 25°C			Ta = - 40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	“H” Level	V _{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	“L” Level	V _{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	“H” Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 50μA	2.0	1.9	2.0	—	1.9	—	V
				I _{OH} = - 50μA	3.0	2.9	3.0	—	2.9	—	
				I _{OH} = - 4mA	3.0	2.58	—	—	2.48	—	
	“L” Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I _{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I _{OL} = 4mA	3.0	—	—	0.36	—	0.44	
Input Leakage Current		I _{IN}	V _{IN} = 5.5V or GND		3.6	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current		I _{CC}	V _{IN} = V _{CC} or GND		3.6	—	—	4.0	—	40.0	μA

TIMING REQUIREMENTS (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION	Ta = 25°C		Ta = -40~85°C		UNIT
			V _{CC} (V)	LIMIT	LIMIT	LIMIT	
Minimum Pulse Width (CK)	t _W (L)		2.7	6.5	7.5		ns
	t _W (H)		3.3 ± 0.3	5.0	5.0		
Minimum Pulse Width (CLR)	t _W (L)		2.7	6.5	7.5		ns
			3.3 ± 0.3	5.0	5.0		
Minimum Set-up Time	t _s		2.7	7.5	8.5		ns
			3.3 ± 0.3	5.0	6.0		
Minimum Hold Time	t _h		2.7	0.0	0.0		ns
			3.3 ± 0.3	0.0	0.0		
Minimum Removal Time (CLR)	t _{rem}		2.7	4.5	4.5		ns
			3.3 ± 0.3	3.0	3.0		

AC characteristics (Input $t_r = t_f = 3\text{ns}$)

PARAMETER	SYM-BOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT
			V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	
Propagation Delay Time (CK-Q)	t _{pLH} t _{pHL}		2.7	15	—	7.6	14.5	ns
				50	—	10.1	18.0	
			3.3 ± 0.3	15	—	5.9	9.3	
				50	—	8.4	12.8	
Propagation Delay Time (CLR-Q)	t _{pHL}		2.7	15	—	7.9	15.0	ns
				50	—	10.4	18.5	
			3.3 ± 0.3	15	—	6.2	9.7	
				50	—	8.7	13.2	
Maximum Clock Frequency	f _{MAX}		2.7	15	65	130	—	MHz
				50	45	60	—	
			3.3 ± 0.3	15	115	180	—	
				50	65	95	—	
Output To Output Skew	t _{osLH} t _{osHL}	(Note 1)	2.7	50	—	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	
Input Capacitance	C _{IN}	(Note 2)	—			4	10	pF
Power Dissipation Capacitance	C _{PD}	(Note 3)	—			29	—	pF

(Note 1) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr.}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/6 \text{ (per F/F)}$$

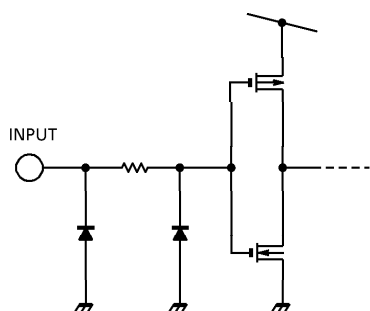
And the total C_{PD} when n pcs. of F/F operate can be gained by the following equation :

$$C_{PD}(\text{total}) = 19 + 10 \cdot n$$

Noise characteristics ($T_a = 25^\circ\text{C}$, Input $t_r = t_f = 3\text{ns}$, $C_L = 50\text{pF}$)

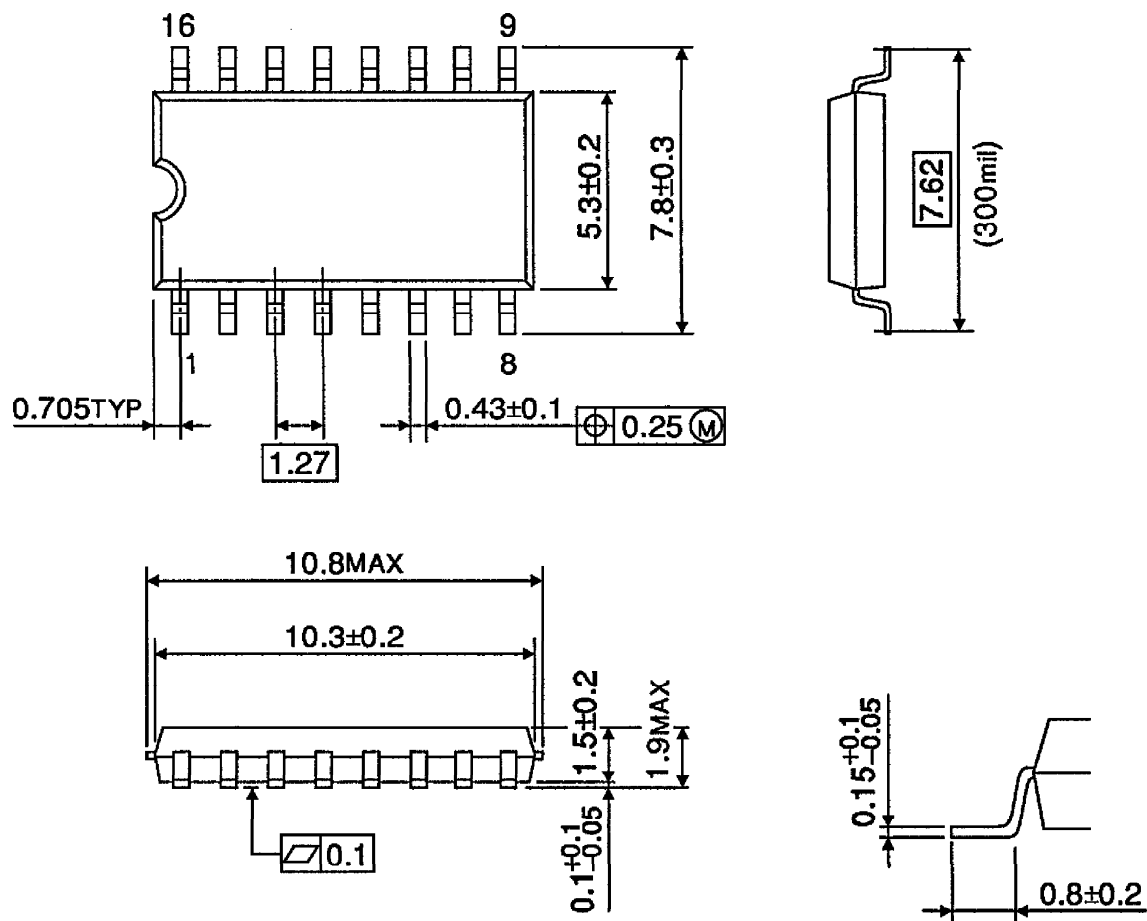
PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.3	0.5	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	-0.3	-0.5	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT



OUTLINE DRAWING
SOP16-P-300-1.27

Unit : mm

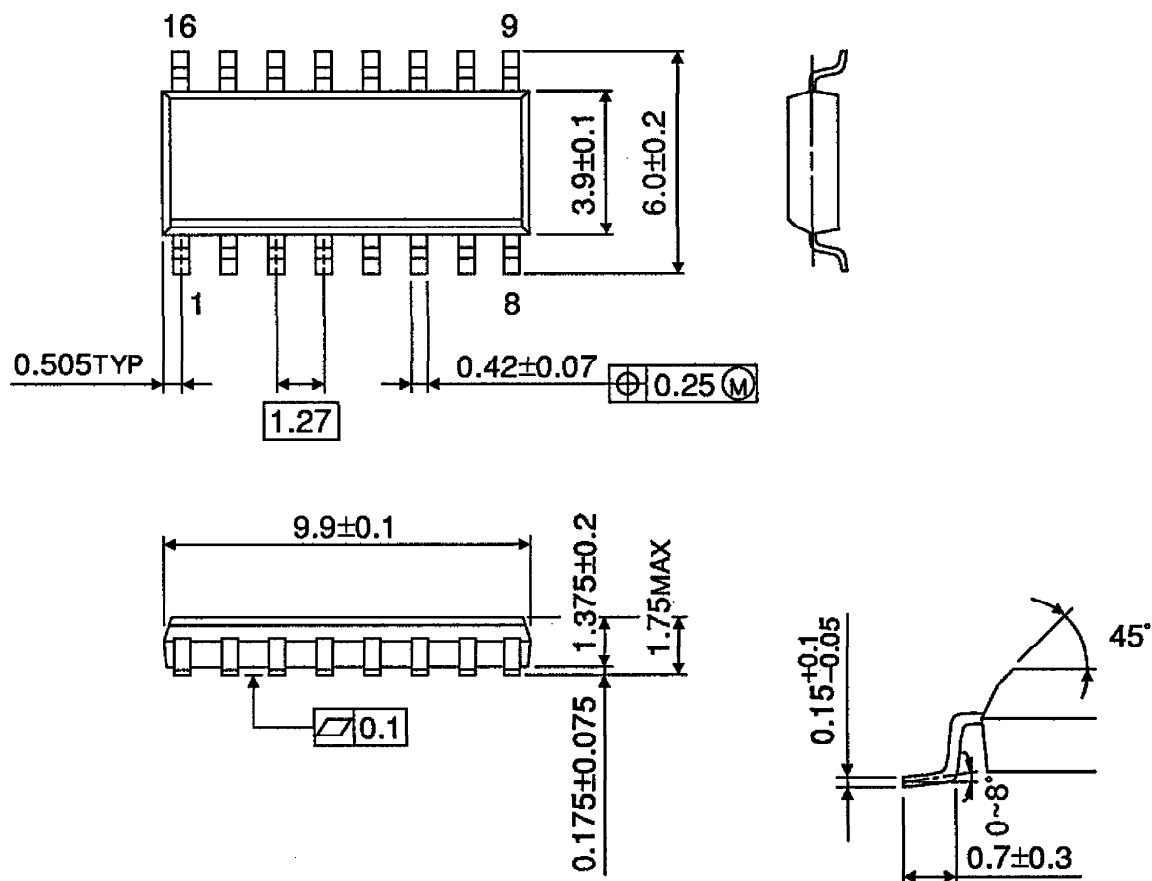


Weight : 0.18g (Typ.)

OUTLINE DRAWING
SOL16-P-150-1.27

Unit : mm

(Note) This package is not available in Japan.

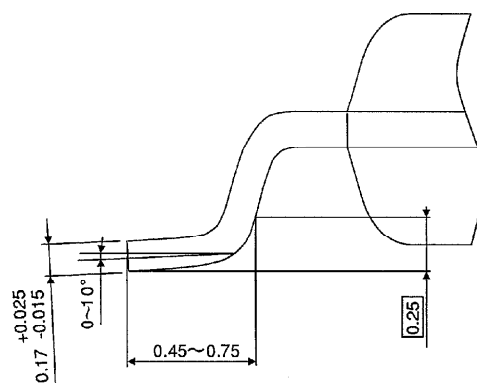
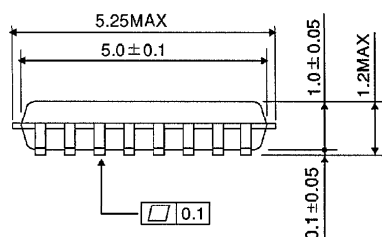
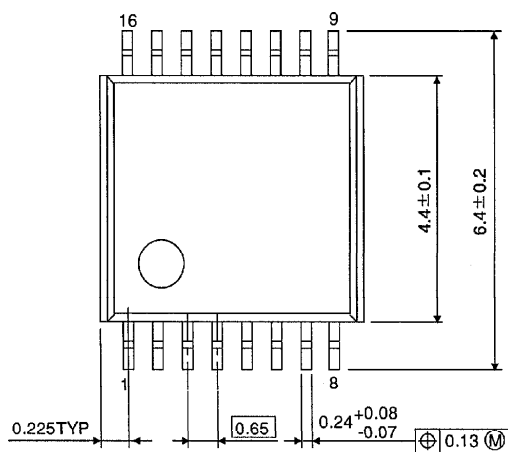


Weight : 0.12g (Typ.)

OUTLINE DRAWING

TSSOP16-P-0044-0.65

Unit : mm



Weight : 0.06g (Typ.)

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