TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LVX245F, TC74LVX245FW, TC74LVX245FT

OCTAL BUS TRANSCEIVER

The TC74LVX245 is a high speed CMOS OCTAL BUS TRANSCEIVER fabricated using silicon gate C^2MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. These devices are suitable for low voltage and battery operated systems.

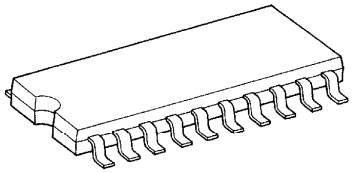
It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input ($\overline{G}$) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

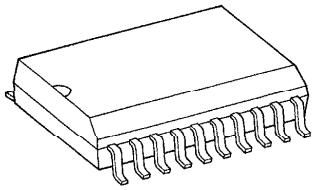
(Note) The JEDEC SOP (FW) is not available in Japan.

TC74LVX245F



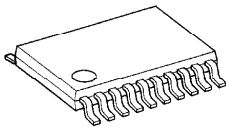
SOP20-P-300-1.27

TC74LVX245FW



SOL20-P-300-1.27

TC74LVX245FT



TSSOP20-P-0044-0.65

Weight
SOP20-P-300-1.27 : 0.22g (Typ.)
SOL20-P-300-1.27 : 0.46g (Typ.)
TSSOP20-P-0044-0.65 : 0.08g (Typ.)

FEATURES

- High speed : $t_{pd} = 4.7ns$ (Typ.) ($V_{CC} = 3.3V$)
- Low power dissipation : $I_{CC} = 4\mu A$ (Max.) ($Ta = 25°C$)
- Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$)
  $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)
- Balanced propagation delays : $t_{pLH} \simeq t_{pHL}$
- Low noise : $V_{OLP} = 0.8V$ (Max.)
- Pin and function compatible with 74HC245

961001EBA2

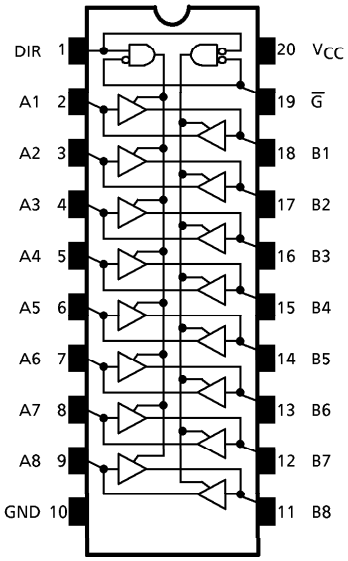
APPLICATION NOTES

Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

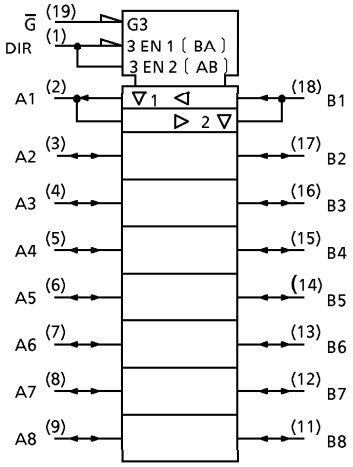
A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

PIN ASSIGNMENT



(TOP VIEW)

IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION	
$\overline{G}$	DIR		A-BUS	B-BUS
L	L	A = B	OUTPUT	INPUT
L	H	B = A	INPUT	OUTPUT
H	X	Z	High Impedance	

X : Don't Care

Z : High Inpedance

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	−0.5~7.0	V
DC Input Voltage (DIR, $\overline{G}$)	V_{IN}	−0.5~7.0	V
DC Bus I/O Voltage	$V_{I/O}$	−0.5~V_{CC}+0.5	V
Input Diode Current	I_{IK}	−20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±75	mA
Power Dissipation	P_D	180	mW
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	2.0~3.6	V
Input Voltage (DIR, $\overline{G}$)	V_{IN}	0~5.5	V
Bus I/O Voltage	$V_{I/O}$	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise And Fall Time	dt/dv	0~100	ns/V

ELECTRICAL CHARACTERISTICS

DC characteristics

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C			Ta = −40~85°C		UNIT
						MIN.	TYP.	MAX.	MIN.	MAX.	
Input Voltage	"H" Level	V_{IH}			2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	"L" Level	V_{IL}			2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output Voltage	"H" Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50μA	2.0	1.9	2.0	—	1.9	—	V
				I_{OH} = −50μA	3.0	2.9	3.0	—	2.9	—	
				I_{OH} = −4mA	3.0	2.58	—	—	2.48	—	
	"L" Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50μA	2.0	—	0.0	0.1	—	0.1	
				I_{OL} = 50μA	3.0	—	0.0	0.1	—	0.1	
				I_{OL} = 4mA	3.0	—	—	0.36	—	0.44	
3-State Output Off-State Current		I_{OZ}	V_{IN} = V_{IH} or V_{IL} V_{OUT} = V_{CC} or GND		3.6	—	—	±0.25	—	±2.5	μA
Input Leakage Current		I_{IN}	V_{IN} = 5.5V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND		3.6	—	—	4.0	—	40.0	μA

AC characteristics (Input $t_r = t_f = 3ns$)

PARAMETER	SYM-BOL	TEST CONDITION			Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	C_L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	
Propagation Delay Time	t_{pLH} t_{pHL}		2.7	15	—	6.1	10.7	1.0	13.5	ns
				50	—	8.6	14.2	1.0	17.0	
			3.3 ± 0.3	15	—	4.7	6.6	1.0	8.0	
				50	—	7.2	10.1	1.0	11.5	
Output Enable Time	t_{pZL} t_{pZH}	$R_L = 1k\Omega$	2.7	15	—	9.0	16.9	1.0	20.5	ns
				50	—	11.5	20.4	1.0	24.0	
			3.3 ± 0.3	15	—	7.1	11.0	1.0	13.0	
				50	—	9.6	14.5	1.0	16.5	
Output Disable Time	t_{pLZ} t_{pHZ}	$R_L = 1k\Omega$	2.7	50	—	11.5	18.0	1.0	21.0	ns
			3.3 ± 0.3	50	—	9.6	12.8	1.0	14.5	
Output To Output Skew	t_{osLH} t_{osHL}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
			3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input Capacitance	C_{IN}	DIR, $\overline{G}$ (Note 2)			—	4	10	—	10	pF
Bus Input Capacitance	$C_{I/O}$	An, Bn			—	8	—	—	—	pF
Power Dissipation Capacitance	C_{PD}	(Note 3)			—	21	—	—	—	pF

(Note 1) Parameter guaranteed by design.
($t_{osLH} = |t_{pLHm} - t_{pLHn}|$, $t_{osHL} = |t_{pHLm} - t_{pHLn}|$)

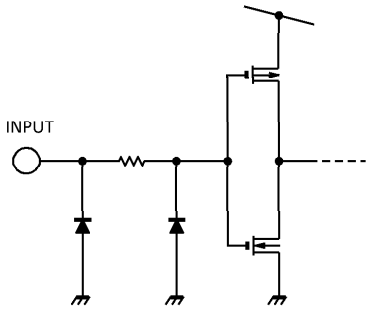
(Note 2) Parameter guaranteed by design.

(Note 3) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
Average operating current can be obtained by the equation :
$I_{CC\,(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/8$ (per bit)

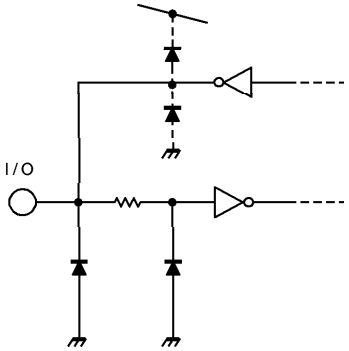
Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3ns$, $C_L = 50pF$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V_{OL}	V_{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V_{OL}	V_{OLV}		3.3	−0.5	−0.8	V
Minimum High Level Dynamic Input Voltage	V_{IHD}		3.3	—	2.0	V
Maximum Low Level Dynamic Input Voltage	V_{ILD}		3.3	—	0.8	V

INPUT EQUIVALENT CIRCUIT (DIR, $\overline{G}$)



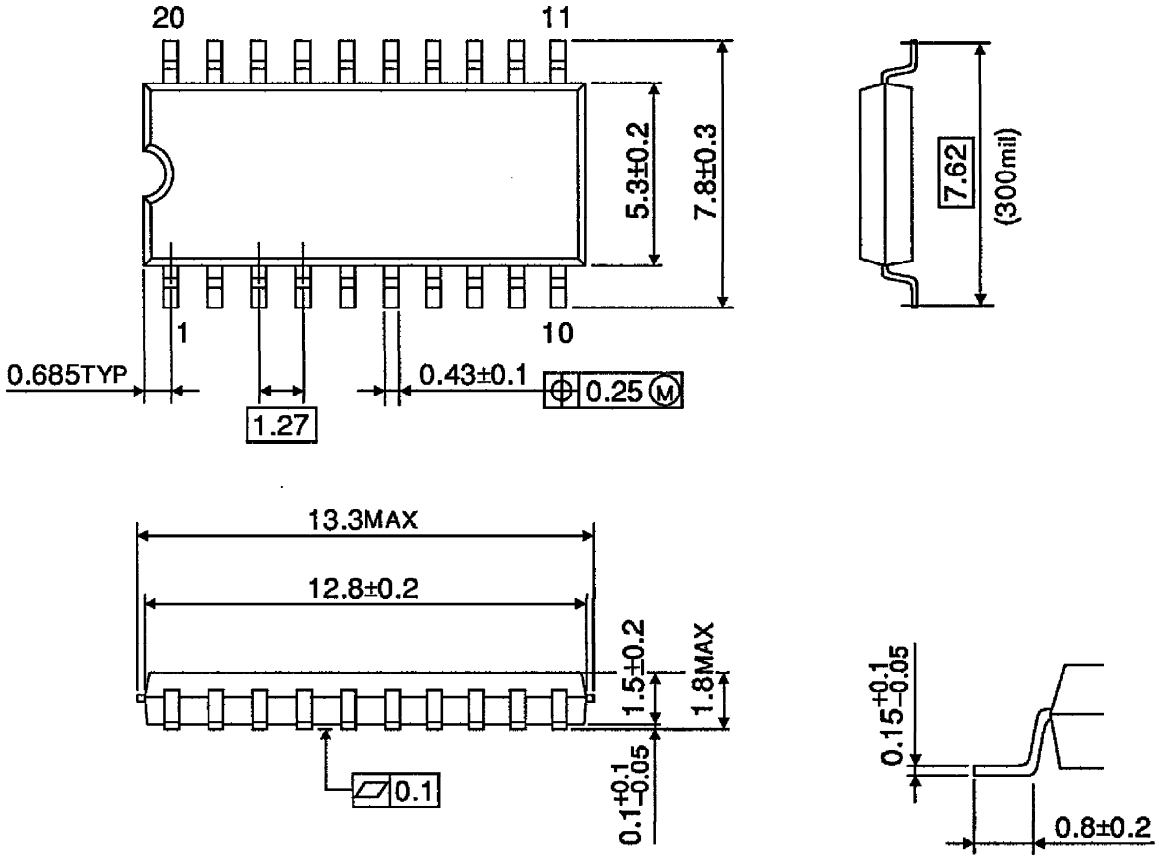
BUS TERMINAL EQUIVALENT CIRCUIT (An, Bn)



OUTLINE DRAWING

SOP20-P-300-1.27

Unit : mm

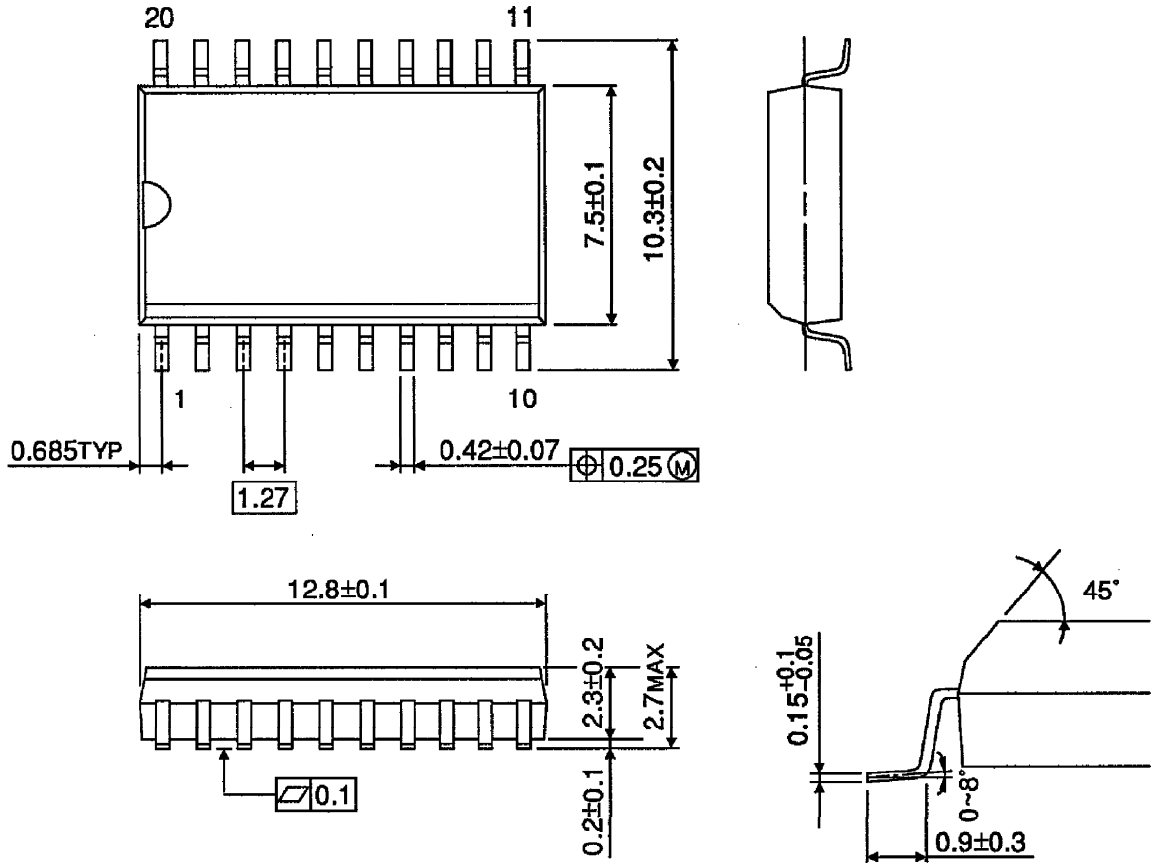


Weight : 0.22g (Typ.)

OUTLINE DRAWING

SOL20-P-300-1.27 Unit : mm

(Note) This package is not available in Japan.

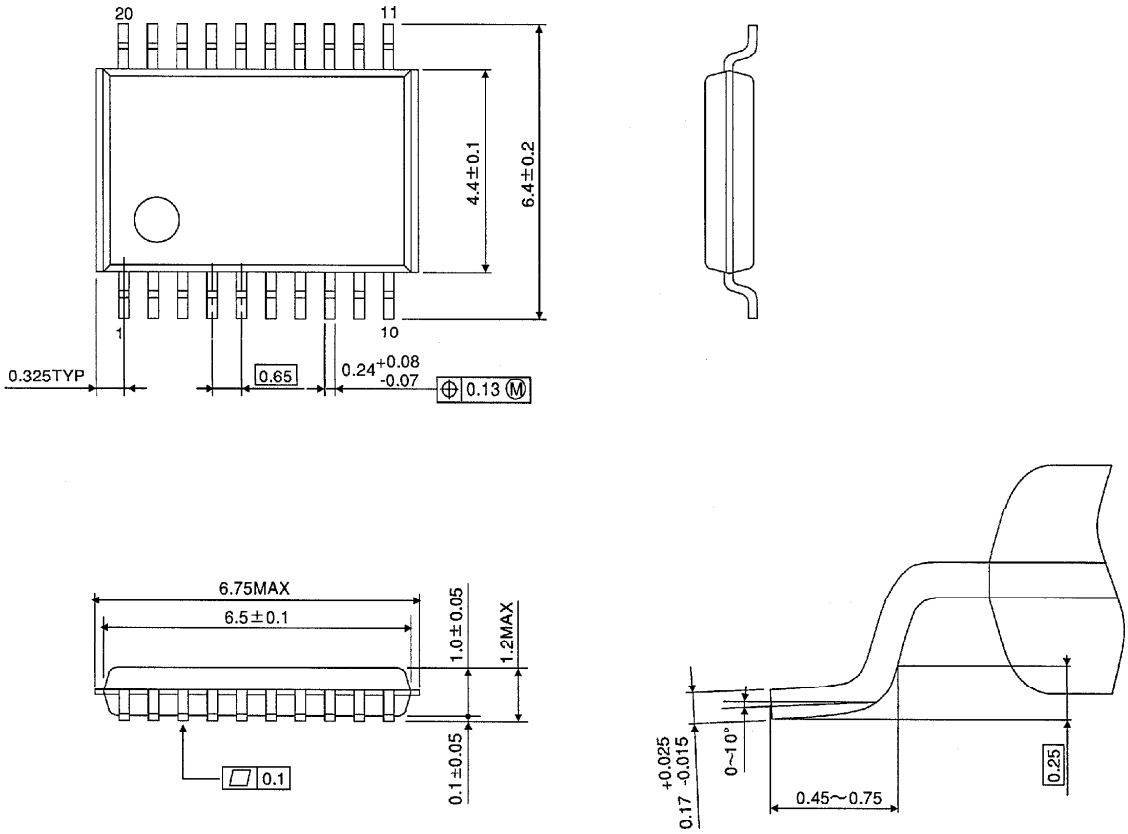


Weight : 0.46g (Typ.)

OUTLINE DRAWING

TSSOP20-P-0044-0.65

Unit : mm



Weight : 0.08g (Typ.)