TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LVX245F, TC74LVX245FW, TC74LVX245FT

OCTAL BUS TRANSCEIVER

The TC74LVX245 is a high speed CMOS OCTAL BUS TRANSCEIVER fabricated using silicon gate C²MOS technology.

Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation. These devices are suitable for low voltage and battery operated systems.

It is intended for two-way asynchronous communication between data busses. The direction of data transmission is determined by the level of the DIR input.

The enable input (\overline{G}) can be used to disable the device so that the busses are effectively isolated.

All inputs are equipped with protection circuits against static discharge.

FEATURES

• High speed : $t_{pd} = 4.7$ ns (Typ.) ($V_{CC} = 3.3$ V)

• Low power dissipation : $I_{CC} = 4\mu A$ (Max.) (Ta = 25°C)

• Input voltage level : $V_{IL} = 0.8V$ (Max.) ($V_{CC} = 3V$) $V_{IH} = 2.0V$ (Min.) ($V_{CC} = 3V$)

منتملمات متم

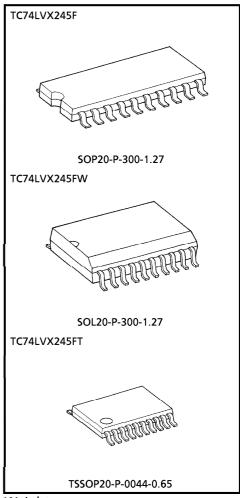
Balanced propagation delays

: ^tpLH≃^tpHL

Low noise : V_{OLP} = 0.8V (Max.)

• Pin and function compatible with 74HC245

(Note) The JEDEC SOP (FW) is not available in Japan.



Weight

SOP20-P-300-1.27 : 0.22g (Typ.) SOL20-P-300-1.27 : 0.46g (Typ.) TSSOP20-P-0044-0.65 : 0.08g (Typ.)

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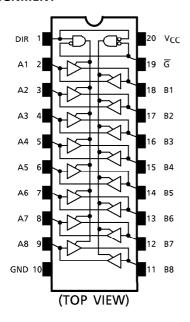
APPLICATION NOTES

Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

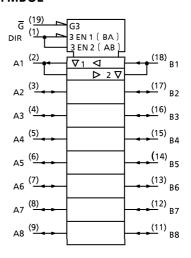
All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

A parasitic diode is formed between the bus and V_{CC} terminals. Therefore bus terminal can not be used to interface 5V to 3V systems directly.

PIN ASSIGNMENT



IEC LOGIC SYMBOL



TRUTH TABLE

INPUTS		OUTPUTS	FUNCTION			
G	DIR	0011013	A-BUS	B-BUS		
L	L	A = B	OUTPUT	INPUT		
L	Н	B = A INPUT		OUTPUT		
Н	Х	Z	High Impedance			

X : Don't Care Z : High Inpedance

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MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage Range	Vcc	-0.5~7.0	V
DC Input Voltage (DIR, \overline{G})	VIN	- 0.5~7.0	V
DC Bus I/O Voltage	V _{I/O}	−0.5~V _{CC} +0.5	٧
Input Diode Current	lικ	- 20	mΑ
Output Diode Current	lok	± 20	mΑ
DC Output Current	IOUT	± 25	mA
DC V _{CC} /Ground Current	Icc	± 75	mΑ
Power Dissipation	PD	180	mW
Storage Temperature	T _{stg}	- 65∼150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	Vcc	2.0~3.6	V
Input Voltage (DIR, \overline{G})	v_{IN}	0~5.5	V
Bus I/O Voltage	V _I /O	0~V _{CC}	V
Operating Temperature	T _{opr}	- 40∼85	°C
Input Rise And Fall Time	dt/dv	0~100	ns / V

ELECTRICAL CHARACTERISTICS

DC characteristics

DADAI	METED	SYM-	TEST C	ONDITION	Vcc	٦	Γa = 25°0	С	Ta = -4	10∼85°C	UNIT
PARAI	METER	BOL	1231 C	ONDITION	(V)	MIN.	TYP.	MAX.	MIN.	MAX.	UNII
					2.0	1.5	_	_	1.5	_	
	"H" Level	V_{IH}			3.0	2.0	_	_	2.0	_	
Input					3.6	2.4		_	2.4	_	l _v l
Voltage					2.0	_		0.5	_	0.5	
	"L" Level	VIL			3.0	_	_	0.8	_	0.8	
					3.6	_	_	0.8	_	0.8	
			V _{IN} = V _{IH}	$I_{OH} = -50\mu A$	2.0	1.9	2.0	_	1.9	_	
	"H" Level	VOH		$I_{OH} = -50\mu A$	3.0	2.9	3.0	_	2.9	_	
Output			or VIL	$I_{OH} = -4mA$	3.0	2.58	_	_	2.48	_	l _v l
Voltage			$V_{IN} = V_{IH}$	$I_{OL} = 50 \mu A$	2.0	_	0.0	0.1	_	0.1]
	"L" Level	VOL		$I_{OL} = 50 \mu A$	3.0	_	0.0	0.1	_	0.1	
			or ^V IL	I _{OL} = 4mA	3.0	_	_	0.36	_	0.44	
3-State Out	3-State Output		VIN=VIH o	r V _{IL}	3.6			±0.25		± 2.5	μΑ
Off-State C	urrent	VOUT = VCC or GND		3.0	_	_	20.23		2.5	μ A	
Input Leak	age Current	IIN	$V_{IN} = 5.5V$ or GND		3.6	_	_	± 0.1	_	± 1.0	μ A
Quiescent S	Supply	Icc	V _{IN} = V _{CC} or GND		3.6			4.0		40.0	μΑ
Current		lcc	1111 - ACC C	, GND	3.0			4.0		40.0	μ

AC characteristics (Inp	out $t_r = t_f = 3ns$)
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PARAMETER	SYM-	TEST		Ta = 25°C			Ta = −40~85°C		UNIT	
PARAIVIETER	BOL CONDITI		V _{CC} (V)	C _L (pF)	MIN.	TYP.	MAX.	MIN.	MAX.	UNIT
	+		2.7	15		6.1	10.7	1.0	13.5	
Propagation Delay	t _{pLH}		2.7	50		8.6	14.2	1.0	17.0	ns
Time	t		3.3 ± 0.3	15		4.7	6.6	1.0	8.0	113
	t _{pHL}		3.3 ± 0.3	50	_	7.2	10.1	1.0	11.5	
	+	t_{pZL} $R_{I} = 1k\Omega$	2.7	15		9.0	16.9	1.0	20.5	
Output Enable Time	լ ւb∑Ր			50	_	11.5	20.4	1.0	24.0	ns
Output Lilable Tille	+	11 - 1122	3.3 ± 0.3	15	_	7.1	11.0	1.0	13.0	
	^t pZH	3.3	3.3 ± 0.3	50		9.6	14.5	1.0	16.5	
Output Disable Time	t _{pLZ}	$Z \mid_{R_L = 1k\Omega}$	2.7	50		11.5	18.0	1.0	21.0	nc
Output Disable Time	t _{pHZ}	K = 1 K T	3.3 ± 0.3	50	_	9.6	12.8	1.0	14.5	ns
Output To Output	tosLH	(Nicto 1)	2.7	50	_	_	1.5	_	1.5	
Skew	tosHL	(Note 1)	3.3 ± 0.3	50	_	_	1.5	_	1.5	ns
Input Capacitance	CIN	DIR, G (Note 2)			4	10	_	10	рF	
Bus Input Capacitance	CI/O	An, Bn		_	8	_	_	_	рF	
Power Dissipation Capacitance	C _{PD}	(Note 3)				21	_	_	_	pF

- (Note 1) Parameter guaranteed by design. $(t_{OSLH} = |t_{DLHm} - t_{DLHn}|, t_{OSHL} = |t_{DHLm} - t_{DHLn}|)$
- (Note 2) Parameter guaranteed by design.
- (Note 3) CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption. Average operating current can be obtained by the equation :

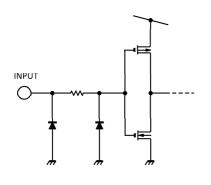
$$I_{CC (opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8 \text{ (per bit)}$$

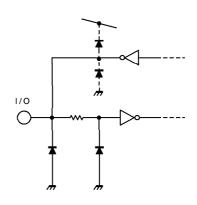
Noise characteristics (Ta = 25°C, Input $t_r = t_f = 3$ ns, $C_L = 50$ pF)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP.	LIMIT	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}		3.3	0.5	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}		3.3	- 0.5	-0.8	V
Minimum High Level Dynamic Input Voltage	V _{IHD}		3.3	_	2.0	V
Maximum Low Level Dynamic Input Voltage	V _{ILD}		3.3	_	0.8	V

INPUT EQUIVALENT CIRCUIT (DIR, \overline{G})

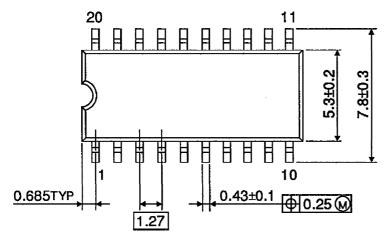
BUS TERMINAL EQUIVALENT CIRCUIT (An, Bn)

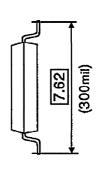


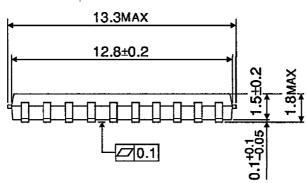


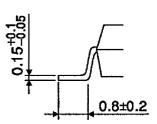
OUTLINE DRAWING SOP20-P-300-1.27

Unit: mm





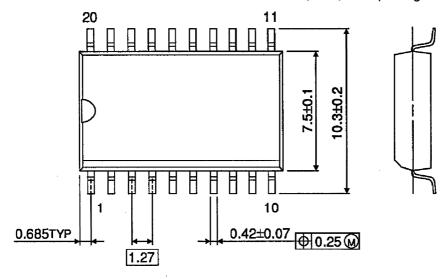


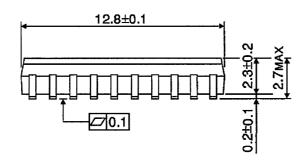


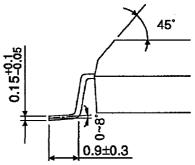
Weight: 0.22g (Typ.)

OUTLINE DRAWING SOL20-P-300-1.27

Unit: mm (Note) This package is not available in Japan.



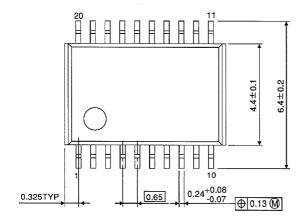


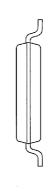


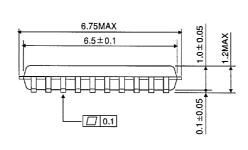
Weight: 0.46g (Typ.)

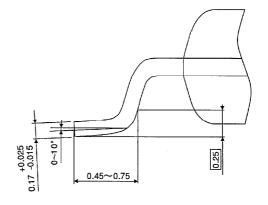
OUTLINE DRAWING TSSOP20-P-0044-0.65

Unit: mm









Weight: 0.08g (Typ.)

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