M30LW128D

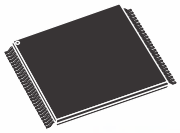
128 Mbit (two 64Mbit, x8/x16, Uniform Block, Flash Memories) 3V Supply, Multiple Memory Product

PRELIMINARY DATA

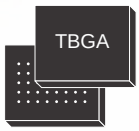
FEATURES SUMMARY

- TWO M58LW064D 64Mbit FLASH MEMORIES STACKED IN A SINGLE PACKAGE
- WIDE x8 or x16 DATA BUS for HIGH BANDWIDTH
- SUPPLY VOLTAGE
  - V_{DD} = 2.7 to 3.6V for Program, Erase and Read operations
  - V_{DDQ} = 1.8 to V_{DD} for I/O buffers
- ACCESS TIME
  - Random Read 110ns
  - Page Mode Read 110/25ns
- PROGRAMMING TIME
  - 16 Word Write Buffer
  - 16µs Word effective programming time
- 128 UNIFORM 64 KWord/128KByte MEMORY BLOCKS
- BLOCK PROTECTION/ UNPROTECTION
- PROGRAM and ERASE SUSPEND
- 128 bit PROTECTION REGISTER
- COMMON FLASH INTERFACE
- 100, 000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code M30LW128D: 8817h

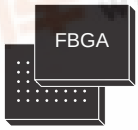
Figure 1. Packages



TSOP56 (N)
14 x 20 mm



TBGA64 (ZA)
10 x 13mm



LFBGA88 (ZE)
8 x 10mm

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SUMMARY DESCRIPTION

The M30LW128D is a 128 Mbit device that is composed of two separate 64 Mbit M58LW064D Flash memories. The device can be erased electrically at block level and programmed in-system using a 2.7V to 3.6V (V_{DD}) supply for the circuitry and a 1.8V to V_{DD} (V_{DDQ}) supply for the Input/Output pins.

The bus width can be configured for x8 or x16 for the devices available in the TSOP56 (14 x 20 mm) and TBGA64 (10x13mm**,** 1mm pitch) packages. The bus width is set to x16 for the devices available in the LFBGA88 (8x10mm, 0.8mm pitch) package.

Each internal M58LW064D has 3 Chip Enable signals to allow up to 4 memories to be connected together without the use of additional glue logic. In this way the address space is contiguous and the microprocessor only requires one Chip Enable, $\overline{E}$, to control both memories.

The device is divided into 128 blocks of 1Mbit (2 x 64 x 1Mb) that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the device. An on-chip Program/Erase Controller (P/E.C) simplifies the process of programming or erasing the device by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the device is consistent with JEDEC standards.

The Write Buffer allows the microprocessor to program from 1 to 16 Words in parallel, both speeding up the programming and freeing up the microprocessor to perform other work. A Word Program command is available to program a single word.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

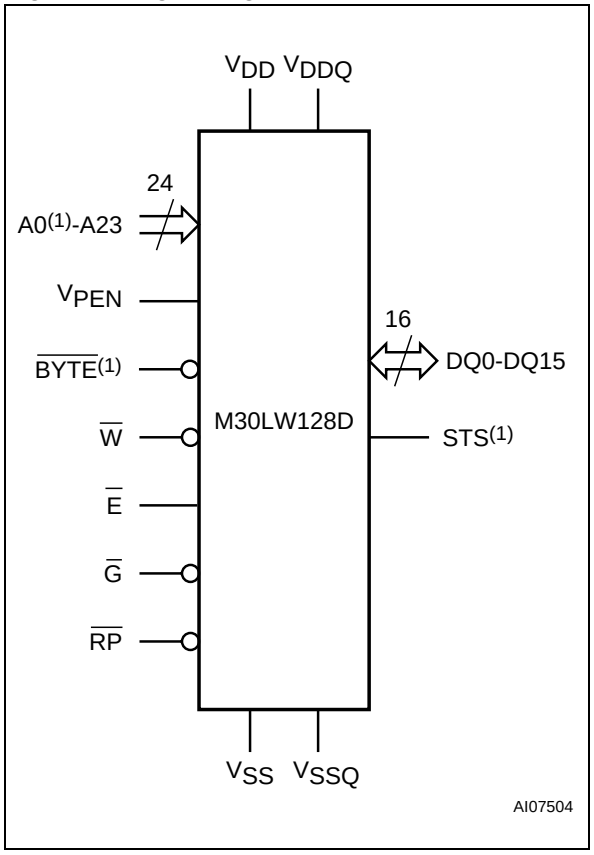
Individual block protection against Program or Erase is provided for data security. All blocks are protected during power-up. The protection of the blocks is non-volatile; after power-up the protection status of each block is restored to the state when power was last removed. Software commands are provided to allow protection of some or all of the blocks and to cancel all block protection bits simultaneously. All Program or Erase operations are blocked when the Program Erase Enable input V_{PEN} is low.

The Reset/Power-Down pin is used to apply a Hardware Reset to the enabled memory and to set the device in power-down mode.

The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes: Ready/Busy mode where a static signal indicates the status of the P/E.C, and Status mode where a pulsing signal indicates the end of a Program or Block Erase operation. In both modes it can be used as a system interrupt signal, useful for saving CPU time. The STS signal is only available with the TSOP56 and TBGA64 packages.

Each memory includes a 128 bit Protection Register. The Protection Register is divided into two 64 bit segments, the first one is written by the manufacturer (contact STMicroelectronics to define the code to be written here), while the second one is programmable by the user. The user programmable segment can be locked.

Figure 2. Logic Diagram



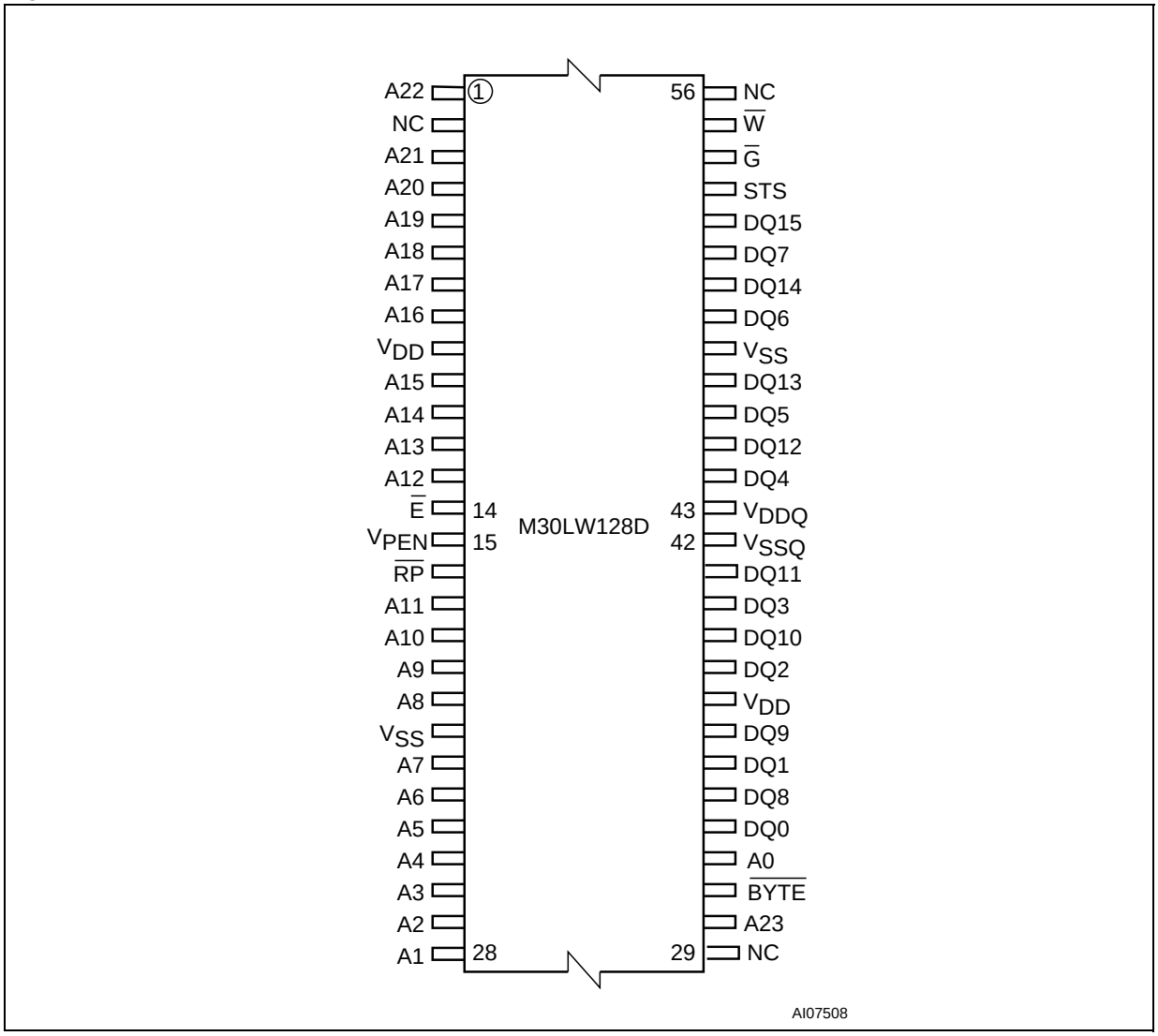
Note: 1. Not available with LFBGA88 package.

Table 1. Signal Names

A0 (1)	Address input (used in X8 mode only)
A1-A22	Address inputs
A23	Address Input to select memory
$\overline{BYTE}$ (1)	Byte/Word Organization Select
DQ0-DQ15	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{RP}$	Reset/Power-Down
STS (1)	Status/(Ready/Busy)
V_{PEN}	Program/Erase Enable
$\overline{W}$	Write Enable
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally
DU	Do Not Use

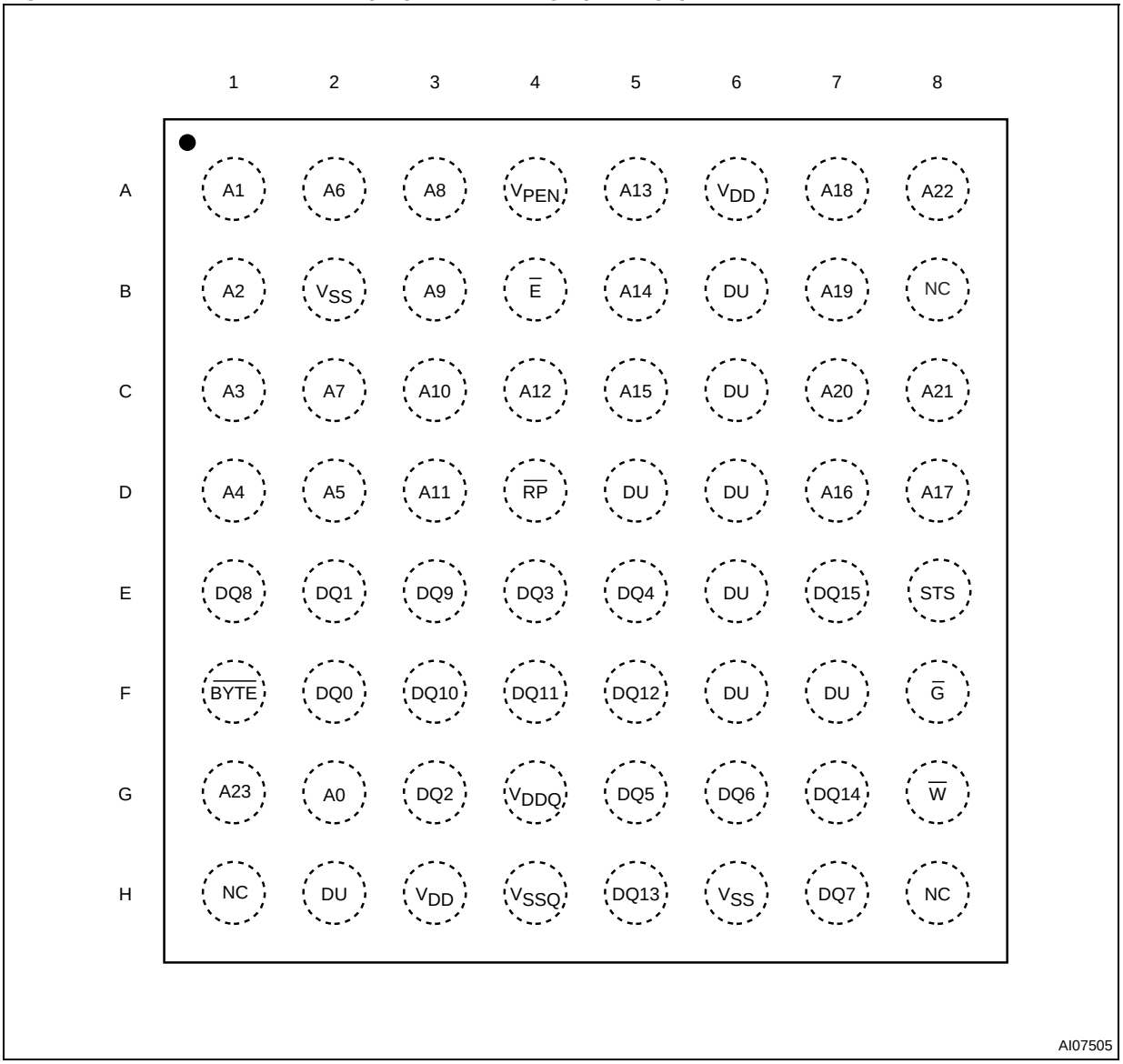
Note: 1. Not available with LFBGA88 package.

Figure 3. TSOP56 Connections



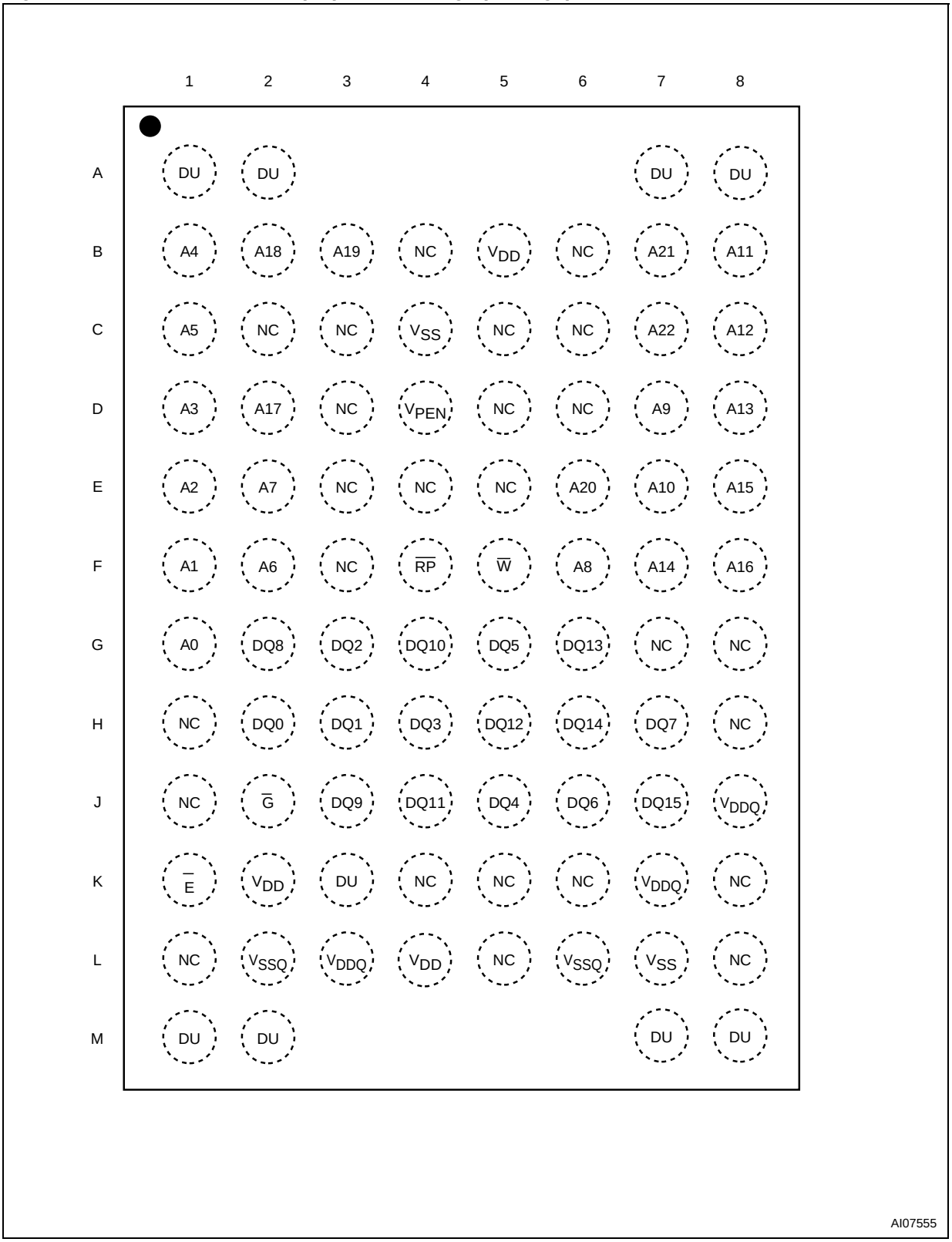
Note: Pin 2 (E1 for a single M58LW064D device) and pin 29 (E2 for a single M58LW064D device) are NC (not connected). They should be tied to ground (V_{SS}) to assure compatibility with a single chip 128Mbit device.

Figure 4. TBGA64 Connections (Top view through package)



Note: Ball B8 (E1 for a single M58LW064D device) and ball H1(E2 for a single M58LW064D device) are NC (not connected). They should be tied to ground (V_{SS}) to assure compatibility with a single chip 128Mbit device.

Figure 5. LFBGA Connections (Top view through package)



Note: 1. The BYTE, STS and A0 connections are not available with the LFBGA88 package.

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Input (A0). The A0 address input is used to select the higher or lower Byte in x8 mode. It is not used in x16 mode (where A1 is the Lowest Significant bit).

The A0 address input is not available with the LFBGA88 package.

Address Inputs (A1-A22). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

The device must be enabled (refer to Table 3, M30LW128D Device Enable) when selecting the addresses. The address inputs are latched on the rising edge of Write Enable or Chip Enable, $\overline{E}$, whichever occurs first.

Address Input (A23). Address Input A23 is used to select between the two internal memories. When it is High, V_{IH}, it selects the Upper Memory, when it is Low, V_{IL}, it selects the Lower Memory. Refer to Memory Enable section for more details.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, $\overline{E}$, whichever occurs first.

When the device is enabled and Output Enable is low, V_{IL}, the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the device is deselected, Output Enable is high, V_{IH}, or the Reset/Power-Down signal is low, V_{IL}. When the Program/Erase Controller is active the Ready/Busy status is given on DQ7.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. The M30LW128D stacked memory uses the A23 address line and the external Chip Enable, $\overline{E}$, to select and enable the internal memories. Refer to Memory Enable section and Table 3, for more details.

When the Chip Enable deselects the memory, power consumption is reduced to the Standby level, I_{DD1}.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation. When Output Enable, $\overline{G}$, is at V_{IH} the outputs are high impedance.

Write Enable ($\overline{W}$). The Write Enable input, $\overline{W}$, controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable.

Reset/Power-Down ($\overline{RP}$). The Reset/Power-Down signal can be used to apply a Hardware Reset to the memory.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL}, for at least t_{PLPH}. When Reset/Power-Down is Low, V_{IL}, the Status Register information is cleared and the power consumption is reduced to power-down level. The device is deselected and outputs are high impedance. If Reset/Power-Down goes low, V_{IL},during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect the operation is aborted and the data may be corrupted. In this case the STS pin stays low, V_{IL}, for a maximum timing of $t_{PLPH} + t_{PHBH}$, until the completion of the Reset/Power-Down pulse.

After Reset/Power-Down goes High, V_{IH}, the device will be ready for Bus Read and Bus Write operations after t_{PHQV}. Note that STS does not fall during a reset, see Ready/Busy Output section.

In an application, it is recommended to associate Reset/Power-Down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the device is performing an Erase or Program operation, the device may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

Byte/Word Organization Select ($\overline{BYTE}$). The Byte/Word Organization Select signal is used to switch between the x8 and x16 bus widths of the memory. When Byte/Word Organization Select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

The Byte/Word Organization Select signal is not available with the LFBGA88 package.

Status/(Ready/Busy) (STS). The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes:

- Ready/Busy - the pin is Low, V_{OL}, during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.

- Status - the pin gives a pulsing signal to indicate the end of a Program or Block Erase operation.

After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured for Status mode using the Configure STS command.

When the Program/Erase Controller is idle, or suspended, STS can float High through a pull-up resistor. The use of an open-drain output allows the STS pins from several devices to be connected to a single pull-up resistor (a Low will indicate that one, or more, of the memories is busy).

STS is not Low during a reset unless the reset was applied when the Program/Erase controller was active.

The STS signal is not available with the LFBGA88 package.

Program/Erase Enable (V_{PEN}). The Program/Erase Enable input, V_{PEN}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid any condition that would result in data corruption.

V_{SS} Ground. Ground, V_{SS}, is the reference for the core power supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 10, AC Measurement Load Circuit.

MEMORY ENABLE

Each internal M58LW064D memory has 3 Chip Enable signals to allow up to 4 memories to be connected together without the use of additional glue logic, see Table 2, Single M58LW064D Device Enable. In this way the address space is contiguous and the microcontroller only requires one Chip Enable, $\overline{E}$, to control both memories.

Figure 6 shows how a 128Mbit Stacked Flash memory is created using two M58LW064D memories. One of the memories is located in the Upper Address space and is referred to as the Upper Memory, the other is located in the lower address space and is referred to as the Lower Memory, see Figure 7, Block Addresses.

The E0, E1 and E2 Chip Enables of each M58LW064D memory are connected internally, as shown in Figure 6.

The external signal A23 is used to select between the Upper and Lower memories. A23 is connected to E2 of the Upper Memory and to E1 of the Lower Memory.

E1 of the Upper Memory is always connected to V_{DD} while E2 of the Lower Memory is always connected to V_{SS}.

The external Chip Enable, $\overline{E}$, is used to enable or disable the memory selected by A23, see Table 3, M30LW128D Device Enable. $\overline{E}$ is connected to the E0 signal of both memories.

The M30LW128D (TSOP56 and TBGA64 packages only) supports both x8 and x16 bus widths. It is also possible to have a x32 bus width by connecting two x16 bus width M30LW128D devices together. Note that the two M30LW128D devices must use the same E0 as Chip Enable, as E1 and E2 are not connected internally.

Table 2. Single M58LW064D Device Enable, E2, E1 and E0

E2	E1	E0	Device
V_{IL}	V_{IL}	V_{IL}	Enabled
V_{IL}	V_{IL}	V_{IH}	Disabled
V_{IL}	V_{IH}	V_{IL}	Disabled
V_{IL}	V_{IH}	V_{IH}	Disabled
V_{IH}	V_{IL}	V_{IL}	Enabled
V_{IH}	V_{IL}	V_{IH}	Enabled
V_{IH}	V_{IH}	V_{IL}	Enabled
V_{IH}	V_{IH}	V_{IH}	Disabled

Table 3. M30LW128D Device Enable, A23 and $\overline{E}$

A23	Internal Signals		Chip Enable, $\overline{E}$	Upper Memory	Lower Memory
$E2_{UM} = E1_{LM}$ (1)	$E1_{UM}$ (1)	$E2_{LM}$ (1)	$E0_{UM} = E0_{LM}$ (1)		
V_{IL}	V_{DD} (V_{IH})	V_{SS} (V_{IL})	V_{IL}	Disabled	Enabled
V_{IL}			V_{IH}	Disabled	Disabled
V_{IH}			V_{IL}	Enabled	Disabled
V_{IH}			V_{IH}	Disabled	Disabled

Note: 1. UM = Upper Memory, LM = Lower Memory.

Figure 6. Stacked Flash Memory

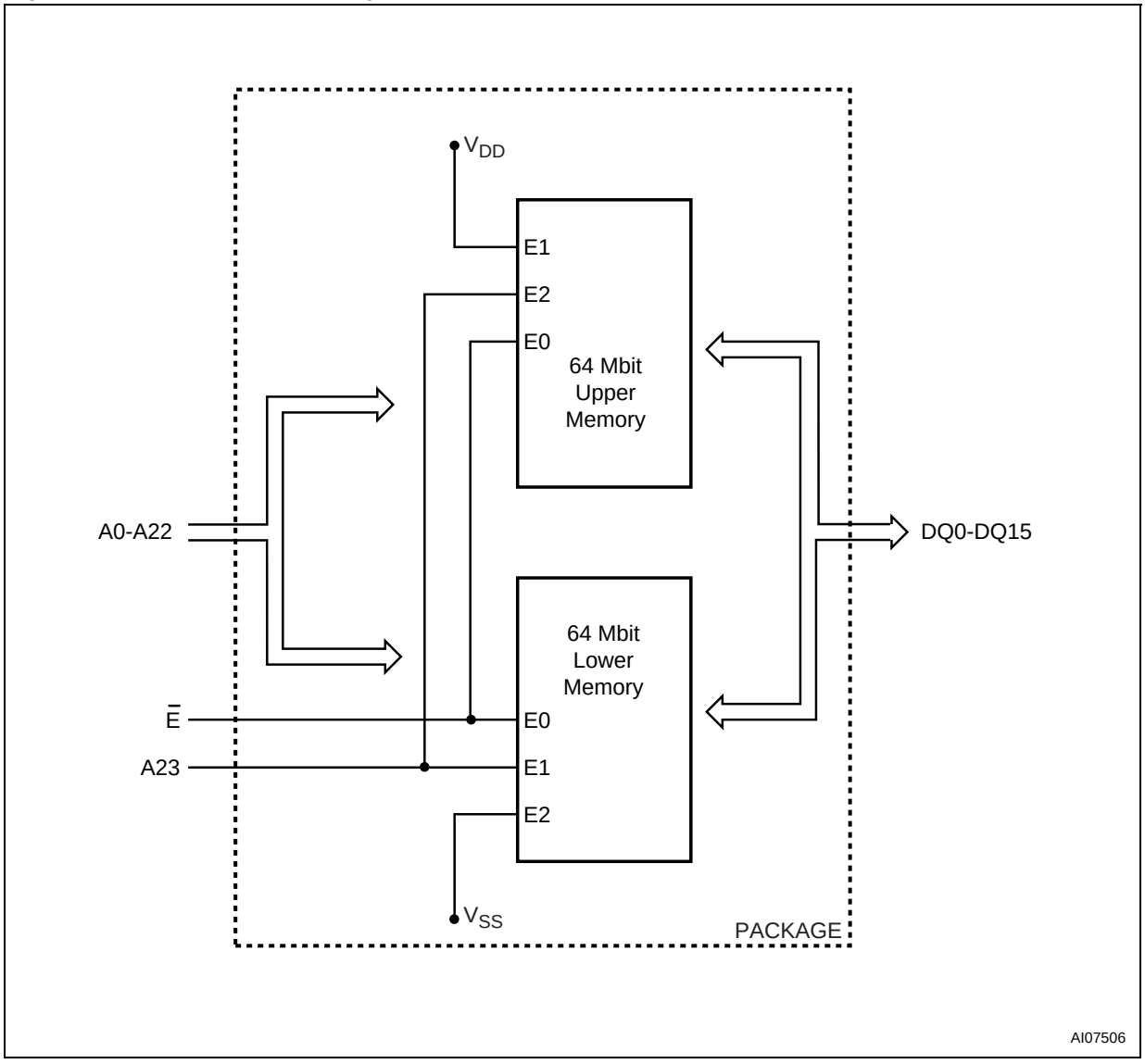
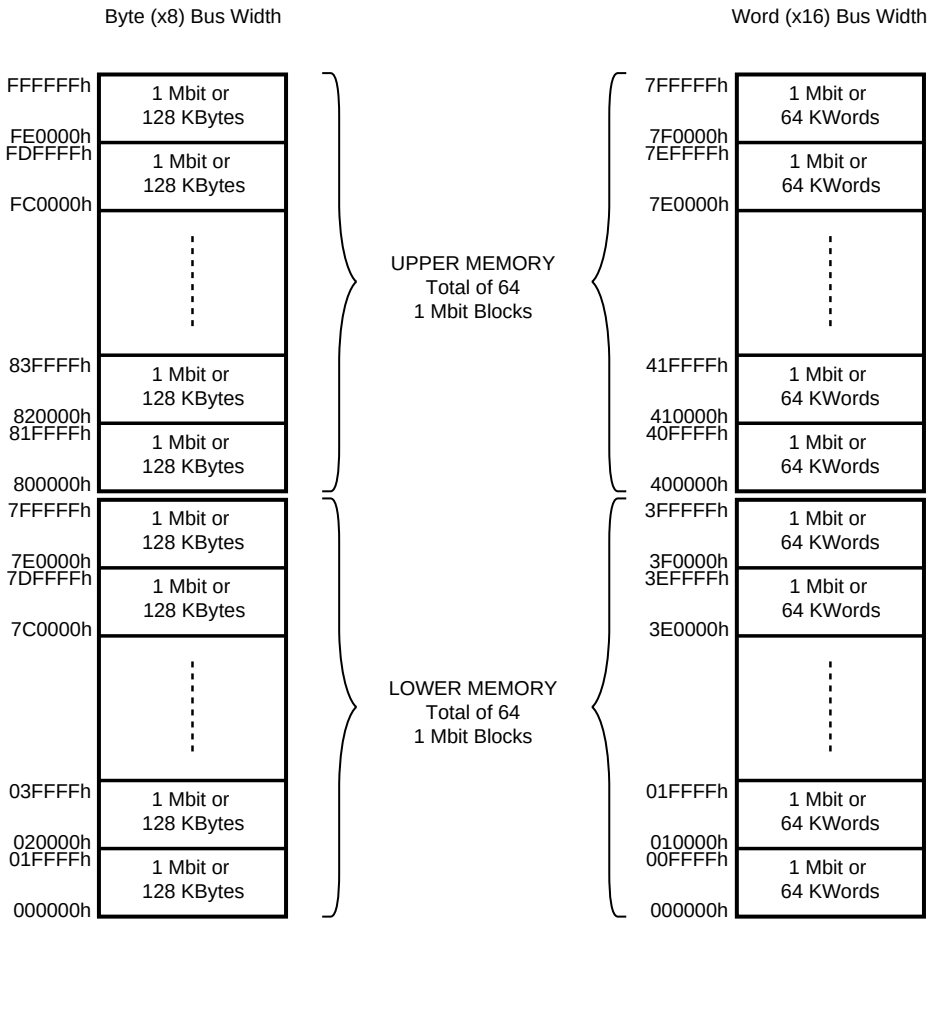


Figure 7. Block Addresses



Note: Also see Appendix A, Table 25 for a full listing of the Block Addresses

BUS OPERATIONS

There are 6 bus operations that control each memory. Each of these is described in this section, see Tables 4, Bus Operations, for a summary.

On Power-up or after a Hardware Reset the device defaults to Read Array mode (Page Read).

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the device and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers (Electronic Signature, Status Register, CFI and Block Protection Status) in the Command Interface.

A valid bus operation involves setting the desired address on the Address inputs, enabling the device (refer to Table 3), applying a Low signal, V_{IL}, to Output Enable and keeping Write Enable High, V_{IH}.

The Data Inputs/Outputs will output the value, see Figure 11, Bus Read AC Waveforms, and Table 16, Bus Read AC Characteristics, for details of when the output becomes valid.

Page Read. Page Read operations are used to read from several addresses within the same memory page.

Each memory page is a 4 Words or 8 Bytes and has the same A3-A22. In x8 mode only A0, A1 and A2 may change, in x16 mode only A1 and A2 may change.

Valid bus operations are the same as Bus Read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. See Figure 12, Page Read AC Waveforms and Table 17, Page Read AC Characteristics for details on when the outputs become valid.

Bus Write. Bus Write operations write to the Command Interface in order to send commands to the device or to latch addresses and input data to program.

A valid Asynchronous Bus Write operation begins by setting the desired address on the Address Inputs and enabling the device (refer to Chip Enable section).

Both the Address Inputs and Data Input/Outputs are latched by the Command Interface on the rising edge of Write Enable or Chip Enable, whichever occurs first.

Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 13, and 14, Write AC Waveforms, and Tables 18 and 19, Write and Chip Enable Controlled Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when the Output Enable is High.

Standby. When Chip Enable is High, V_{IH}, the device enters Standby mode and the Data Inputs/Outputs pins are placed in the high impedance state regardless of Output Enable or Write Enable. The Supply Current is reduced to the Standby Supply Current, I_{DD1}.

During Program or Erase operations the device will continue to use the Program/Erase Supply Current, I_{DD3}, for Program or Erase operations until the operation completes.

Automatic Low Power. If there is no change in the state of the bus for a short period of time during Asynchronous Bus Read operations the device enters Auto Low Power mode where the internal Supply Current is reduced to the Auto-Standby Supply Current, I_{DD5}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Automatic Low Power is only available in Asynchronous Read modes.

Power-Down. The device is in Power-Down mode when Reset/Power-Down, $\overline{RP}$, is Low. The power consumption is reduced to the Power-Down level, I_{DD2}, and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Table 4. Bus Operations

Bus Operation	Memory Enabled	A23	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	A1-A22 (x16) A0-A22 (x8)	DQ0-DQ15 (x16) DQ0-DQ7 (x8)(1)
Bus Read	Upper	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High	Address	Data Output
	Lower	V_{IL}						
Page Read	Upper	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High	Address	Data Output
	Lower	V_{IL}						
Bus Write	Upper	V_{IH}	V_{IL}	V_{IH}	V_{IL}	High	Address	Data Input
	Lower	V_{IL}						
Output Disable	Output disabled	X	V_{IL}	V_{IH}	V_{IH}	High	X	High Z
Standby	Device disabled	X	V_{IH}	X	X	High	X	High Z
Power-Down	Device disabled	X	X	X	X	V_{IL}	X	High Z

Note: 1. DQ8-DQ15 are High Z in x8 mode.
2. X = Don't Care V_{IL} or V_{IH}. High = V_{IH} or V_{HH}.

COMMAND INTERFACE

All Bus Write operations to the device are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. As the device contains two internal memories care must be taken to issue the commands to the correct address. Commands issued with A23 High will be addressed to the Upper Memory, commands issued with A23 Low will be addressed to the Lower Memory.

The Commands are summarized in Table 5, Commands. Refer to Table 5 in conjunction with the text descriptions below.

After power-up or a Reset operation the device enters Read mode.

Read Memory Array Command. The Read Memory Array command is used to return the device to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the device to Read mode. Once the command is issued the device remains in Read mode until another command is issued. From Read mode Bus Read operations will access the memory arrays. After power-up or a reset the device defaults to Read Array mode (Page Read).

While the Program/Erase Controller is executing a Program, Erase, Block Protect, Blocks Unprotect or Protection Register Program operation the device will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code, the Block Protection Status and the Protection Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code, the Block Protection Status or the Protection Register until another command is issued. Refer to Table 7, Read Electronic Signature, Tables 8 and 9, Word and Byte-wide Read Protection Register and Figure 8, Protection Register Memory Map for information on the addresses.

Read Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See Appendix B, Tables 26, 27, 28, 29, 30 and 31 for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command. The Read Status Register command is used to read the Status Register. One Bus Write cycle is required to issue the Read Status Register command. As the device contains two Status Registers (one for each internal memory) the command must be issued to the same address as the previous operation (Block Erase, Write to Buffer, Word Program etc.). Once the command is issued subsequent Bus Read operations to the same internal memory (A23 Low or A23 High depending on where the command was issued to) read the Status Register until another command is issued. If the Bus Read operation is issued to the other internal memory, then the other Status Register will be read, giving the status of the last command issued in the other internal memory.

The Status Register information is present on the output data bus (DQ1-DQ7) when the device is enabled and Output Enable is Low, V_{IL}.

See the section on the Status Register and Table 11 for details on the definitions of the Status Register bits

Clear Status Register Command. The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command. The command must be issued to the same address as the previous operation (Block Erase, Write to Buffer, Word Program etc.).

The bits in the Status Register are sticky and do not automatically return to '0' when a new Write to Buffer and Program, Erase, Block Protect, Block Unprotect or Protection Register Program command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During Erase, the device being erased will only accept the Read Status Register and Program/Erase Suspend commands, ignoring all other commands. The device not being erased will accept

any command. Typical Erase times are given in Table 10.

See Appendix C, Figure 21, Block Erase Flowchart and Pseudo Code, for a suggested flowchart on using the Block Erase command.

Word/Byte Program Command. The Word/Byte Program command is used to program a single Word or Byte in the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Word Program command, the second write cycle latches the address and data to be programmed in the internal state machine and starts the Program/Erase Controller.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

Write to Buffer and Program Command. The Write to Buffer and Program command is used to program the memory array. If the command is issued with A23 High the Upper Memory will be programmed, if the command is issued with A23 Low the Lower Memory will be programmed.

Up to 16 Words/32 Bytes can be loaded into the Write Buffer and programmed into the memory array. Each Write Buffer has the same A5-A22 addresses. In Byte-wide mode only A0-A4 may change, in Word-wide mode only A1-A4 may change.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words/Bytes to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word into the Write Buffer. The addresses must have the same A5-A22.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

See Appendix C, Figure 19, Write to Buffer and Program Flowchart and Pseudo Code, for a suggested flowchart on using the Write to Buffer and Program command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Write to Buffer and Program or Erase operation. The command will only be accepted during a Program or an Erase operation. It can be issued at any time during an Erase operation but will only be accepted during a Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. The command must be issued to the same address as the current Program or Erase operation. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (bit 7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the device will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing, it is possible for the operation to complete. Once the Program/Erase Controller Status bit (bit 7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (bit 2) or the Erase Suspend Status bit (bit 6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see Table 10.

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Word Program, Write to Buffer and Program, and Program Suspend commands will also be accepted.

When one of the devices is being Program or Erase Suspended, any command issued to the other internal Flash memory will be accepted. When a program operation is completed inside a

Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See Appendix C, Figure 20, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 22, Erase Suspend & Resume Flowchart and Pseudo Code, for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. The command must be issued to the same address as the Program/Erase Suspend command. Once the command is issued subsequent Bus Read operations read the Status Register.

Block Protect Command. The Block Protect command is used to protect a block and prevent Program or Erase operations from changing the data in it. Two Bus Write cycles are required to issue the Block Protect command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the device will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

The Block Protection bits are non-volatile, once set they remain set through reset and power-down/power-up. They are cleared by a Blocks Unprotect command.

See Appendix C, Figure 23, Block Protect Flowchart and Pseudo Code, for a suggested flowchart on using the Block Protect command.

Blocks Unprotect Command. The Blocks Unprotect command is used to unprotect all of the blocks. To unprotect all of the blocks in both of the internal memories the command must be issued to both memories, that is first with A23 Low and then with A23 High.

Four Bus Write cycles are required to issue the Blocks Unprotect command; the first two are written with A23 Low, the second two are written with A23 High. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Blocks Unprotect operation the device will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in Table 10.

See Appendix C, Figure 24, Blocks Unprotect Flowchart and Pseudo Code, for a suggested flowchart on using the Blocks Unprotect command.

Protection Register Program Command.

The Protection Register Program command is used to Program the 64 bit user segment of the Protection Register. Only the lower address Protection Register is available to the customer (A23 Low), the other Protection Register is reserved.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The user-programmable segment can be locked by programming bit 1 of the Protection Register Lock location to ‘0’ (see Table 8 and x for Word-wide and Byte-wide protection addressing). Bit 0 of the Protection Register Lock location locks the factory programmed segment and is programmed to ‘0’ in the factory. The locking of the Protection Register is not reversible, once the lock bits are programmed no further changes can be made to the values stored in the Protection Register, see Figure 8, Protection Register Memory Map. Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. See Appendix C, Figure 25, Protection Register Program Flowchart and Pseudo Code, for the flowchart for using the Protection Register Program command.

Configure STS Command.

The Configure STS command is used to configure the Status/(Ready/Busy) pin. It has to be configured for both internal memories, that is the command has to be issued first with A23 Low and then with A23 High. After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured in Status mode using the Configure STS command (refer to Status/(Ready/Busy) section for more details.

Four Bus Write cycles are required to issue the Configure STS command. The first two cycles

must be written with A23 Low and the second two with A23 High.

- The first bus cycle sets up the Configure STS command. A23 must be Low.
- The second Bus Write cycle specifies one of the four possible configurations, A23 must be Low, (refer to Table 6, Configuration Codes):
  - Ready/Busy mode
  - Pulse on Erase complete mode
  - Pulse on Program complete mode
  - Pulse on Erase or Program complete mode
- The third Bus Write cycle re-sets up the Configure STS command. This time A23 must be High.
- The fourth re-specifies the configuration code given in the second Bus Write cycle. A23 must be High.

The device will not accept the Configure STS command while the Program/Erase controller is busy or during Program/Erase Suspend. When STS pin is pulsing it remains Low for a typical time of 250ns. Any invalid Configuration Code will set an error in the Status Register.

The Configure STS command is not available with the LFBGA88 package.

Table 5. Commands

Command	Cycles	Bus Operations											
		1st Cycle			2nd Cycle			Subsequent			Final		
		Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	2	Write	RA	FFh	Read	RA	RD						
Read Electronic Signature	≥ 2	Write	X	90h	Read	IDA(2)	IDD(2)						
Read Status Register	2	Write	PA/BA	70h	Read	PA/BA	SRD						
Read Query	≥ 2	Write	X	98h	Read	QA(3)	QD(3)						
Clear Status Register	1	Write	PA/BA	50h									
Block Erase	2	Write	BA	20h	Write	BA	D0						
Word/Byte Program	2	Write	PA	40h 10h	Write	PA	PD						
Write to Buffer and Program	4+N	Write	BA	E8h	Write	BA	N	Write	PA	PD	Write	BA	D0h
Program/Erase Suspend	1	Write	PA/BA	B0h									
Program/Erase Resume	1	Write	PA/BA	D0h									
Block Protect	2	Write	BA	60h	Write	BA	01h						
Blocks Unprotect	4	Write	000000h	60h	Write	000000h	D0h	Write	400000h	60h	Write	400000h	D0h
Protection Register Program	2	Write	PRA	C0h	Write	PRA	PRD						
Configure STS command(4)	4	Write	000000h	B8h	Write	000000h	CC	Write	400000h	B8h	Write	400000h	CC

Note: 1. X Don't Care; RA Read Address, RD Read Data, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address, PD Program Data, QA Query Address, QD Query Data, BA Any address in Block, PRA Protection register address, PRD Protection Register Data, CC Configuration Code. The shaded areas highlight the differences with a single M58LW064D memory.
2. For Identifier addresses and data refer to Table 7, Read Electronic Signature.
3. For Query Address and Data refer to Appendix B, CFI.
4. Not available with LFBGA88 package.

Table 6. Configuration Codes

Configuration Code	DQ1	DQ2	Mode	STS Pin	Description
00h	0	0	Ready/Busy	V_{OL} during P/E operations Hi-Z when the memory is ready	The STS pin is Low during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
01h	0	1	Pulse on Erase complete	Pulse Low then High when operation completed(2)	Supplies a system interrupt pulse at the end of a Block Erase operation.
02h	1	0	Pulse on Program complete		Supplies a system interrupt pulse at the end of a Program operation.
03h	1	1	Pulse on Erase or Program complete		Supplies a system interrupt pulse at the end of a Block Erase or Program operation.

Note: 1. DQ2-DQ7 are reserved
2. When STS pin is pulsing it remains Low for a typical time of 250ns.

Table 7. Read Electronic Signature

Code	Bus Width	Address (A23-A1)(3)	Data (DQ15-DQ0)
Manufacturer Code	x8	000000h	20h
	x16		0020h
Device Code	x8	000001h	17h
	x16		8817h
Block Protection Status	x8	SBA(1)+02h	00h (Block Unprotected) 01h (Block Protected)
	x16		0000h (Block Unprotected) 0001h (Block Protected)
Protection Register	x8, x16	000080h(2)	PRD(1)

Note: 1. SBA is the Start Base Address of each block, PRD is Protection Register Data.
2. Base Address, refer to Figure 8 and Tables 8 and 9 for more information. A23 must be Low to address the customer's Protection Register. The other Protection Register is reserved.
3. A0 is not used in Read Electronic Signature in either x8 or x16 mode. The data is always presented on the lower byte in x16 mode.

Figure 8. Protection Register Memory Map

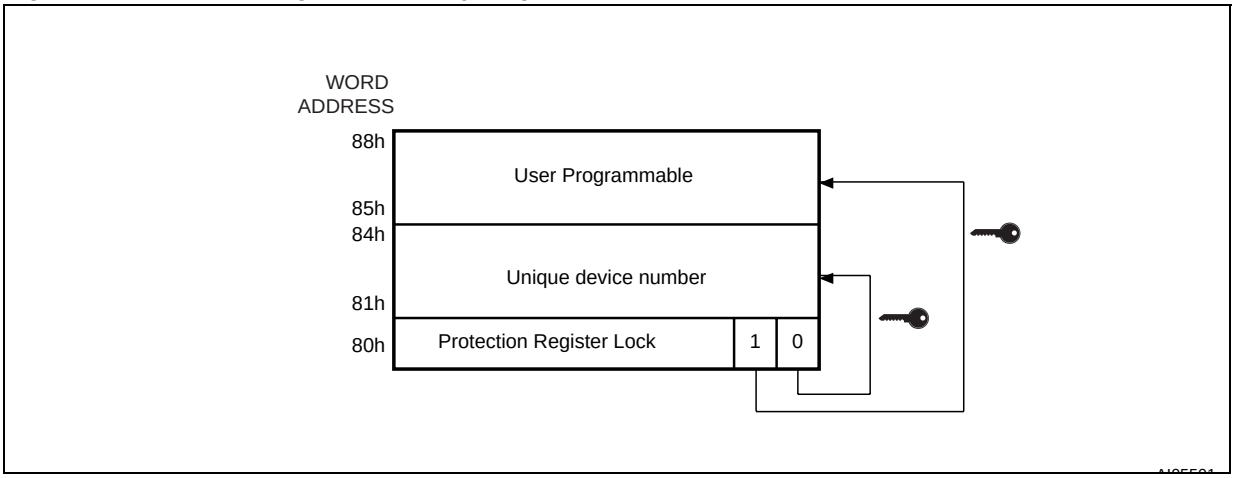


Table 8. Word-Wide Read Protection Register

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
Lock	Factory, User	1	0	0	0	0	0	0	0
0	Factory (Unique ID)	1	0	0	0	0	0	0	1
1	Factory (Unique ID)	1	0	0	0	0	0	1	0
2	Factory (Unique ID)	1	0	0	0	0	0	1	1
3	Factory (Unique ID)	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Table 9. Byte-Wide Read Protection Register

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
Lock	Factory, User	1	0	0	0	0	0	0	0
Lock	Factory, User	1	0	0	0	0	0	0	0
0	Factory (Unique ID)	1	0	0	0	0	0	0	1
1	Factory (Unique ID)	1	0	0	0	0	0	0	1
2	Factory (Unique ID)	1	0	0	0	0	0	1	0
3	Factory (Unique ID)	1	0	0	0	0	0	1	0
4	Factory (Unique ID)	1	0	0	0	0	0	1	1
5	Factory (Unique ID)	1	0	0	0	0	0	1	1
6	Factory (Unique ID)	1	0	0	0	0	1	0	0
7	Factory (Unique ID)	1	0	0	0	0	1	0	0
8	User	1	0	0	0	0	1	0	1
9	User	1	0	0	0	0	1	0	1
A	User	1	0	0	0	0	1	1	0
B	User	1	0	0	0	0	1	1	0
C	User	1	0	0	0	0	1	1	1
D	User	1	0	0	0	0	1	1	1
E	User	1	0	0	0	1	0	0	0
F	User	1	0	0	0	1	0	0	0

Table 10. Program/Erase Times and Program/Erase Endurance Cycles

Parameters	M30LW128D			Unit
	Min	Typ(1,2)	Max(2)	
Block (1Mb) Erase		1.2	4.8(4)	s
Chip Program (Write to Buffer)		98	290(4)	s
Chip Erase Time		148	440 (4)	s
Program Write Buffer		192 (3)	576 (4)	µs
Word/Byte Program Time (Word/Byte Program command)		16	48 (4)	µs
Program Suspend Latency Time		1	20 (5)	µs
Erase Suspend Latency Time		1	25 (5)	µs
Block Protect Time		18	30 (5)	µs
Blocks Unprotect Time		0.75	1.2 (5)	s
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	20			years

Note: 1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Effective byte programming time 6µs, effective word programming time 12µs.
4. Maximum value measured at worst case conditions for both temperature and V_{DD} after 100,000 program/erase cycles.
5. Maximum value measured at worst case conditions for both temperature and V_{DD}.

STATUS REGISTER

The Status Register provides information on the current or previous Program, Erase, Block Protect or Blocks Unprotect operation. The various bits in the Status Register convey information and errors on the operation. They are output on DQ7-DQ0.

To read the Status Register the Read Status Register command can be issued. The Status Register is automatically read after Program, Erase, Block Protect, Blocks Unprotect and Program/Erase Resume commands. As the device contains two Status Registers (one for each internal memory) the Status Register must be read at the same address as the previous operation.

The contents of the Status Register can be updated during an Erase or Program operation by toggling the Output Enable pin or by dis-activating and then reactivating the device (refer to Table 3).

Status Register bits 5, 4, 3 and 1 are associated with various error conditions and can only be reset with the Clear Status Register command. The Status Register bits are summarized in Table 11, Status Register Bits. Refer to Table 11 in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low, V_{OL}, the Program/Erase Controller is active and all other Status Register bits are High Impedance; when the bit is High, V_{OH}, the Program/Erase Controller is inactive.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, Block Protect and Blocks Unprotect operations the Program/Erase Controller Status bit can be polled to find the end of the operation. The other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status and Block Protection Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended and is waiting to be resumed. The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the memory may still complete the operation rather than entering the Suspend mode.

When the Erase Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the device has failed to verify that the block has erased correctly or that all blocks have been unprotected successfully. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Erase Status bit is Low, V_{OL}, the device has successfully verified that the block has erased correctly or all blocks have been unprotected successfully. When the Erase Status bit is High, V_{OH}, the erase operation has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH}.

- If only the Erase Status bit (bit 5) is set High, V_{OH}, then the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly or that all the blocks have been unprotected successfully.
- If the failure is due to an erase or blocks unprotect with V_{PEN} low, V_{OL}, then V_{PEN} Status bit (bit 3) is also set High, V_{OH}.
- If the failure is due to an erase on a protected block then Block Protection Status bit (bit 1) is also set High, V_{OH}.
- If the failure is due to a program or erase incorrect command sequence then Program Status bit (bit 4) is also set High, V_{OH}.

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program or Block Protect failure. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Status bit is Low, V_{OL}, the device has successfully verified that the Write Buffer has programmed correctly or the block is protected. When the Program Status bit is High, V_{OH}, the program or block protect operation has failed. Depending on the cause of the failure other Status Register bits may also be set to High, V_{OH}.

- If only the Program Status bit (bit 4) is set High, V_{OH}, then the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that the Write Buffer has programmed correctly or that the Block is protected.
- If the failure is due to a program or block protect with V_{PEN} low, V_{OL}, then V_{PEN} Status bit (bit 3) is also set High, V_{OH}.
- If the failure is due to a program on a protected block then Block Protection Status bit (bit 1) is also set High, V_{OH}.
- If the failure is due to a program or erase incorrect command sequence then Erase Status bit (bit 5) is also set High, V_{OH}.

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

V_{PEN} Status (Bit 3). The V_{PEN} Status bit can be used to identify if a Program, Erase, Block Protection or Block Unprotection operation has been attempted when V_{PEN} is Low, V_{IL}.

When the V_{PEN} Status bit is Low, V_{OL}, no Program, Erase, Block Protection or Block Unprotection operations have been attempted with V_{PEN} Low, V_{IL}, since the last Clear Status Register command, or hardware reset. When the V_{PEN} Status bit is High, V_{OH}, a Program, Erase, Block Protection or Block Unprotection operation has been attempted with V_{PEN} Low, V_{IL}.

Once set High, the V_{PEN} Status bit can only be reset by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program, Erase, Block Protection or Block Unprotection command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended and is waiting to be resumed. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive); after a Program/Erase Suspend command is issued the device may still complete the operation rather than entering the Suspend mode.

When the Program Suspend Status bit is Low, V_{OL}, the Program/Erase Controller is active or has completed its operation; when the bit is High, V_{OH}, a Program/Erase Suspend command has been issued and the device is waiting for a Program/ Erase Resume command.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a protected block.

When the Block Protection Status bit is Low, V_{OL}, no Program or Erase operations have been attempted to protected blocks since the last Clear Status Register command or hardware reset; when the Block Protection Status bit is High, V_{OH}, a Program (Program Status bit 4 set High) or Erase (Erase Status bit 5 set High) operation has been attempted on a protected block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value should be masked.

Table 11. Status Register Bits

OPERATION	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Result (Hex)
Program/Erase Controller active	0	Hi-Z						N/A
Write Buffer not ready	0	Hi-Z						N/A
Write Buffer ready	1	0	0	0	0	0	0	80h
Write Buffer ready in Erase Suspend	1	1	0	0	0	0	0	C0h
Program suspended	1	0	0	0	0	1	0	84h
Program suspended in Erase Suspend	1	1	0	0	0	1	0	C4h
Program/Block Protect completed successfully	1	0	0	0	0	0	0	80h
Program completed successfully in Erase Suspend	1	1	0	0	0	0	0	C0h
Program/Block protect failure due to incorrect command sequence	1	0	1	1	0	0	0	B0h
Program failure due to incorrect command sequence in Erase Suspend	1	1	1	1	0	0	0	F0h
Program/Block Protect failure due to V_{PEN} error	1	0	0	1	1	0	0	98h
Program failure due to V_{PEN} error in Erase Suspend	1	1	0	1	1	0	0	D8h
Program failure due to Block Protection	1	0	0	1	0	0	1	92h
Program failure due to Block Protection in Erase Suspend	1	1	0	1	0	0	1	D2h
Program/Block Protect failure due to cell failure	1	0	0	1	0	0	0	90h
Program failure due to cell failure in Erase Suspend	1	1	0	1	0	0	0	D0h
Erase Suspended	1	1	0	0	0	0	0	C0h
Erase/Blocks Unprotect completed successfully	1	0	0	0	0	0	0	80h
Erase/Blocks Unprotect failure due to incorrect command sequence	1	0	1	1	0	0	0	B0h
Erase/Blocks Unprotect failure due to V_{PEN} error	1	0	1	0	1	0	0	A8h
Erase failure due to Block Protection	1	0	1	0	0	0	1	A2h
Erase/Blocks Unprotect failure due to failed cells in Block	1	0	1	0	0	0	0	A0h
Configure STS error due to invalid configuration code	1	0	1	1	0	0	0	B0h

MAXIMUM RATING

Stressing the device above the ratings listed in Table 12, Absolute Maximum Ratings, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 12. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–55	150	°C
V_{IO}	Input or Output Voltage	–0.6	V_{DDQ} +0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	–0.6	5.0	V
I_{OSC}	Output Short-circuit Current		100(1)	mA

Note: 1. Maximum one output short-circuited at a time and for no longer than 1 second.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 13, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 13. Operating and AC Measurement Conditions

Parameter		M30LW128D		Units
		Min	Max	
Supply Voltage (V_{DD})		2.7	3.6	V
Input/Output Supply Voltage (V_{DDQ})		2.7	3.6	V
Ambient Temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load Capacitance (C_L)		30		pF
Input Pulses Voltages		0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages		0.5 V_{DDQ}		V

Figure 9. AC Measurement Input Output Waveform

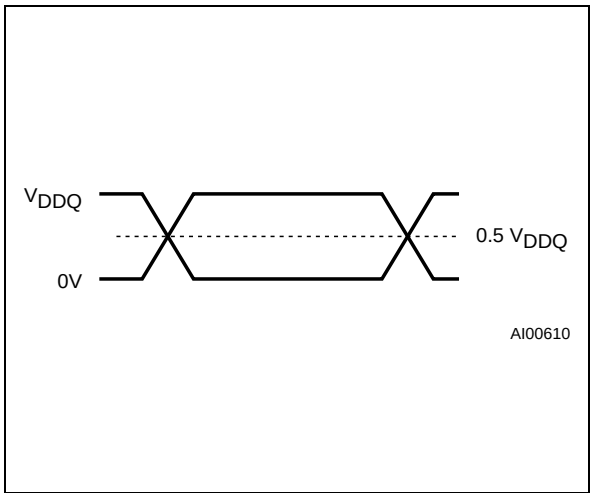


Figure 10. AC Measurement Load Circuit

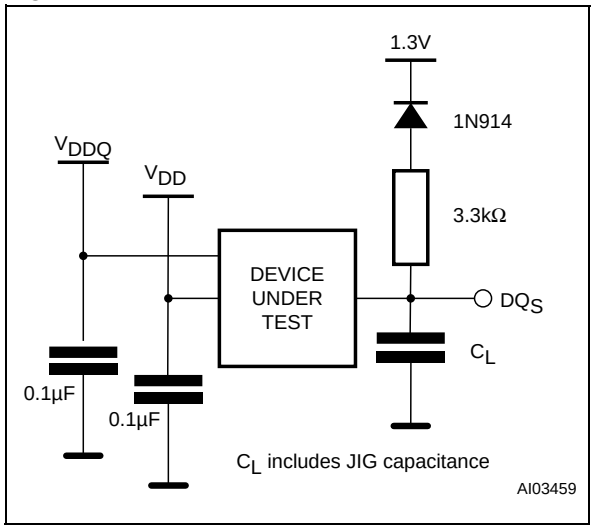


Table 14. Capacitance

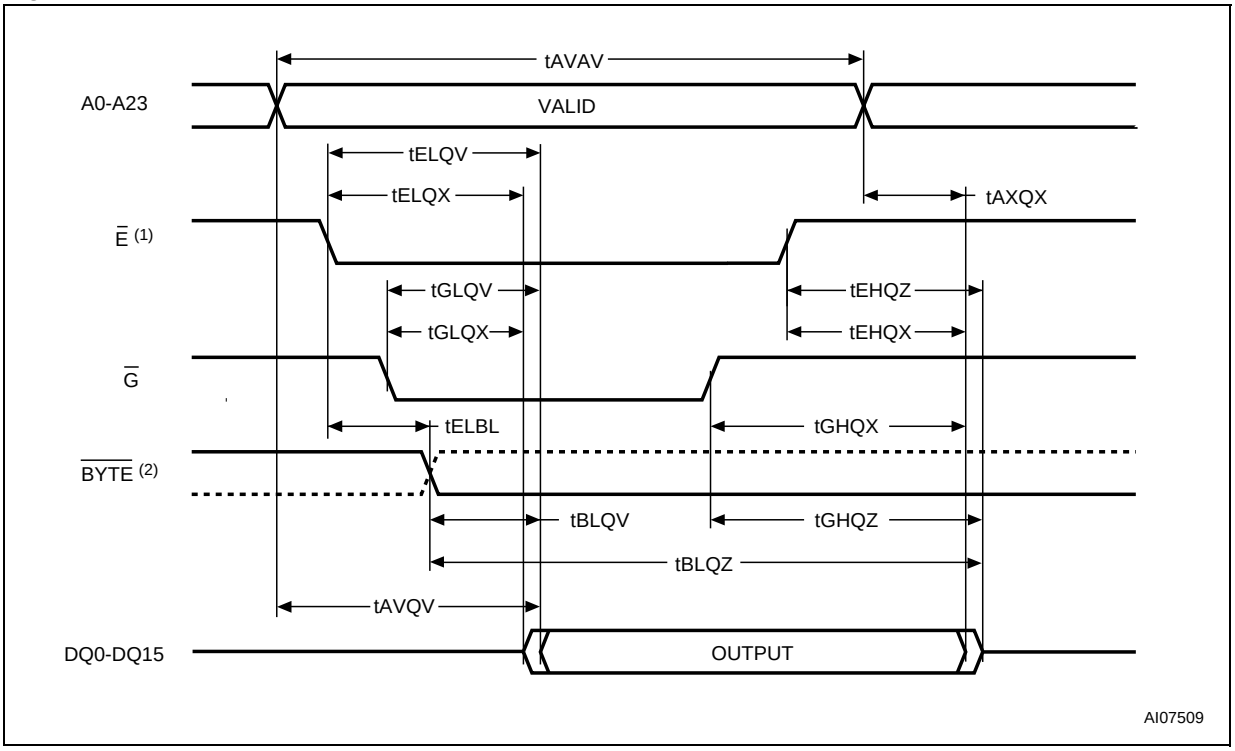
Symbol	Parameter	Test Condition	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Note: 1. T_A = 25°C, f = 1 MHz
2. Sampled only, not 100% tested.

Table 15. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$		±5	µA
I_{DD}	Supply Current (Random Read)	$\overline{E} = V_{IL}$, f=5MHz		20	mA
I_{DDO}	Supply Current (Page Read)	$\overline{E} = V_{IL}$, f=33MHz		29	mA
I_{DD1}	Supply Current (Standby)	$E = V_{IH}$, $\overline{RP} = V_{IH}$		80	µA
I_{DD5}	Supply Current (Auto Low-Power)	$E = V_{IL}$, $\overline{RP} = V_{IH}$		80	µA
I_{DD2}	Supply Current (Reset/Power-Down)	$\overline{RP} = V_{IL}$		80	µA
I_{DD3}	Supply Current (Program or Erase, Block Protect, Block Unprotect)	Program or Erase operation in progress		30	mA
I_{DD4}	Supply Current (Erase/Program Suspend)	$E = V_{IH}$		80	µA
V_{IL}	Input Low Voltage		–0.5	$0.3V_{DDQ}$	V
V_{IH}	Input High Voltage		$0.7V_{DDQ}$	V_{DDQ} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.2		V
V_{LKO}	V_{DD} Supply Voltage (Erase and Program lockout)			2	V
V_{PENH}	V_{PEN} Supply Voltage (block erase, program and block protect)		2.7	3.6	V

Figure 11. Bus Read AC Waveforms

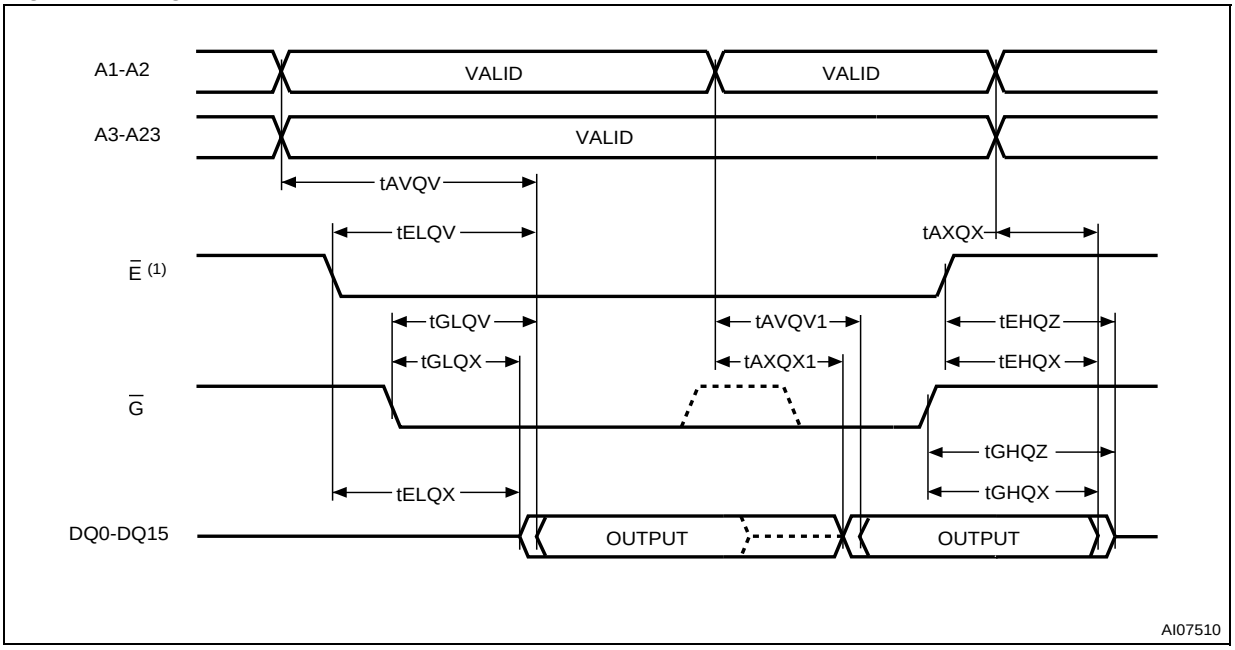


Note: 1. Refer to Table 3 for details of how the device is enabled.
2. BYTE can be Low or High. The BYTE signal is not available with the LFBGA88 package.

Table 16. Bus Read AC Characteristics

Symbol	Parameter	Test Condition		M30LW128D	Unit
				110	
t_{AVAV}	Address Valid to Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	110	ns
t_{AVQV}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	110	ns
t_{AXQX}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	0	ns
t_{BLQV}	Byte Low (or High) to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	1	µs
t_{BLQZ}	Byte Low (or High) to Output Hi-Z	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	1	µs
t_{EHQX}	Chip Enable High to Output Transition	$\overline{G} = V_{IL}$	Min	0	ns
t_{EHQZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	25	ns
t_{ELBL}	Chip Enable Low to Byte Low (or High)	$\overline{G} = V_{IL}$	Max	10	ns
t_{ELQX}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	ns
t_{ELQV}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	110	ns
t_{GHQX}	Output Enable High to Output Transition	$\overline{E} = V_{IL}$	Min	0	ns
t_{GHQZ}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	15	ns
t_{GLQX}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	ns
t_{GLQV}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	25	ns

Figure 12. Page Read AC Waveforms



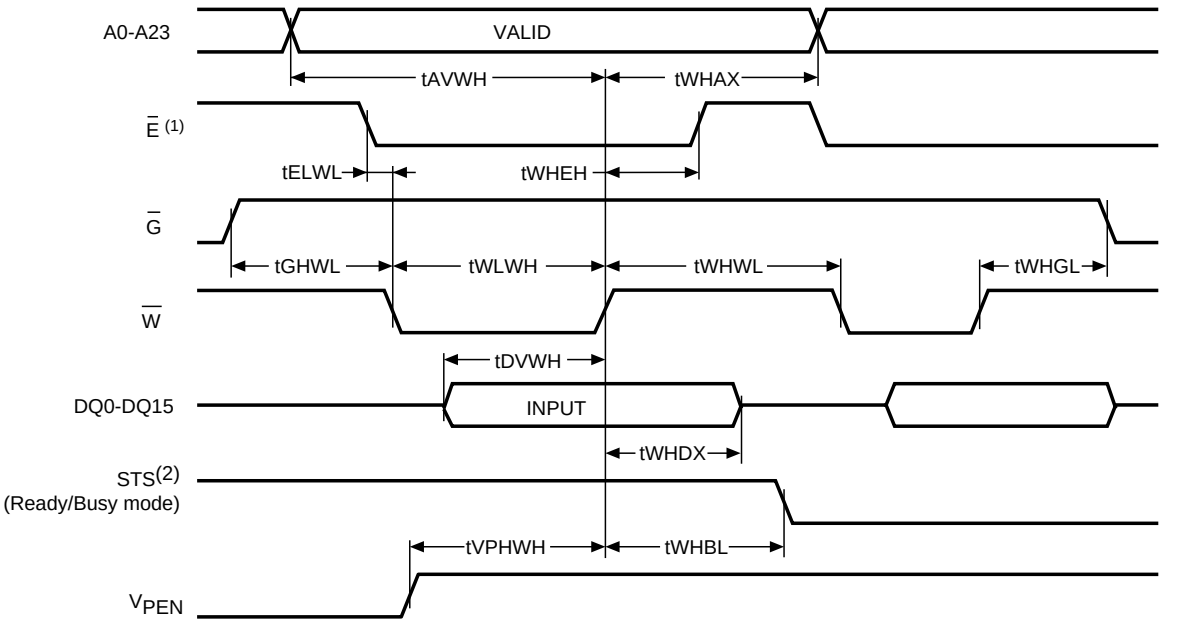
Note: 1. Refer to Table 3 for details of how the device is enabled.

Table 17. Page Read AC Characteristics

Symbol	Parameter	Test Condition		M30LW128D	Unit
				110	
t_{AXQX1}	Address Transition to Output Transition	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	6	ns
t_{AVQV1}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	25	ns

Note: For other timings see Table 16, Bus Read AC Characteristics.

Figure 13. Write AC Waveform, Write Enable Controlled

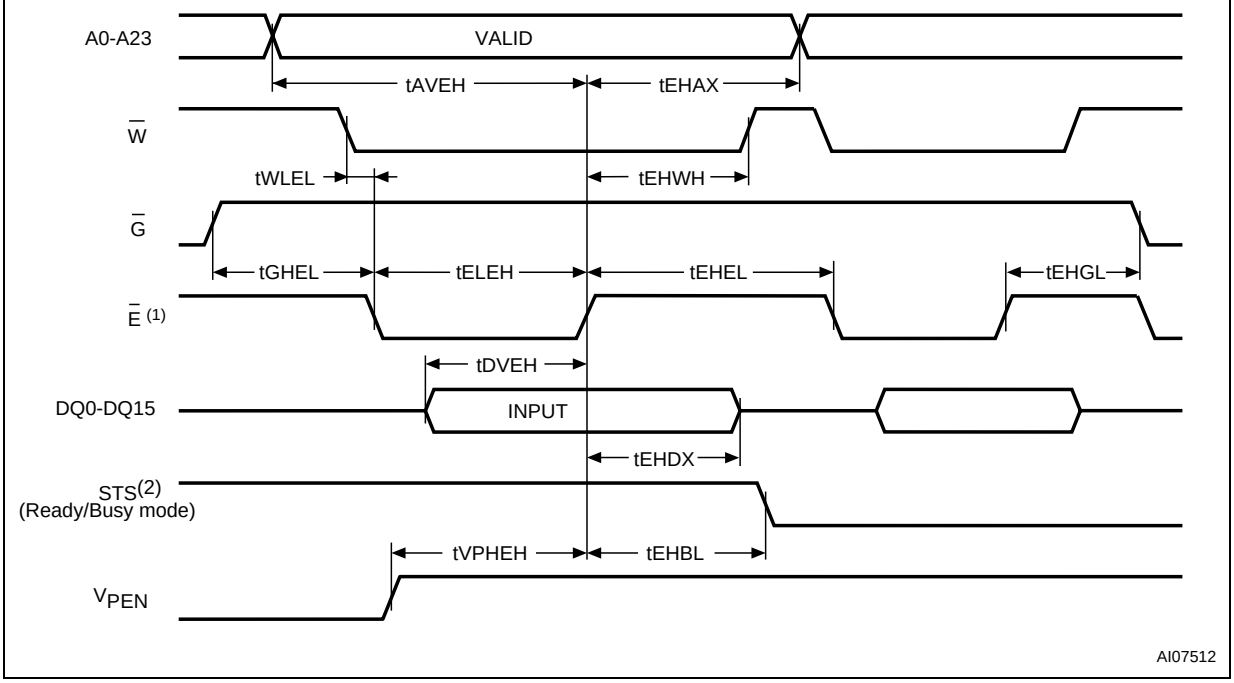


Note: 1. Refer to Table 3 for details of how the device is enabled.
2. Not available with the LFBGA88 package.

Table 18. Write AC Characteristics, Write Enable Controlled

Symbol	Parameter	Test Condition		M30LW128D	Unit
				110	
t_{AVWH}	Address Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	ns
t_{DVWH}	Data Input Valid to Write Enable High	$\overline{E} = V_{IL}$	Min	50	ns
t_{ELWL}	Chip Enable Low to Write Enable Low		Min	0	ns
t_{VPHWH}	Program/Erase Enable High to Write Enable High		Min	0	ns
t_{WHAX}	Write Enable High to Address Transition	$\overline{E} = V_{IL}$	Min	0	ns
t_{WHBL}	Write Enable High to Status/(Ready/Busy) low		Max	500	ns
t_{WHDX}	Write Enable High to Input Transition	$\overline{E} = V_{IL}$	Min	0	ns
t_{WHEH}	Write Enable High to Chip Enable High		Min	0	ns
t_{GHWL}	Output Enable High to Write Enable Low		Min	20	ns
t_{WHGL}	Write Enable High to Output Enable Low		Min	35	ns
t_{WHWL}	Write Enable High to Write Enable Low		Min	30	ns
t_{WLWH}	Write Enable Low to Write Enable High	$\overline{E} = V_{IL}$	Min	70	ns

Figure 14. Write AC Waveforms, Chip Enable Controlled

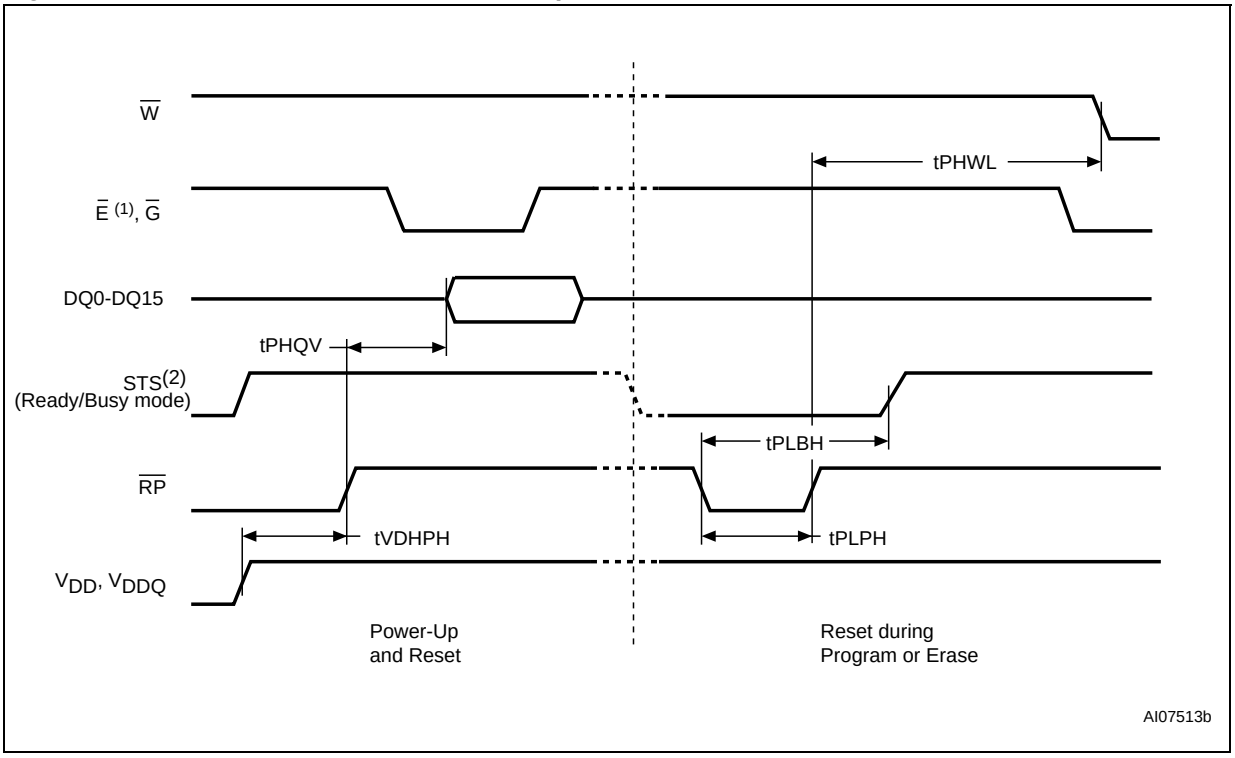


Note: 1. Refer to Table 3 for details of how the device is enabled.
2. Not available with the LFBGA88 package.

Table 19. Write AC Characteristics, Chip Enable Controlled.

Symbol	Parameter	Test Condition		M30LW128D	Unit
				110	
t_{AVEH}	Address Valid to Chip Enable High	$\overline{W} = V_{IL}$	Min	50	ns
t_{DVEH}	Data Input Valid to Chip Enable High	$\overline{W} = V_{IL}$	Min	50	ns
t_{WLEL}	Write Enable Low to Chip Enable Low		Min	0	ns
t_{VPHEH}	Program/Erase Enable High to Chip Enable High		Min	0	ns
t_{EHAX}	Chip Enable High to Address Transition	$\overline{W} = V_{IL}$	Min	5	ns
t_{EHBL}	Chip Enable High to Status/(Ready/Busy) low		Max	500	ns
t_{EHDX}	Chip Enable High to Input Transition	$\overline{W} = V_{IL}$	Min	5	ns
t_{EHWH}	Chip Enable High to Write Enable High		Min	0	ns
t_{GHEL}	Output Enable High to Chip Enable Low		Min	20	ns
t_{EHGL}	Chip Enable High to Output Enable Low		Min	35	ns
t_{EHEL}	Chip Enable High to Chip Enable Low		Min	30	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	$\overline{W} = V_{IL}$	Min	70	ns

Figure 15. Reset, Power-Down and Power-Up AC Waveform



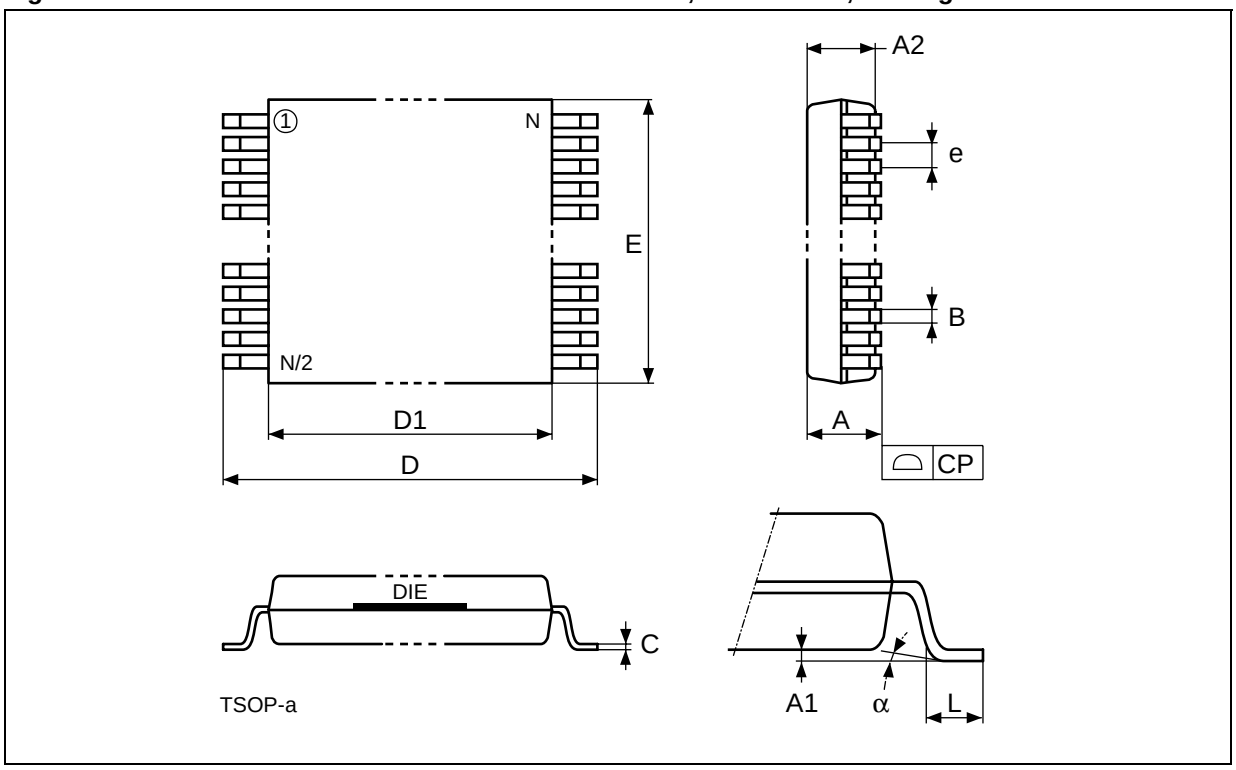
Note: 1. Refer to Table 3 for details of how the device is enabled.
2. Not available with the LFBGA88 package.

Table 20. Reset, Power-Down and Power-Up AC Characteristics

Symbol	Parameter		M30LW128D	Unit
			110	
t_{PHQV}	Reset/Power-Down High to Data Valid	Max	150	ns
t_{PHWL}	Reset/Power-Down High to Write Enable Low	Max	1	µs
t_{PLPH}	Reset/Power-Down Low to Reset/Power-Down High	Min	100	ns
t_{PLBH}	Reset/Power-Down Low to Status/(Ready/Busy) High	Max	30	µs
t_{VDHPH}	Supply Voltages High to Reset/Power-Down High	Min	0	µs

PACKAGE MECHANICAL

Figure 16. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Outline

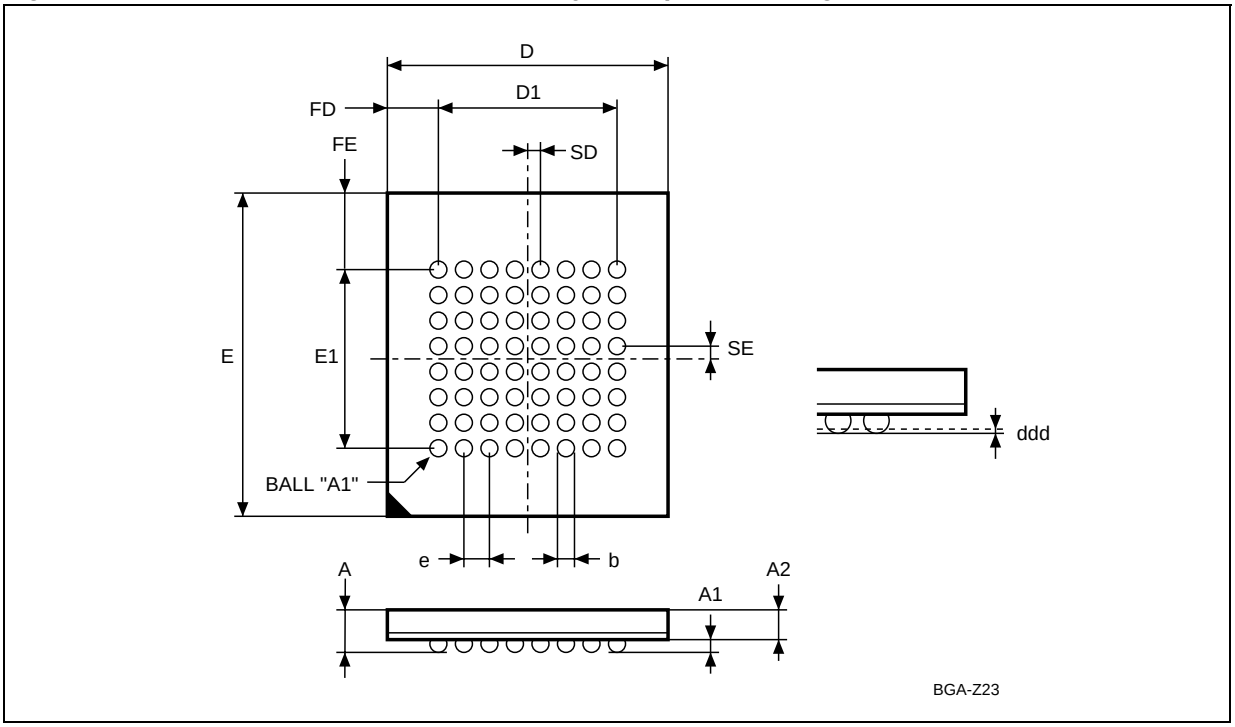


Note: Drawing is not to scale.

Table 21. TSOP56 - 56 lead Plastic Thin Small Outline, 14 x 20 mm, Package Mechanical Data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.0472
A1		0.05	0.15		0.0020	0.0059
A2		0.95	1.05		0.0374	0.0413
B		0.17	0.27		0.0067	0.0106
C		0.10	0.21		0.0039	0.0083
D		19.80	20.20		0.7795	0.7953
D1		18.30	18.50		0.7205	0.7283
E		13.90	14.10		0.5472	0.5551
e	0.50	–	–	0.0197	–	–
L		0.50	0.70		0.0197	0.0276
α		0°	5°		0°	5°
N	56			56		
CP			0.10			0.0039

Figure 17. TBGA64 - 10x13mm, 8 x 8 ball array 1mm pitch, Package Outline

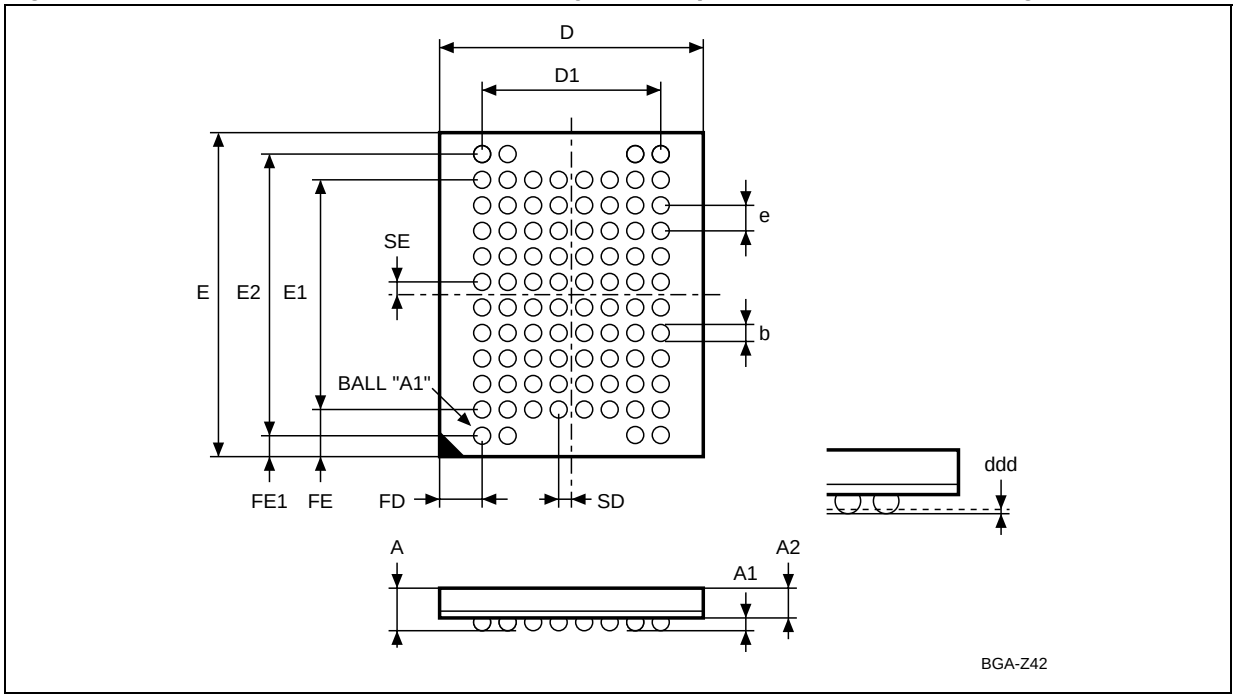


Note: Drawing is not to scale.

Table 22. TBGA64 - 10x13mm, 8 x 8 ball array, 1 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2			0.850			0.0335
b		0.400	0.500		0.0157	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000	–	–	0.2756	–	–
ddd			0.100			0.0039
e	1.000	–	–	0.0394	–	–
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	7.000	–	–	0.2756	–	–
FD	1.500	–	–	0.0591	–	–
FE	3.000	–	–	0.1181	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

Figure 18. LFBGA88 8x10 mm - 8x10 ball array, 0.8mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 23. LFBGA88 8x10mm - 8x10 ball array, 0.8mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.400			0.0551
A1		0.300			0.0118	
A2	0.960			0.0378		
b	0.400	0.350	0.450	0.0157	0.0138	0.0177
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600	–	–	0.2205	–	–
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200	–	–	0.2835	–	–
E2	8.800	–	–	0.3465	–	–
e	0.800	–	–	0.0315	–	–
FD	1.200	–	–	0.0472	–	–
FE	1.400	–	–	0.0551	–	–
FE1	0.600	–	–	0.0236	–	–
SD	0.400	–	–	0.0157	–	–
SE	0.400	–	–	0.0157	–	–

Note: All of the values in the table are preliminary and are subject to change.

PART NUMBERING

Table 24. Ordering Information Scheme

Example: M30LW128D 110 N 1 T

Device Type
M30 = Multiple Memory Product, Multiple Flash

Architecture
L = Page Mode

Operating Voltage
W = V_{DD} = 2.7V to 3.6V, V_{DDQ} = 1.8V to V_{DD}

Device Function
128D = Two 64 Mbit (x8, x16), Uniform Block

Speed
110 = 110 ns

Package
N = TSOP56: 14 x 20 mm
ZA = TBGA64: 10 x 13 mm, 1mm pitch
ZE = LFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESS TABLE

Table 25. Block Addresses

Block No.		Address Range (x8 Bus Width)	Address Range (x16 Bus Width)
Upper Memory	128	FE0000h-FFFFFFh	7F0000h-7FFFFFh
	127	FC0000h-FDFFFFh	7E0000h-7EFFFFh
	126	FA0000h-FBFFFFh	7D0000h-7DFFFFh
	125	F80000h-F9FFFFh	7C0000h-7CFFFFh
	124	F60000h-F7FFFFh	7B0000h-7BFFFFh
	123	F40000h-F5FFFFh	7A0000h-7AFFFFh
	122	F20000h-F3FFFFh	790000h-79FFFFh
	121	F00000h-F1FFFFh	780000h-78FFFFh
	120	EE0000h-EFFFFFh	770000h-77FFFFh
	119	EC0000h-EDFFFFh	760000h-76FFFFh
	118	EA0000h-EBFFFFh	750000h-75FFFFh
	117	E80000h-E9FFFFh	740000h-74FFFFh
	116	E60000h-E7FFFFh	730000h-73FFFFh
	115	E40000h-E5FFFFh	720000h-72FFFFh
	114	E20000h-E3FFFFh	710000h-71FFFFh
	113	E00000h-E1FFFFh	700000h-70FFFFh
	112	DE0000h-DFFFFFh	6F0000h-6FFFFFh
	111	DC0000h-DDFFFFh	6E0000h-6EFFFFh
	110	DA0000h-DBFFFFh	6D0000h-6DFFFFh
	109	D80000h-D9FFFFh	6C0000h-6CFFFFh
	108	D60000h-D7FFFFh	6B0000h-6BFFFFh
	107	D40000h-D5FFFFh	6A0000h-6AFFFFh
	106	D20000h-D3FFFFh	690000h-69FFFFh
	105	D00000h-D1FFFFh	680000h-68FFFFh
	104	CE0000h-CFFFFFh	670000h-67FFFFh
	103	CC0000h-CDFFFFh	660000h-66FFFFh
	102	CA0000h-CBFFFFh	650000h-65FFFFh
	101	C80000h-C9FFFFh	640000h-64FFFFh
	100	C60000h-C7FFFFh	630000h-63FFFFh
	99	C40000h-C5FFFFh	620000h-62FFFFh
	98	C20000h-C3FFFFh	610000h-61FFFFh
	97	C00000h-C1FFFFh	600000h-60FFFFh
	96	BE0000h-BFFFFFh	5F0000h-5FFFFFh
	95	BC0000h-BDFFFFh	5E0000h-5EFFFFh
	94	BA0000h-BBFFFFh	5D0000h-5DFFFFh
	93	B80000h-B9FFFFh	5C0000h-5CFFFFh
	92	B60000h-B7FFFFh	5B0000h-5BFFFFh
	91	B40000h-B5FFFFh	5A0000h-5AFFFFh
	90	B20000h-B3FFFFh	590000h-59FFFFh
	89	B00000h-B1FFFFh	580000h-58FFFFh
	88	AE0000h-AFFFFFh	570000h-57FFFFh
	87	AC0000h-ADFFFFh	560000h-56FFFFh
	86	AA0000h-ABFFFFh	550000h-55FFFFh
	85	A80000h-A9FFFFh	540000h-54FFFFh
	84	A60000h-A7FFFFh	530000h-53FFFFh
	83	A40000h-A5FFFFh	520000h-52FFFFh
	82	A20000h-A3FFFFh	510000h-51FFFFh
	81	A00000h-A1FFFFh	500000h-50FFFFh
	80	9E0000h-9FFFFFh	4F0000h-4FFFFFh
	79	9C0000h-9DFFFFh	4E0000h-4EFFFFh
	78	9A0000h-9BFFFFh	4D0000h-4DFFFFh
	77	980000h-99FFFFh	4C0000h-4CFFFFh
	76	960000h-97FFFFh	4B0000h-4BFFFFh
	75	940000h-95FFFFh	4A0000h-4AFFFFh
	74	920000h-93FFFFh	490000h-49FFFFh
	73	900000h-91FFFFh	480000h-48FFFFh
	72	8E0000h-8FFFFFh	470000h-47FFFFh
	71	8C0000h-8DFFFFh	460000h-46FFFFh
	70	8A0000h-8BFFFFh	450000h-45FFFFh
	69	880000h-89FFFFh	440000h-44FFFFh
	68	860000h-87FFFFh	430000h-43FFFFh
	67	840000h-85FFFFh	420000h-42FFFFh
	66	820000h-83FFFFh	410000h-41FFFFh
	65	800000h-81FFFFh	400000h-40FFFFh

	Block No.	Address Range (x8 Bus Width)	Address Range (x16 Bus Width)
Lower Memory	64	7E0000h-7FFFFFh	3F0000h-3FFFFFh
	63	7C0000h-7DFFFFh	3E0000h-3EFFFFh
	62	7A0000h-7BFFFFh	3D0000h-3DFFFFh
	61	780000h-79FFFFh	3C0000h-3CFFFFh
	60	760000h-77FFFFh	3B0000h-3BFFFFh
	59	740000h-75FFFFh	3A0000h-3AFFFFh
	58	720000h-73FFFFh	390000h-39FFFFh
	57	700000h-71FFFFh	380000h-38FFFFh
	56	6E0000h-6FFFFFh	370000h-37FFFFh
	55	6C0000h-6DFFFFh	360000h-36FFFFh
	54	6A0000h-6BFFFFh	350000h-35FFFFh
	53	680000h-69FFFFh	340000h-34FFFFh
	52	660000h-67FFFFh	330000h-33FFFFh
	51	640000h-65FFFFh	320000h-32FFFFh
	50	620000h-63FFFFh	310000h-31FFFFh
	49	600000h-61FFFFh	300000h-30FFFFh
	48	5E0000h-5FFFFFh	2F0000h-2FFFFFh
	47	5C0000h-5DFFFFh	2E0000h-2EFFFFh
	46	5A0000h-5BFFFFh	2D0000h-2DFFFFh
	45	580000h-59FFFFh	2C0000h-2CFFFFh
	44	560000h-57FFFFh	2B0000h-2BFFFFh
	43	540000h-55FFFFh	2A0000h-2AFFFFh
	42	520000h-53FFFFh	290000h-29FFFFh
	41	500000h-51FFFFh	280000h-28FFFFh
	40	4E0000h-4FFFFFh	270000h-27FFFFh
	39	4C0000h-4DFFFFh	260000h-26FFFFh
	38	4A0000h-4BFFFFh	250000h-25FFFFh
	37	480000h-49FFFFh	240000h-24FFFFh
	36	460000h-47FFFFh	230000h-23FFFFh
	35	440000h-45FFFFh	220000h-22FFFFh
	34	420000h-43FFFFh	210000h-21FFFFh
	33	400000h-41FFFFh	200000h-20FFFFh
	32	3E0000h-3FFFFFh	1F0000h-1FFFFFh
	31	3C0000h-3DFFFFh	1E0000h-1EFFFFh
	30	3A0000h-3BFFFFh	1D0000h-1DFFFFh

	Block No.	Address Range (x8 Bus Width)	Address Range (x16 Bus Width)
Lower Memory	29	380000h-39FFFFh	1C0000h-1CFFFFh
	28	360000h-37FFFFh	1B0000h-1BFFFFh
	27	340000h-35FFFFh	1A0000h-1AFFFFh
	26	320000h-33FFFFh	190000h-19FFFFh
	25	300000h-31FFFFh	180000h-18FFFFh
	24	2E0000h-2FFFFFh	170000h-17FFFFh
	23	2C0000h-2DFFFFh	160000h-16FFFFh
	22	2A0000h-2BFFFFh	150000h-15FFFFh
	21	280000h-29FFFFh	140000h-14FFFFh
	20	260000h-27FFFFh	130000h-13FFFFh
	19	240000h-25FFFFh	120000h-12FFFFh
	18	220000h-23FFFFh	110000h-11FFFFh
	17	200000h-21FFFFh	100000h-10FFFFh
	16	1E0000h-1FFFFFh	0F0000h-0FFFFFh
	15	1C0000h-1DFFFFh	0E0000h-0EFFFFh
	14	1A0000h-1BFFFFh	0D0000h-0DFFFFh
	13	180000h-19FFFFh	0C0000h-0CFFFFh
	12	160000h-17FFFFh	0B0000h-0BFFFFh
	11	140000h-15FFFFh	0A0000h-0AFFFFh
	10	120000h-13FFFFh	090000h-09FFFFh
	9	100000h-11FFFFh	080000h-08FFFFh
	8	0E0000h-0FFFFFh	070000h-07FFFFh
	7	0C0000h-0DFFFFh	060000h-06FFFFh
	6	0A0000h-0BFFFFh	050000h-05FFFFh
	5	080000h-09FFFFh	040000h-04FFFFh
	4	060000h-07FFFFh	030000h-03FFFFh
	3	040000h-05FFFFh	020000h-02FFFFh
	2	020000h-03FFFFh	010000h-01FFFFh
	1	000000h-01FFFFh	000000h-00FFFFh

APPENDIX B. COMMON FLASH INTERFACE - CFI

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 26, 27, 28, 29, 30 and 31 show the addresses used to retrieve the data.

Table 26. Query Structure Overview

Address		Sub-section Name	Description
x16	x8(4)		
0000h	10h		Manufacturer Code
0001h	11h		Device Code
0010h	20h	CFI Query Identification String	Command set ID and algorithm data offset
001Bh	36h	System Interface Information	Device timing and voltage information
0027h	4Eh	Device Geometry Definition	Flash memory layout
P(h)(1)		Primary Algorithm-specific Extended Query Table	Additional information specific to the Primary Algorithm (optional)
A(h)(2)		Alternate Algorithm-specific Extended Query Table	Additional information specific to the Alternate Algorithm (optional)
(SBA+02)h		Block Status Register	Block-related Information

Note: 1. Offset 15h defines P which points to the Primary Algorithm Extended Query Address Table.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.
3. SBA is the Start Base Address for each block.
4. In x8 mode A0 must be set to V_{IL}. Otherwise, 00h will be output.

Table 27. CFI - Query Address and Data Output

Address		Data		Description
x16	x8(3)			
0010h	20h	51h	"Q"	Query ASCII String 51h; "Q" 52h; "R" 59h; "Y"
0011h	22h	52h	"R"	
0012h	24h	59h	"Y"	
0013h	26h	01h		Primary Vendor: Command Set and Control Interface ID Code
0014h	28h	00h		
0015h	2Ah	31h		Primary algorithm extended Query Address Table: P(h)
0016h	2Ch	00h		
0017h	2Eh	00h		Alternate Vendor: Command Set and Control Interface ID Code
0018h	30h	00h		
0019h	32h	00h		Alternate Algorithm Extended Query address Table
001Ah(2)	34h	00h		

Note: 1. Query Data are always presented on DQ7-DQ0. DQ15-DQ8 are set to '0'.
2. Offset 19h defines A which points to the Alternate Algorithm Extended Query Address Table.
3. In x8 mode A0 must be set to V_{IL}. Otherwise, 00h will be output.

Table 28. CFI - Device Voltage and Timing Specification

Address		Data	Description
x16	x8(4)		
001Bh	36h	27h (1)	V_{DD} Min, 2.7V
001Ch	38h	36h (1)	V_{DD} max, 3.6V
001Dh	3Ah	00h (2)	V_{PP} min – Not Available
001Eh	3Ch	00h (2)	V_{PP} max – Not Available
001Fh	3Eh	04h	2^n µs typical time-out for Word, DWord prog – Not Available
0020h	40h	08h	2^n µs, typical time-out for max buffer write
0021h	42h	0Ah	2^n ms, typical time-out for Erase Block
0022h	44h	00h (3)	2^n ms, typical time-out for chip erase – Not Available
0023h	46h	04h	2^n x typical for Word Dword time-out max – Not Available
0024h	48h	04h	2^n x typical for buffer write time-out max
0025h	4Ah	04h	2^n x typical for individual block erase time-out maximum
0026h	4Ch	00h (3)	2^n x typical for chip erase max time-out – Not Available

Note: 1. Bits are coded in Binary Code Decimal, bit7 to bit4 are scaled in Volts and bit3 to bit0 in mV.
2. Bit7 to bit4 are coded in Hexadecimal and scaled in Volts while bit3 to bit0 are in Binary Code Decimal and scaled in 100mV.
3. Not supported.
4. In x8 mode A0 must be set to V_{IL}. Otherwise, 00h will be output.

Table 29. Device Geometry Definition

Address		Data	Description	
x16	x8(1)			
0027h	4Eh	18h	n where 2^n is number of bytes memory Size	
0028h	50h	02h	Device Interface	02h is the interface for M30LW128D devices delivered in TSOP56 and TBGA64 packages (x8 and x16 modes available)
	N/A(2)	01h		01h is the interface for M30LW128D devices delivered in LFBGA88 packages (x16 mode available)
0029h	52h	00h		
002Ah	54h	05h	Maximum number of bytes in Write Buffer, 2^n	
002Bh	56h	00h		
002Ch	58h	01h	Bit7-0 = number of Erase Block Regions in device	
002Dh	5Ah	7Fh	Number (n-1) of Erase Blocks of identical size; n=128	
002Eh	5Ch	00h		
002Fh	5Eh	00h	Erase Block Region Information x 256 bytes per Erase block (128K bytes)	
0030h	60h	02h		

Note: 1. In x8 mode A0 must be set to V_{IL}. Otherwise, 00h will be output.
2. N/A = Not Applicable. Only the x16 mode is available with the LFBGA88 package.

Table 30. Block Status Register

Address	Data		Selected Block Information
(BA+2)h(1)	bit0	0	Block Unprotected
		1	Block Protected
	bit1	0	Last erase operation ended successfully (2)
		1	Last erase operation not ended successfully (2)
	bit7-2	0	Reserved for future features

Note: 1. BA specifies the block address location, A22-A17.
2. Not Supported.

Table 31. Extended Query information

Address			Data (Hex)		Description
offset	x16	x8(2)			
(P)h	0031h	62h	50h	"P"	Query ASCII string - Extended Table
(P+1)h	0032h	64h	52h	"R"	
(P+2)h	0033h	66h	49h	"I"	
(P+3)h	0034h	68h	31h		Major version number
(P+4)h	0035h	6Ah	31h		Minor version number
(P+5)h	0036h	6Ch	CEh		Optional Feature: (1=yes, 0=no) bit0, Chip Erase Supported (0=no) bit1, Suspend Erase Supported (1=yes) bit2, Suspend Program Supported (1=yes) bit3, Protect/Unprotect Supported (1=yes) bit4, Queue Erase Supported (0=no) bit5, Instant Individual Block locking (0=no) bit6, Protection bits supported (1=yes) bit7, Page Read supported (1=yes) bit8, Synchronous Read supported (0=no) bit9, Multi chip device (1=yes) bit10, Simultaneous operations supported (1=yes) Bits 11 to 31 reserved for future use
(P+6)h	0037h	6Eh	06h		
(P+7)h	0038h	70h	00h		
(P+8)h	0039h	72h	00h		
(P+9)h	003Ah	74h	01h		Function allowed after Suspend: Program allowed after Erase Suspend (1=yes) Bits 1 to 7 reserved for future use
(P+A)h	003Bh	76h	01h		Block Status Register bit0, Block Protect-Bit status active (1=yes) bit1, Block Lock-Down Bit status (not available) bits 2 to 15 reserved for future use
(P+B)h	003Ch	78h	00h		
(P+C)h	003Dh	7Ah	33h		V_{DD} OPTIMUM Program/Erase voltage conditions
(P+D)h	003Eh	7Ch	00h		V_{PP} OPTIMUM Program/Erase voltage conditions
(P+E)h	003Fh	7Eh	01h		OTP protection: No. of protection register fields
(P+F)h	0040h	80h	80h		Protection Register's start address, least significant bits
(P+10)h	0041h	82h	00h		Protection Register's start address, most significant bits
(P+11)h	0042h	84h	03h		n where 2^n is number of factory reprogrammed bytes
(P+12)h	0043h	86h	03h		n where 2^n is number of user programmable bytes
(P+13)h	0044h	88h	03h		Page Read: 2^n Bytes (n = bits 0-7)
(P+14)h	0045h	8Ah	00h		Synchronous mode configuration fields
(P+15)h	0046h	8Ch	Reserved for future use		

Note: 1. Bit7 to bit4 are coded in Hexadecimal and scaled in Volt while bit3 to bit0 are in Binary Code Decimal and scaled in mV.
2. In x8 mode, A0 must be set to V_{IL}, otherwise 00h will be output.

APPENDIX C. FLOW CHARTS

Figure 19. Write to Buffer and Program Flowchart and Pseudo Code

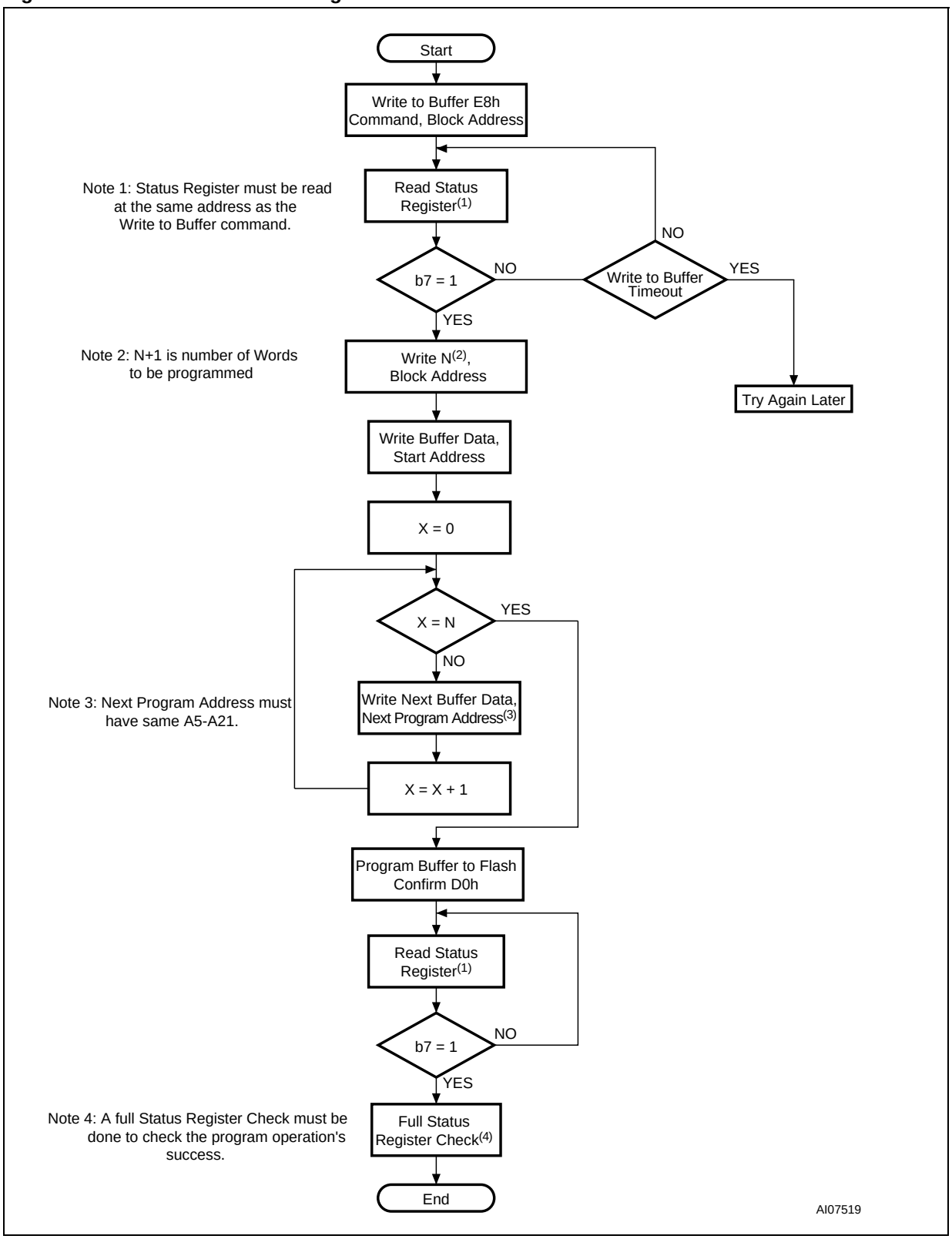
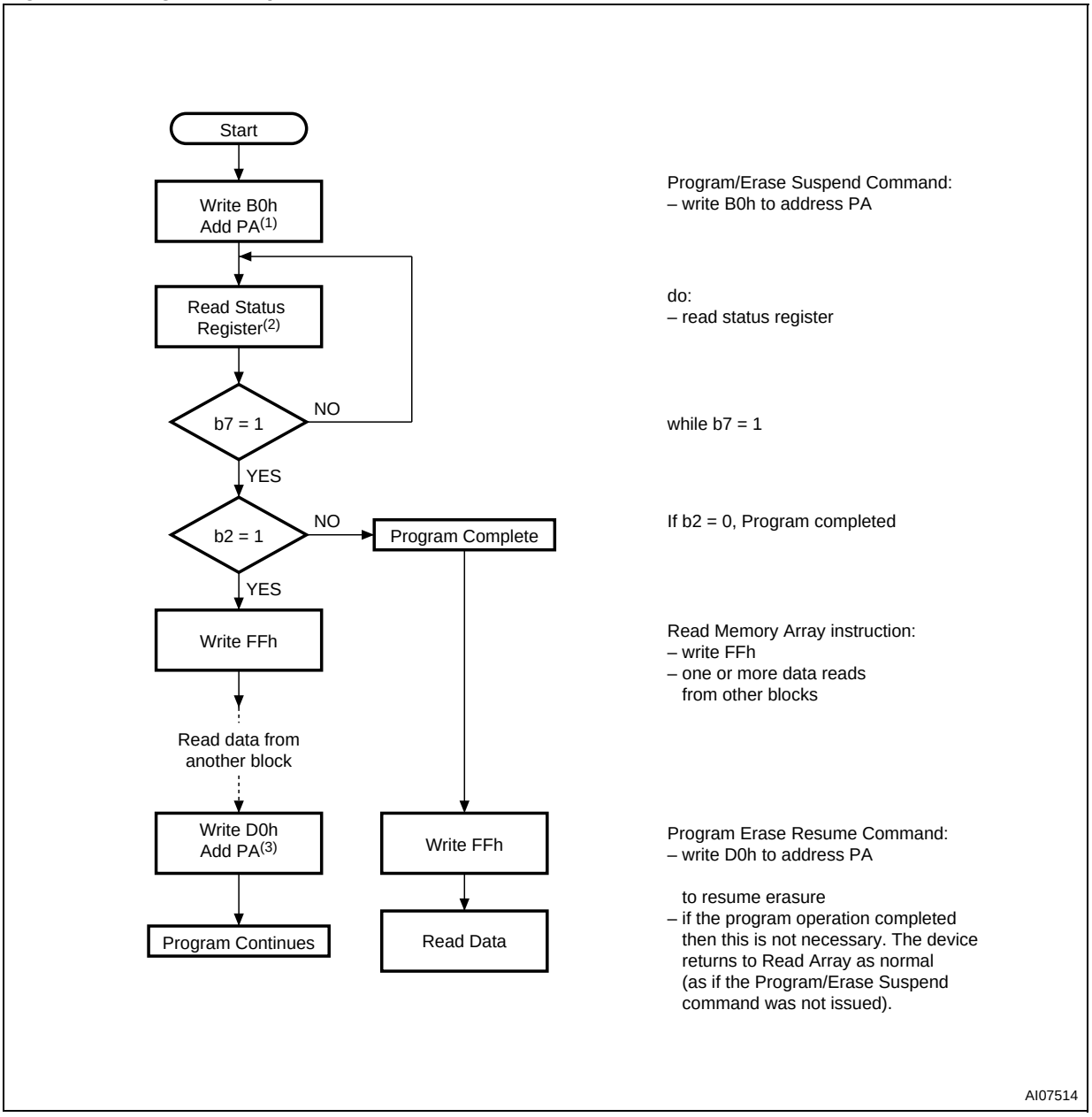
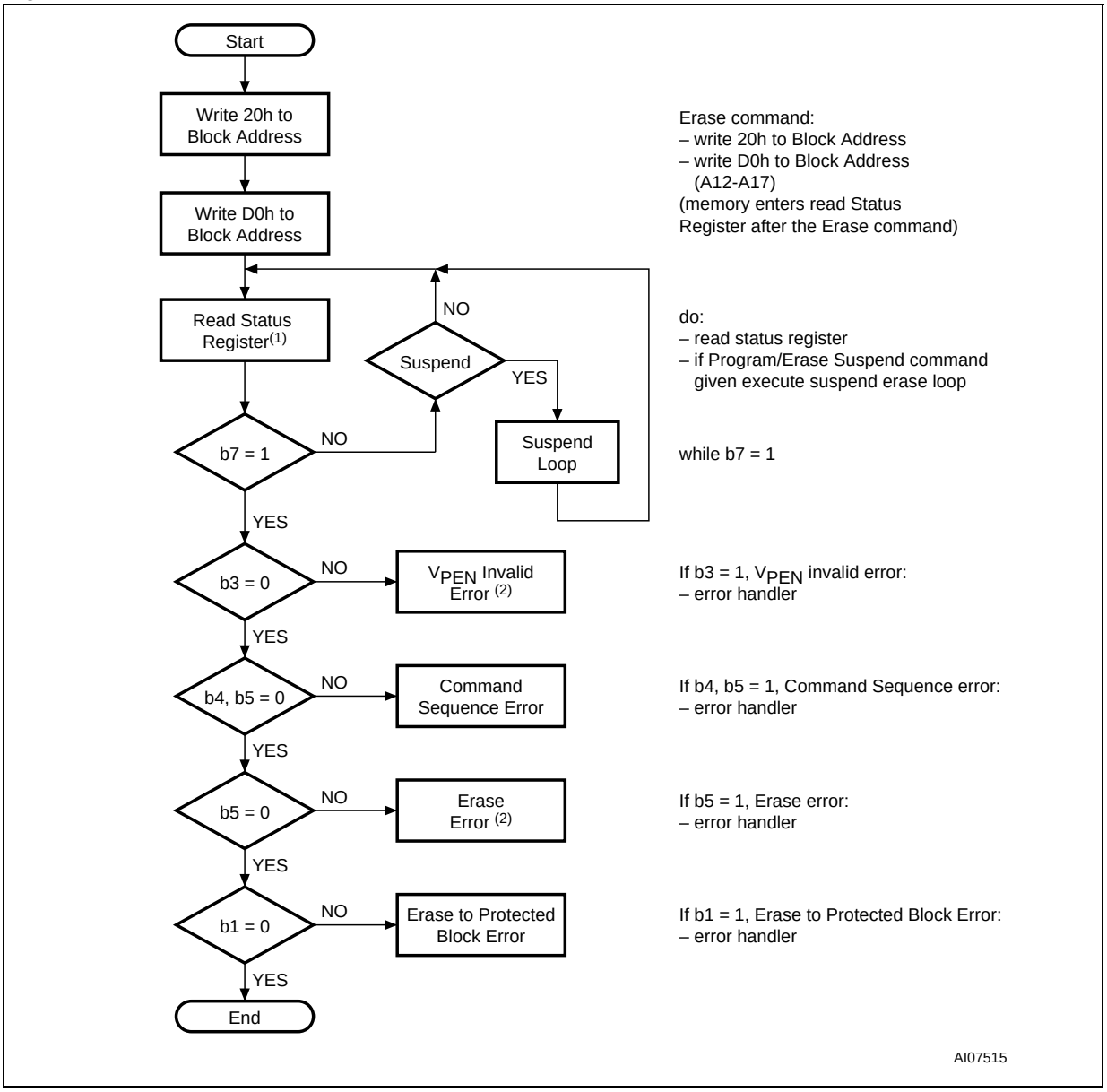


Figure 20. Program Suspend & Resume Flowchart and Pseudo Code



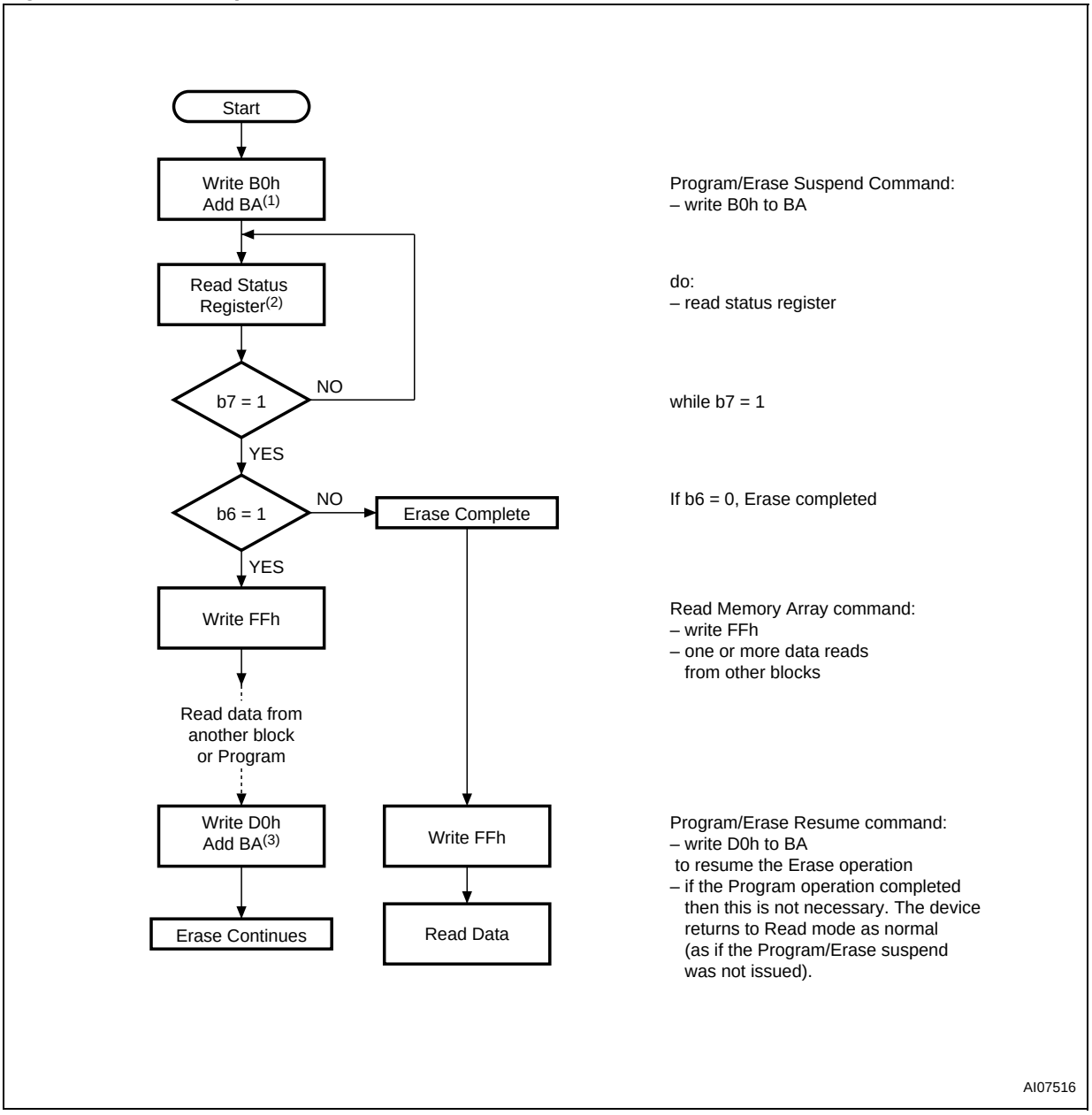
Note: 1. PA = Program Address. The Program/ Erase Suspend command must be issued to the same address as the current Program command.
2. The Read Status Register command must be issued to the same address as the Program/ Erase Suspend command.
3. PA = Program Address. The Program/ Erase Resume command must be issued to the same address as the Program/ Erase Suspend command.

Figure 21. Erase Flowchart and Pseudo Code



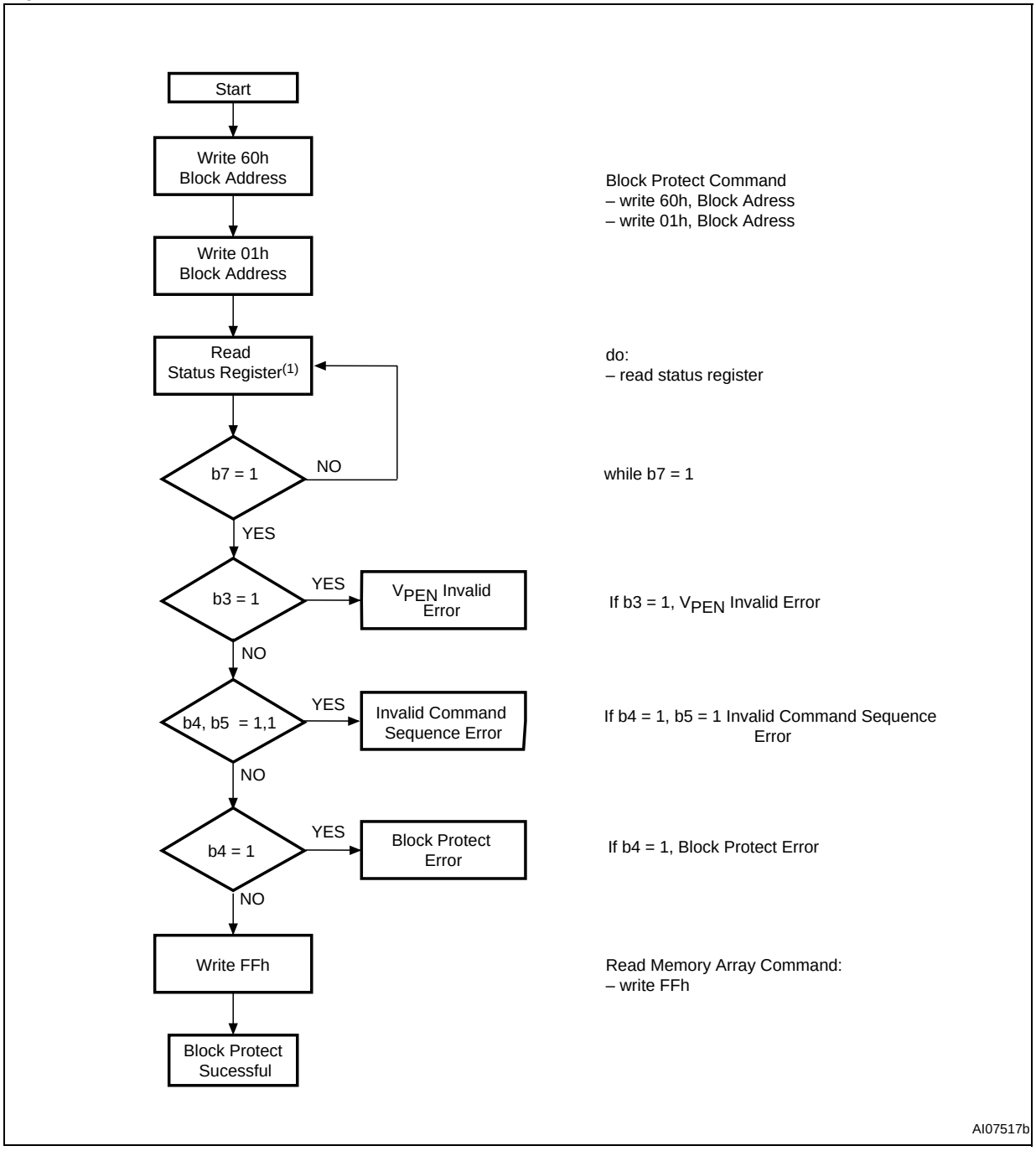
Note: 1. The Read Status Register command must be issued to the same address as the Block Erase command.
2. If an error is found, the Status Register must be cleared (Clear Status Register Command) before further Program or Erase operations.

Figure 22. Erase Suspend & Resume Flowchart and Pseudo Code



Note: 1. The Program/ Erase Suspend command must be issued to the same address as the current Erase command.
2. The Read Status Register command must be issued to the same address as the Program/ Erase Suspend command.
3. The Program/ Erase Resume command must be issued to the same address as the Program/ Erase Suspend command.

Figure 23. Block Protect Flowchart and Pseudo Code



Note: 1. The Read Status Register command must be issued to the same address as the Block Protect command.

Figure 24. Blocks Unprotect Flowchart and Pseudo Code

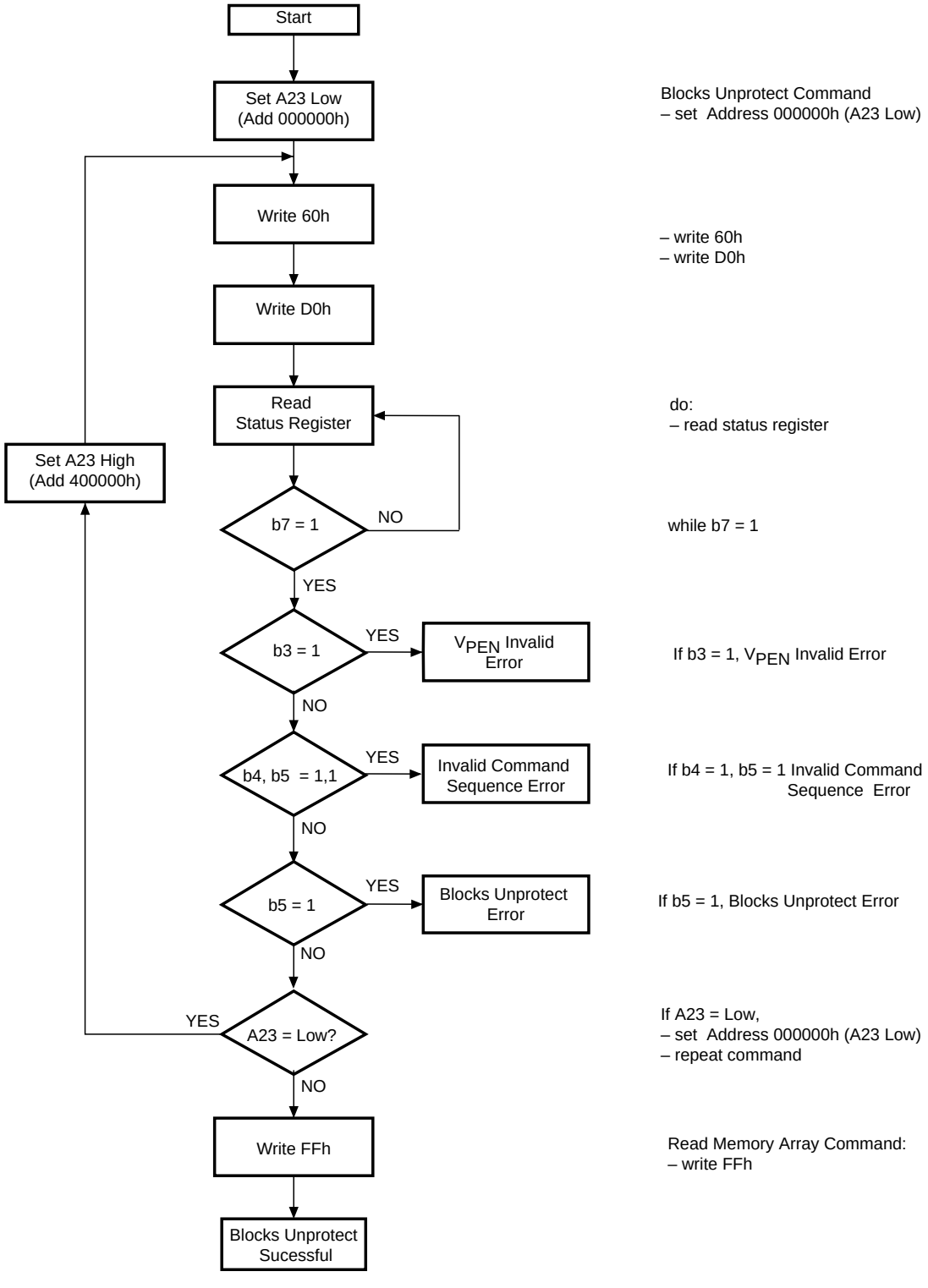
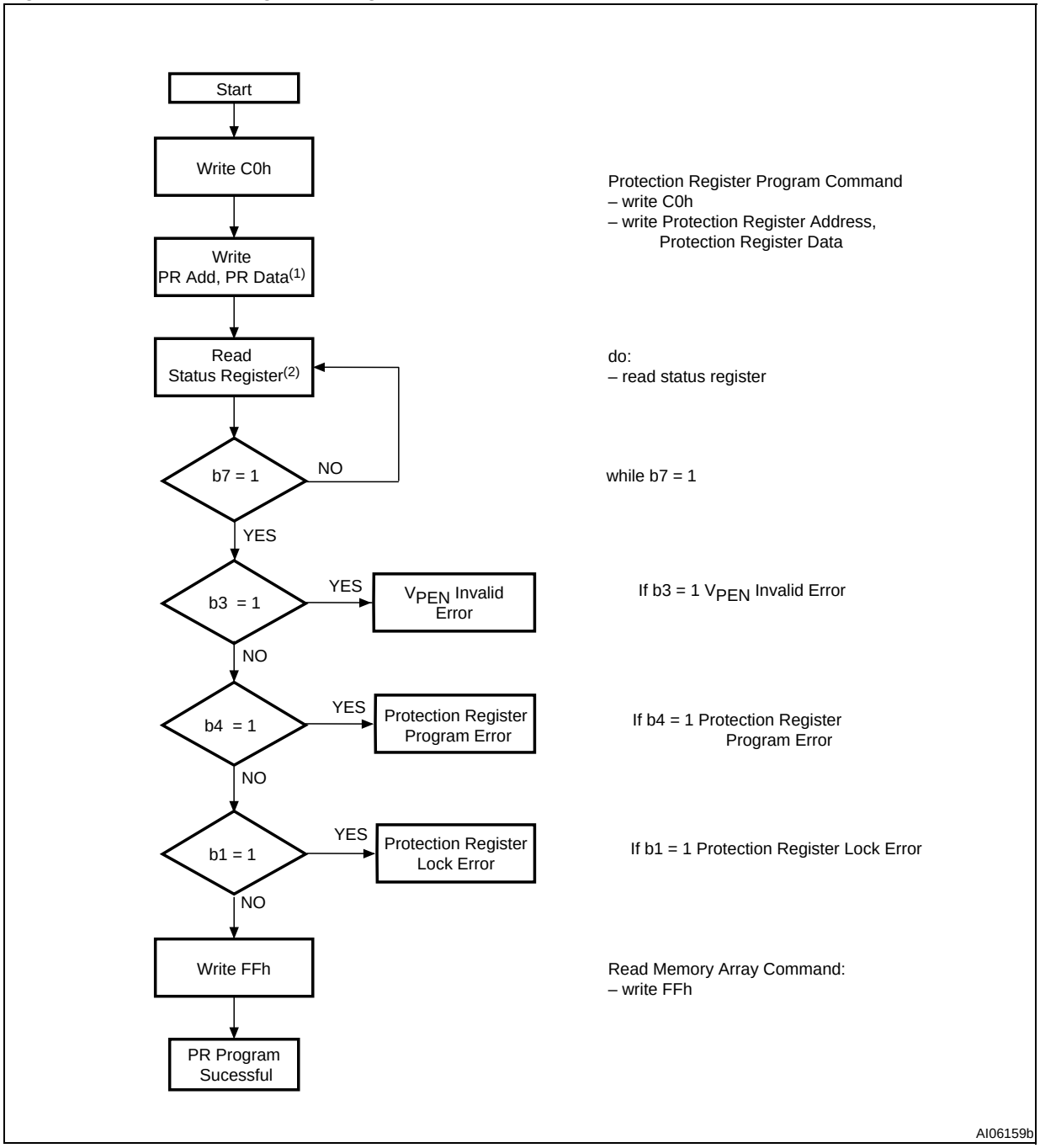
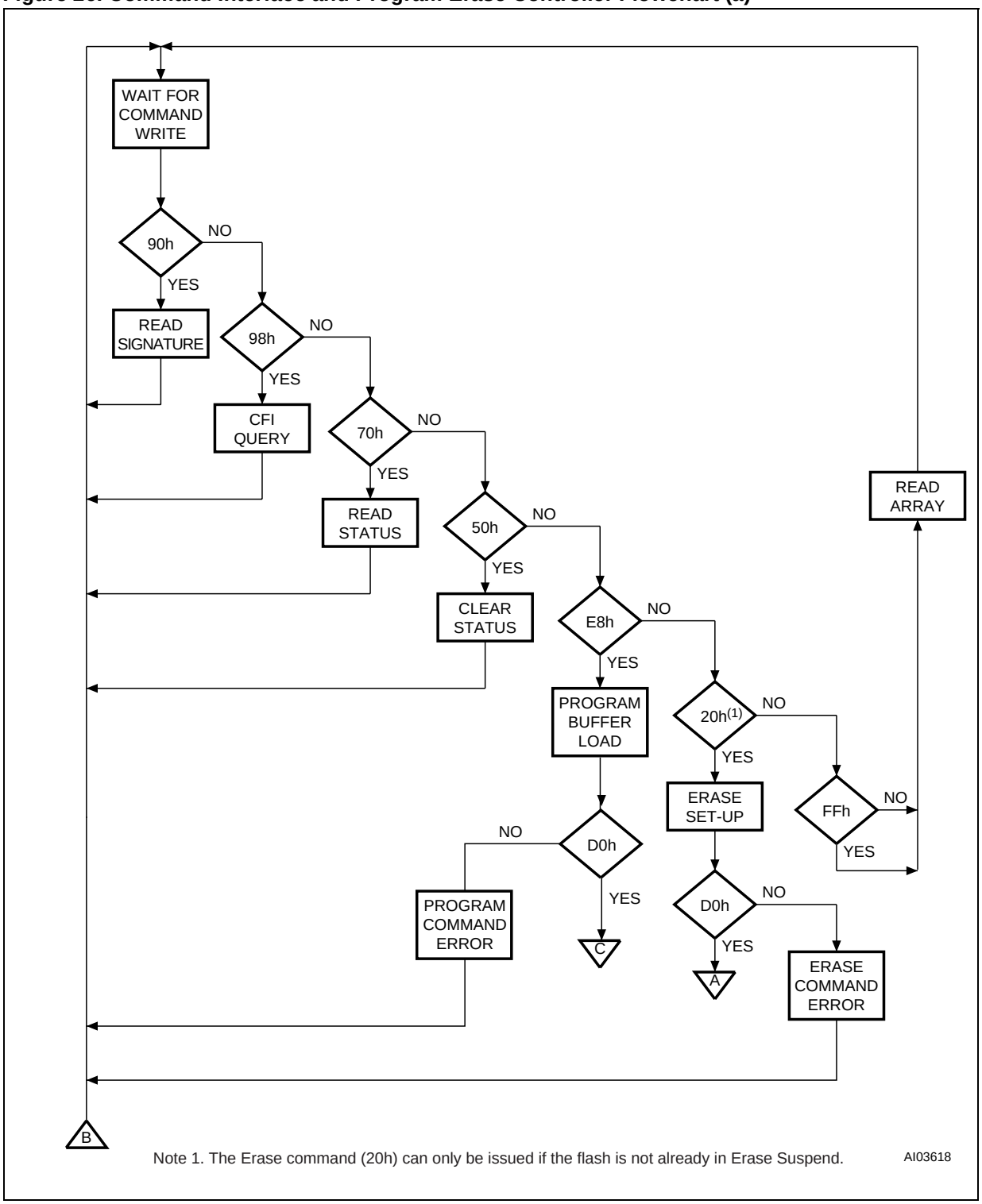


Figure 25. Protection Register Program Flowchart and Pseudo Code



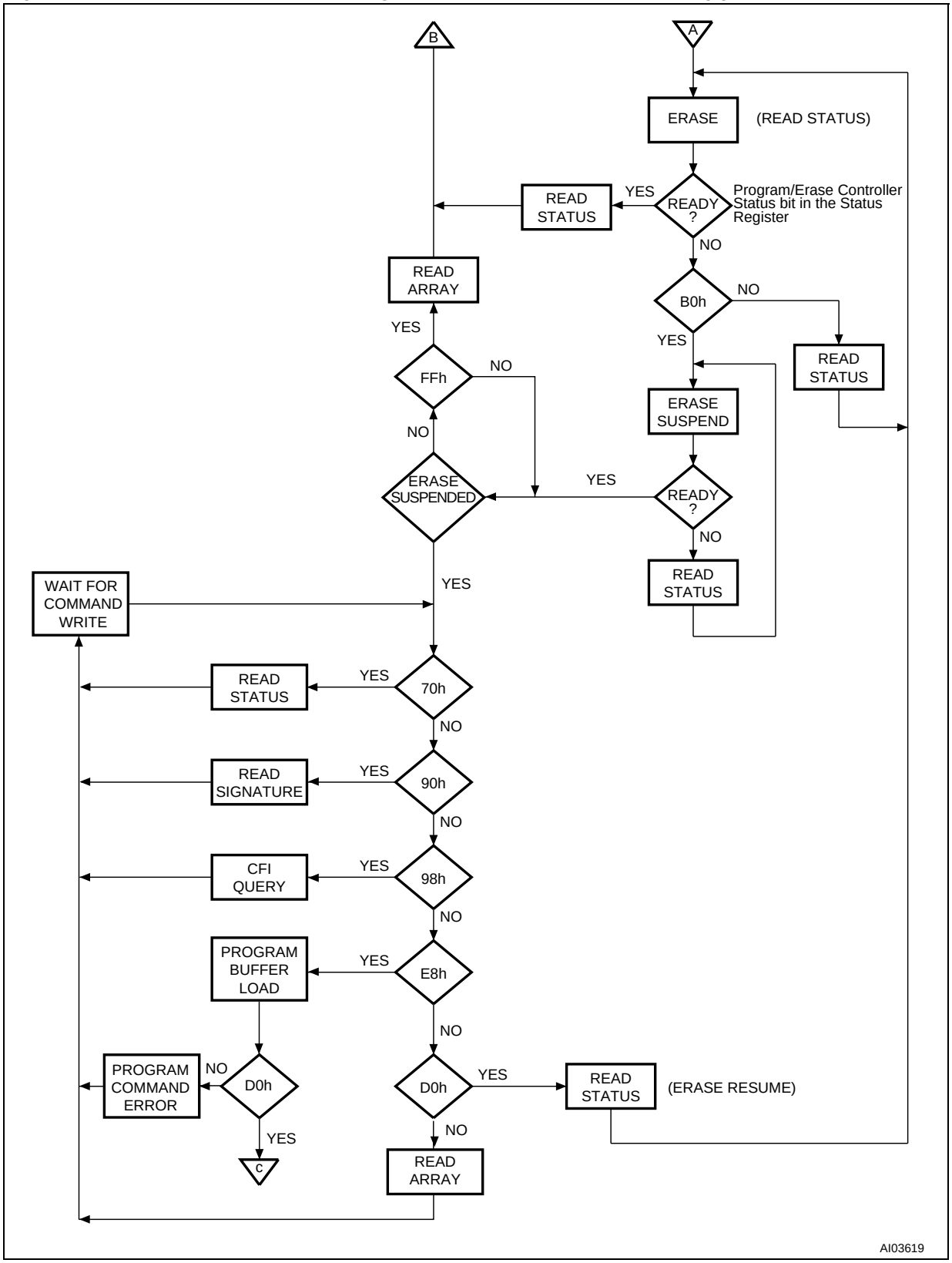
Note: 1. PR = Protection Register
2. The Read Status Register command must be issued to the same address as the Protection Register Program command.

Figure 26. Command Interface and Program Erase Controller Flowchart (a)



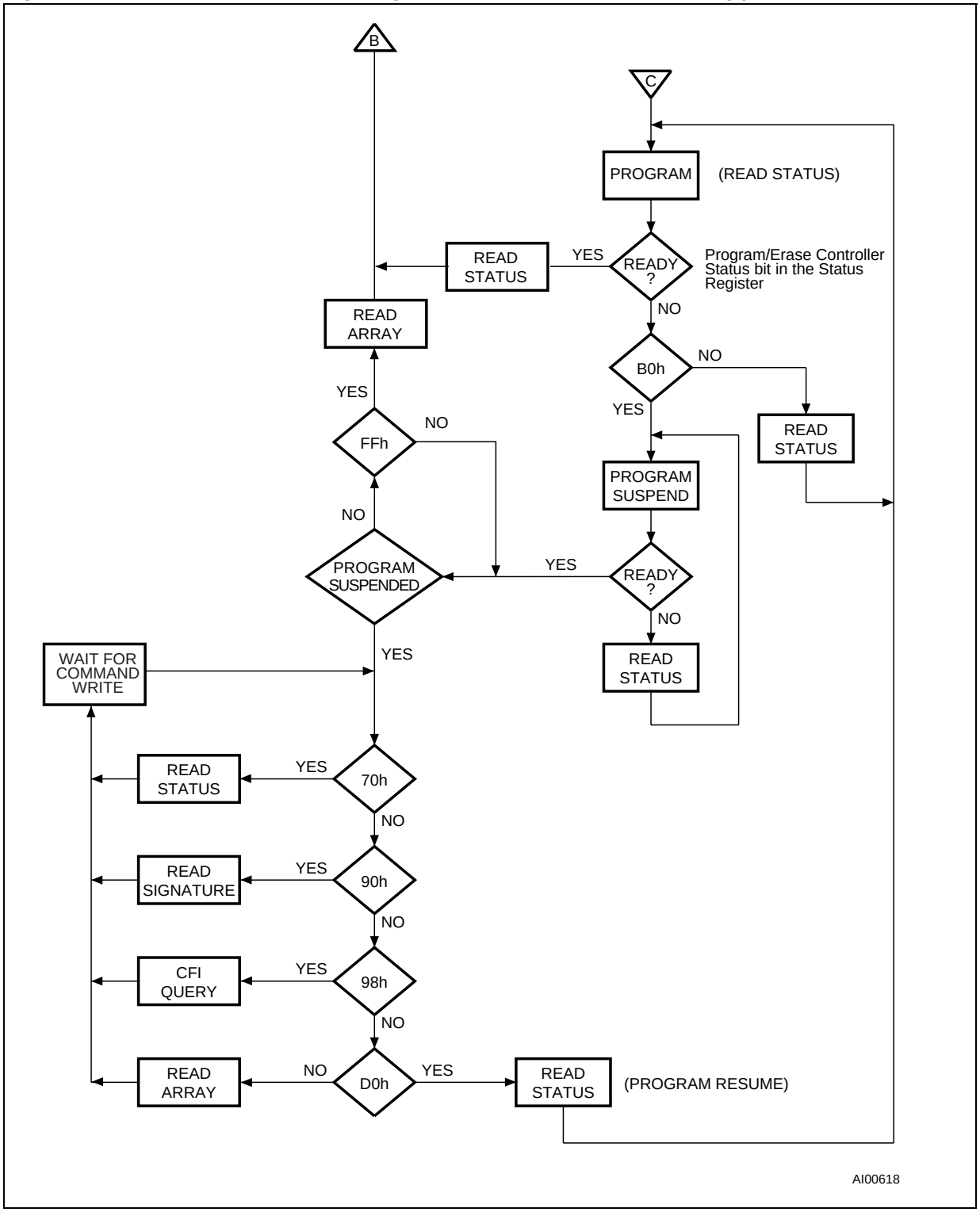
Note: The commands must be issued to the addresses detailed in the Command Interface section, Table 5.

Figure 27. Command Interface and Program Erase Controller Flowchart (b)



Note: The commands must be issued to the addresses detailed in the Command Interface section, Table 5.

Figure 28. Command Interface and Program Erase Controller Flowchart (c).



Note: The commands must be issued to the addresses detailed in the Command Interface section, Table 5.

REVISION HISTORY

Table 32. Document Revision History

Date	Version	Revision Details
10-Oct-2002	1.0	First Issue
11-Feb-2003	2.0	Device code changed, LFBGA88 package added, Program /Erase Times and Program/Erase Endurance cycles table modified, Read Electronic Signature table modified, CFI Tables clarified in particular Table 31 and 29 (Extended Query Information and Device Geometry Definition). I_{OSC} parameter added to Absolute Maximum Ratings table. I_{DD} and V_{LKO} clarified and I_{DDO} and V_{PENH} parameters added to DC Characteristics table. t_{PHWL} parameter added to Reset, Power-Down and Power-Up AC Waveforms figure and Characteristics table. I_{DD1}, I_{DD5}, I_{DD2}, I_{DD4}, V_{IL}, V_{IH} and V_{LKO} values refined in DC Characteristics table. Chip Enable state corrected for Power-Down in Table 4, Bus Operations. Addresses modified for Blocks Unprotect and Configure STS commands in Table 5, Commands. Addresses modified in Figure 24, Blocks Unprotect Flowchart and Pseudo Code. Figure 23, Block Protect Flowchart and Pseudo Code, clarified. Blocks Temporary Unprotect feature of Reset/Power Down pin no longer available. Program/Erase Suspend, Write to Buffer and Program, and Block Erase Commands clarified.