Preliminary W27C4096

Winbond Electronics Corp.

256K × 16 ELECTRICALLY ERASABLE EPROM

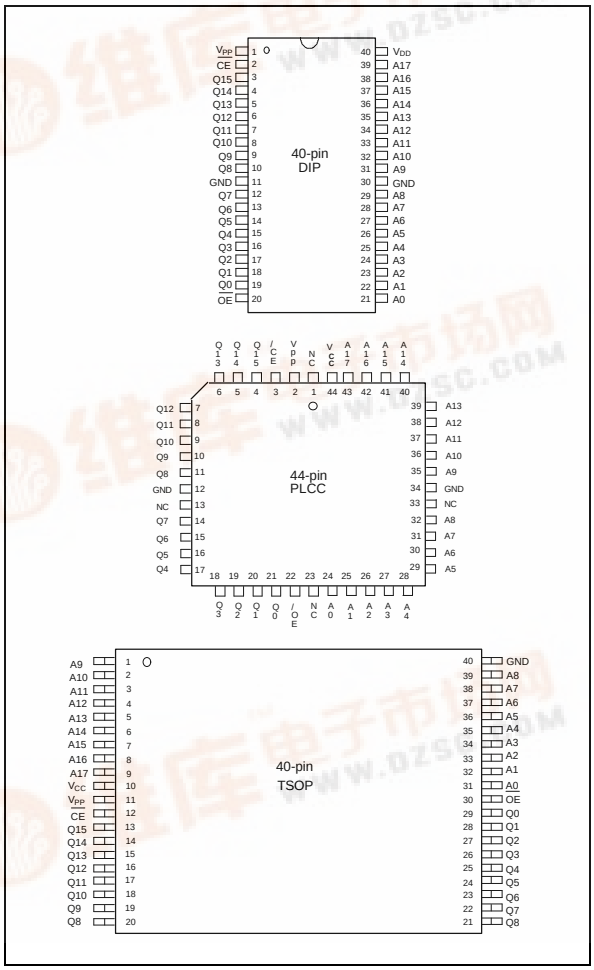
GENERAL DESCRIPTION

The W27C4096 is a high speed, low power Electrically Erasable and Programmable Read Only Memory organized as 262144 × 16 bits that operates on a single 5 volt power supply. The W27C4096 provides an electrical chip erase function.

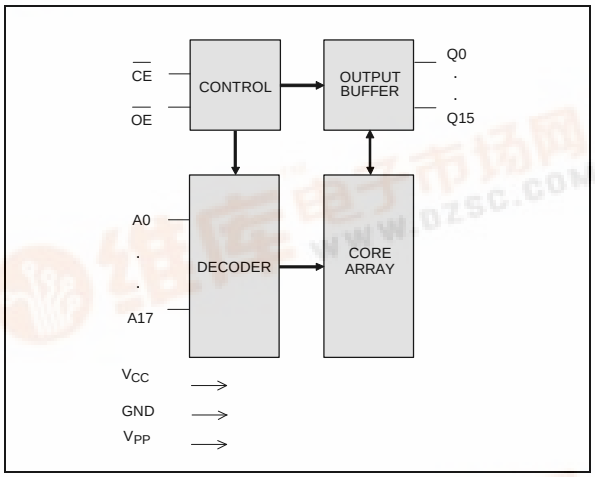
FEATURES

- High speed access time: 120/150 nS (max.)
- Read operating current: 30 mA (max.)
- Erase/Programming operating current 30 mA (max.)
- Standby current: 100 µA (max.)
- Single 5V power supply
- +14V erase/+12V programming voltage
- Fully static operation
- All inputs and outputs directly TTL/CMOS compatible
- Three-state outputs
- Available packages: 40-pin 600 mil DIP, TSOP and 44-pin PLCC

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0–A17	Address Inputs
Q0–Q15	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Program/Erase Supply Voltage
VCC	Power Supply
GND	Ground
NC	No Connection

Publication Release Date: March 1999
Revision A1

FUNCTIONAL DESCRIPTION

Read Mode

Like conventional UVEPROMs, the W27C4096 has two control functions, both of which produce data at the outputs. $\overline{CE}$ is for power control and chip select. $\overline{OE}$ controls the output buffer to gate data to the output pins. When addresses are stable, the address access time (T_{ACC}) is equal to the delay from $\overline{CE}$ to output (T_{CE}), and data are available at the outputs T_{OE} after the falling edge of $\overline{OE}$, if T_{ACC} and T_{CE} timings are met.

Erase Mode

The erase operation is the only way to change data from "0" to "1." Unlike conventional UVEPROMs, which use ultraviolet light to erase the contents of the entire chip (a procedure that requires up to half an hour), the W27C4096 uses electrical erasure. Generally, the chip can be erased within 100 mS by using an EPROM writer with a special erase algorithm.

Erase mode is entered when V_{PP} is raised to V_{PE} (14V), V_{CC} = V_{CE} (5V), $\overline{CE}$ low, $\overline{OE}$ high, A9 = V_{PE} (14V), A0 low, and all other address pins low and data input pins high.

Erase Verify Mode

After an erase operation, all of the words in the chip must be verified to check whether they have been successfully erased to "1" or not. The erase verify mode automatically ensures a substantial erase margin. This mode will be entered after the erase operation if V_{PP} = V_{PE} (14V), $\overline{CE}$ high, and $\overline{OE}$ low.

Program Mode

Programming is performed exactly as it is in conventional UVEPROMs, and programming is the only way to change cell data from "1" to "0." The program mode is entered when V_{PP} is raised to V_{PP} (12V), V_{CC} = V_{CP} (5V), $\overline{CE}$ low, $\overline{OE}$ high, the address pins equal the desired address, and the input pins equal the desired inputs.

Program Verify Mode

All of the words in the chip must be verified to check whether they have been successfully programmed with the desired data or not. Hence, after each word is programmed, a program verify operation should be performed. The program verify mode automatically ensures a substantial program margin. This mode will be entered after the program operation if V_{PP} = V_{PP} (12V), $\overline{CE}$ high, $\overline{OE}$ low and V_{CC} = V_{CP} (5V).

Erase/Program Inhibit

Erase or program inhibit mode allows parallel erasing or programming of multiple chips with different data. When $\overline{CE}$ high , V_{PP} = V_{PP}/V_{PE} (12V/14V), and V_{CC} = 5V, erasing or programming of non-target chips is inhibited, so that except for the $\overline{CE}$ and V_{PP}, and V_{CC}, the W27C4096 may have common inputs.

Standby Mode

The standby mode significantly reduces V_{CC} current. This mode is entered when $\overline{CE}$ high , V_{PP} = 5V, and V_{CC} = 5V. In standby mode, all outputs are in a high impedance state, independent of $\overline{OE}$.

Two-line Output Control

Since EPROMs are often used in large memory arrays, the W27C4096 provides two control inputs for multiple memory connections. Two-line control provides for lowest possible memory power dissipation and ensures that data bus contention will not occur.

System Considerations

EPROM power switching characteristics require careful device decoupling. System designers are interested in three supply current issues: standby current levels (I_{SB}), active current levels (I_{CC}), and transient current peaks produced by the falling and rising edges of $\overline{CE}$. Transient current magnitudes depend on the device output's capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between its V_{CC} and GND. This high frequency, low inherent-inductance capacitor should be placed as close as possible to the device. Additionally, for every eight devices, a 4.7 µF electrolytic capacitor should be placed at the array's power supply connection between V_{CC} and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

TABLE OF OPERATING MODES

(V_{PP} = 12V, V_{PE} = 14V, V_{HH} = 12V, V_{CP} = 5V, X = V_{IH} or V_{IL})

MODE	PINS						
	$\overline{CE}$	$\overline{OE}$	A0	A9	V_{CC}	V_{PP}	OUTPUTS
Read	V_{IL}	V_{IL}	X	X	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	X	X	V_{CC}	V_{CC}	High Z
Standby (TTL)	V_{IH}	X	X	X	V_{CC}	V_{CC}	High Z
Standby (CMOS)	V_{CC} ±0.3V	X	X	X	V_{CC}	V_{CC}	High Z
Program	V_{IL}	V_{IH}	X	X	V_{CP}	V_{PP}	D_{IN}
Program Verify	V_{IH}	V_{IL}	X	X	V_{CP}	V_{PP}	D_{OUT}
Program Inhibit	V_{IH}	X	X	X	V_{CP}	V_{PP}	High Z
Erase	V_{IL}	V_{IH}	V_{IL}	V_{PE}	V_{CE}	V_{PE}	D_{IH}
Erase Verify	V_{IH}	V_{IL}	X	X	V_{CE}	V_{PE}	D_{OUT}
Erase Inhibit	V_{IH}	X	X	X	V_{CE}	V_{PE}	High Z
Product Identifier-manufacturer	V_{IL}	V_{IL}	V_{IL}	V_{HH}	V_{CC}	V_{CC}	00DA (Hex)
Product Identifier-device	V_{IL}	V_{IL}	V_{IH}	V_{HH}	V_{CC}	V_{CC}	000D (Hex)

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Ambient Temperature with Power Applied	-55 to +125	°C
Storage Temperature	-65 to +125	°C
Voltage on all pins with Respect to Ground Except V_{PP}, A9 and V_{CC} pins	-0.5 to V_{CC} +0.5	V
Voltage on V_{PP} Pin with Respect to Ground	-0.5 to +14.5	V
Voltage on A9 Pin with Respect to Ground	-0.5 to +14.5	V
Voltage on V_{CC} Pin with Respect to Ground	-0.5 to +7	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Erase Characteristics

(T_A = 25° C ±5° C, V_{CC} = 5.0V ± 5%, V_{HH} = 14V)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}	-10	-	10	µA
V_{CC} Erase Current	I_{CP}	$\overline{CE}$ = V_{IL}	-	-	30	mA
V_{PP} Erase Current	I_{PP}	$\overline{CE}$ = V_{IL}	-	-	30	mA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.4	-	5.5	V
Output Low Voltage (Verify)	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	-
A9 Erase Voltage	V_{ID}	-	13.75	14	14.25	V
V_{PP} Erase Voltage	V_{PE}	-	13.75	14	14.25	V
V_{CC} Supply Voltage (Erase)	V_{CE}	-	4.5	5.0	5.5	V

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

CAPACITANCE

(V_{CC} = 5V, T_A = 25° C, f = 1 MHz)

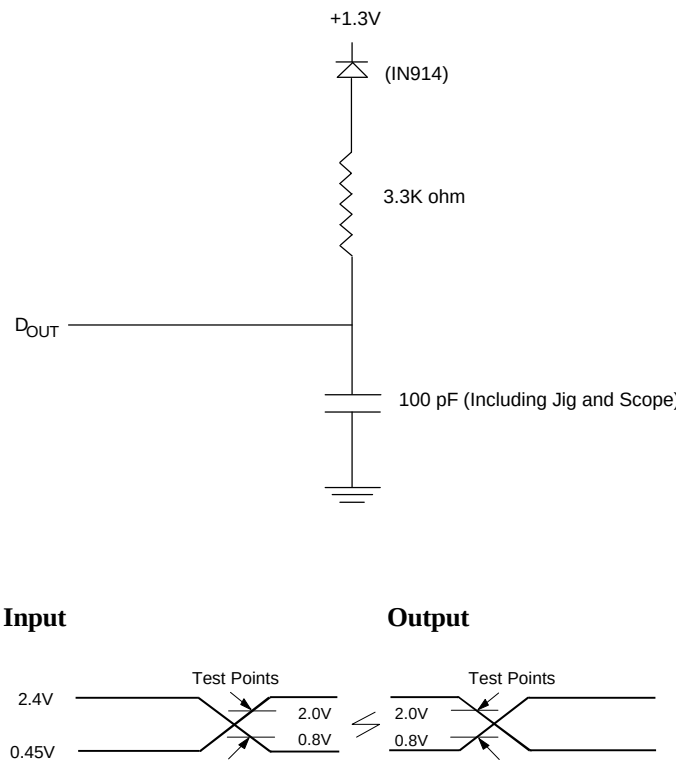
PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	12	pF

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0.45V to 2.4V
Input Rise and Fall Times	10 nS
Input and Output Timing Reference Level	0.8V/2.0V
Output Load	C_L = 100 pF, I_{OH}/I_{OL} = -0.4 mA/2.1 mA

AC Test Load and Waveform



READ OPERATION DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 50° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = 0V to V_{CC}	-5	-	5	µA
Output Leakage Current	I_{LO}	V_{OUT} = 0V to V_{CC}	-10	-	10	µA
V_{CC} Standby Current	I_{SB}	$\overline{CE}$ = V_{IH}	-	-	1.0	mA
	I_{SB1}	$\overline{CE}$ = V_{CC} ±0.2V	-	5	100	µA
V_{CC} Operating Current	I_{CC}	$\overline{CE}$ = V_{IL} I_{OUT} = 0 mA, f = 5 MHz	-	-	30	mA
V_{PP} Operating Current	I_{PP}	V_{PP} = V_{CC}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.2	-	V_{CC} +0.5	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V
V_{PP} Operating Voltage	V_{PP}	-	V_{CC} -0.7	-	V_{CC}	V

READ OPERATION AC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 0 to 50° C)

PARAMETER	SYM.	W27C4096-12		W27C4096-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	120	-	150	-	nS
Chip Enable Access Time	T_{CE}	-	120	-	150	nS
Address Access Time	T_{ACC}	-	120	-	150	nS
Output Enable Access Time	T_{OE}	-	50	-	70	nS
$\overline{OE}$ High to High-Z Output	T_{DF}	-	30	-	30	nS
Output Hold from Address Change	T_{OH}	0	-	0	-	nS

Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

DC PROGRAMMING CHARACTERISTICS

(V_{CC} = 5.0V ±5%, T_A = 25° C ±5° C)

PARAMETER	SYM.	CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Input Load Current	I_{LI}	V_{IN} = V_{IL} or V_{IH}	-10	-	10	µA
V_{CC} Program Current	I_{CP}	$\overline{CE}$ = V_{IL}	-	-	30	mA
V_{PP} Program Current	I_{PP}	$\overline{CE}$ = V_{IL}	-	-	30	mA
Input Low Voltage	V_{IL}	-	-0.3	-	0.8	V
Input High Voltage	V_{IH}	-	2.4	-	5.5	V
Output Low Voltage (Verify)	V_{OL}	I_{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage (Verify)	V_{OH}	I_{OH} = -0.4 mA	2.4	-	-	V
A9 Silicon I.D. Voltage	V_{ID}	-	11.5	12.0	12.5	V
V_{PP} Program Voltage	V_{PP}	-	11.75	12.0	12.25	V
V_{CC} Supply Voltage (Program)	V_{CP}	-	4.5	5.0	5.5	V

AC PROGRAMMING/ERASE CHARACTERISTICS

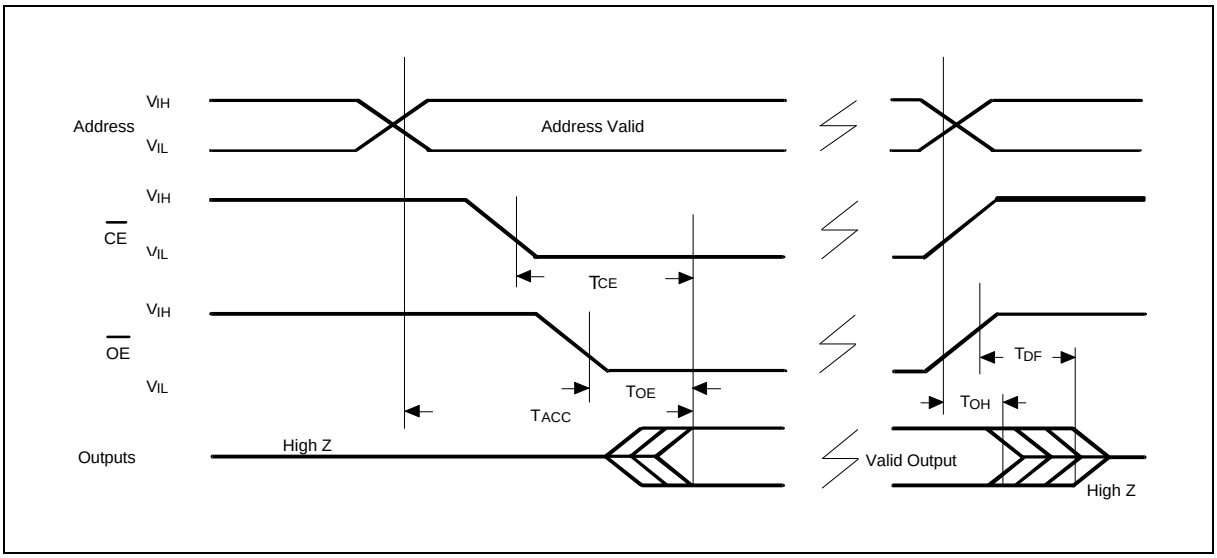
(V_{CC} = 5.0V ±5%, T_A = 25° C ±5° C)

PARAMETER	SYM.	LIMITS			UNIT
		MIN.	TYP.	MAX.	
V_{PP} Setup Time	T_{VPS}	2.0	-	-	µS
Address Setup Time	T_{AS}	2.0	-	-	µS
Data Setup Time	T_{DS}	2.0	-	-	µS
$\overline{CE}$ Program Pulse Width	T_{PWP}	95	100	105	µS
$\overline{CE}$ Erase Pulse Width	T_{PWE}	95	100	105	mS
Data Hold Time	T_{DH}	2.0	-	-	µS
$\overline{OE}$ Setup Time	T_{OES}	2.0	-	-	µS
Data Valid from $\overline{OE}$	T_{OEV}	-	-	150	nS
$\overline{OE}$ High to Output High Z	T_{DFP}	0	-	130	nS
Address Hold Time	T_{AH}	0	-	-	µS
Address Hold Time after $\overline{CE}$ High (Erase)	T_{AHC}	2.0	-	-	µS

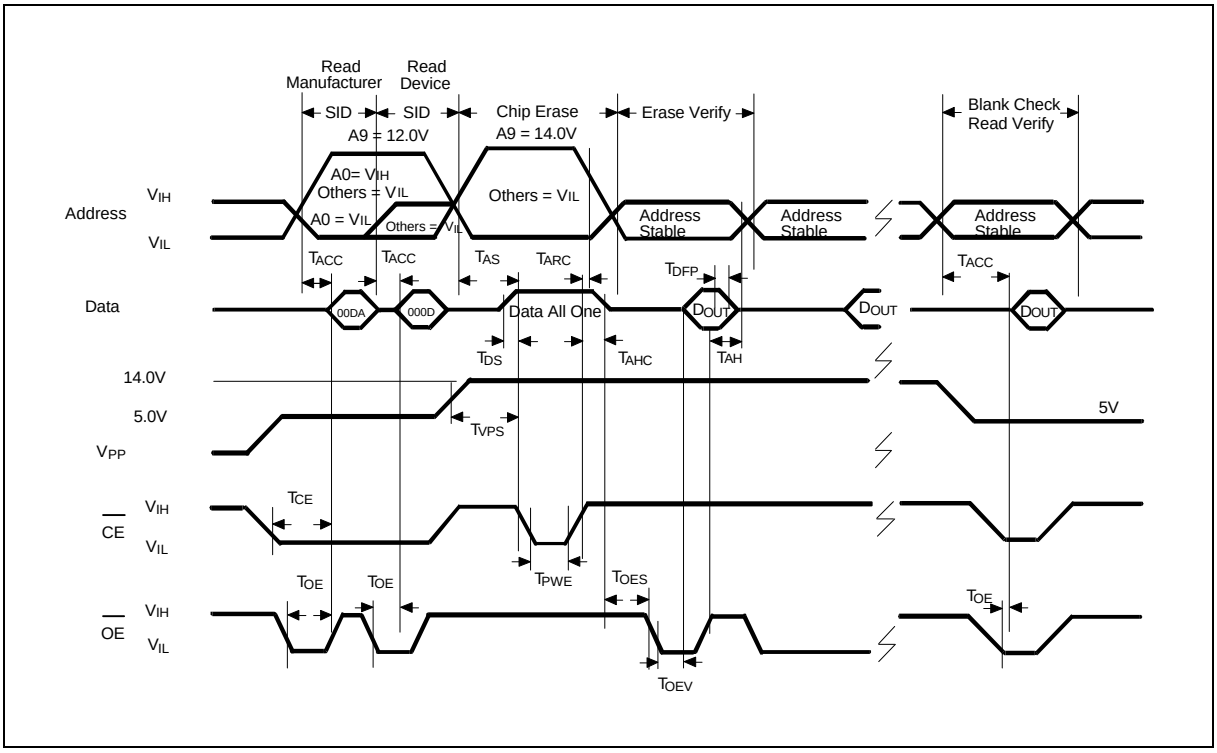
Note: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

TIMING WAVEFORMS

AC Read Waveform

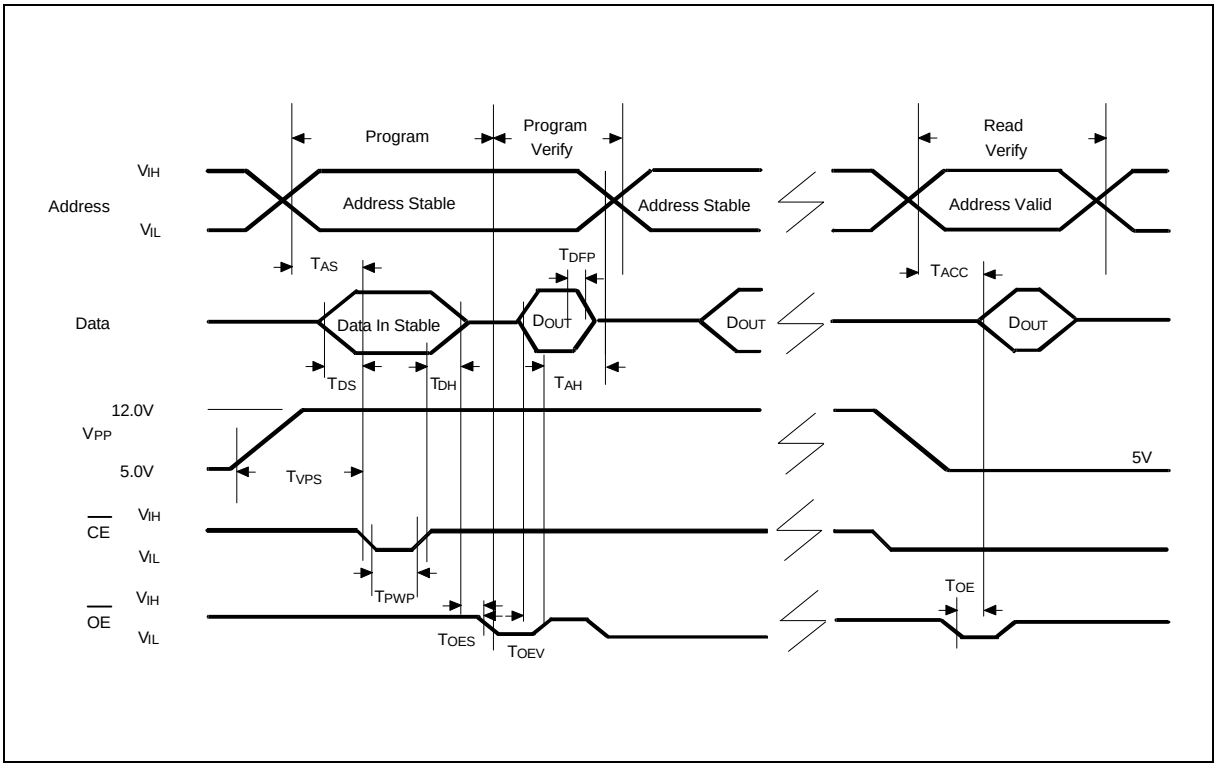


Erase Waveform

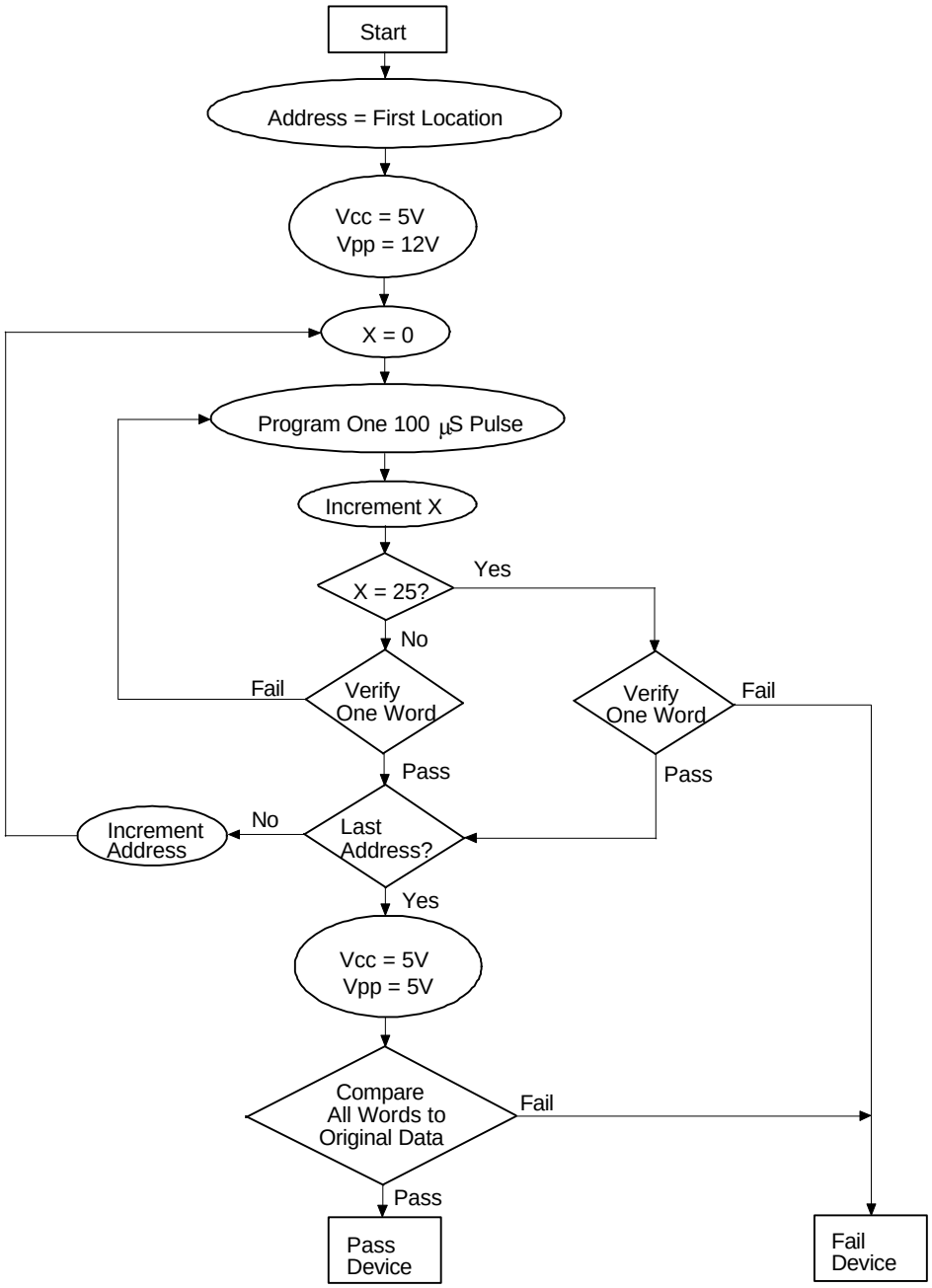


Timing Waveforms, continued

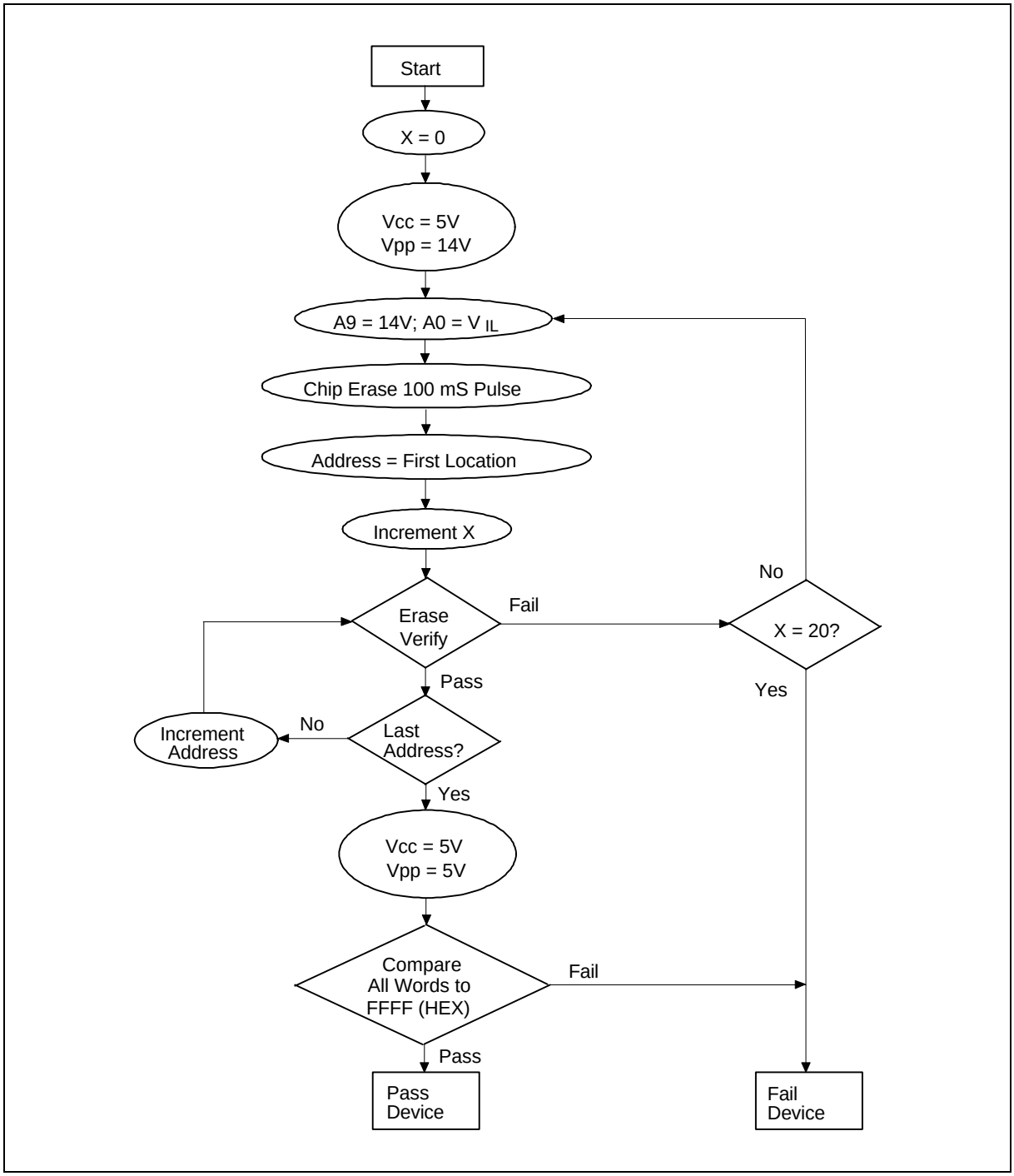
Programming Waveform



SMART PROGRAMMING ALGORITHM



SMART ERASE ALGORITHM



ORDERING INFORMATION

PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY Vcc CURRENT MAX. (mA)	PACKAGE
W27C4096-12	120	30	100	600 mil DIP
W27C4096T-12	120	30	100	40-pin TSOP
W27C4096P-12	120	30	100	44-pin PLCC
W27C4096-15	150	30	100	600 mil DIP
W27C4096T-15	150	30	100	40-pin TSOP
W27C4096P-15	150	30	100	44-pin PLCC

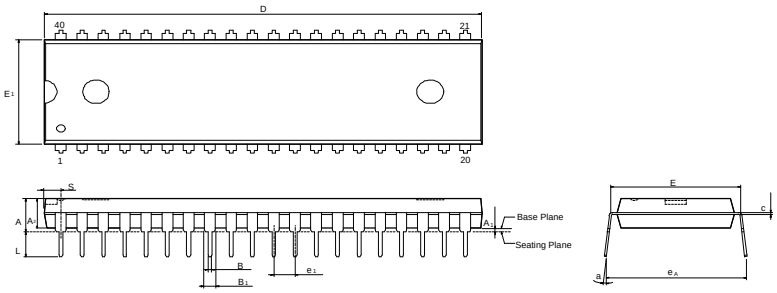
Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

Winbond Electronics Corp.

PACKAGE DIMENSIONS

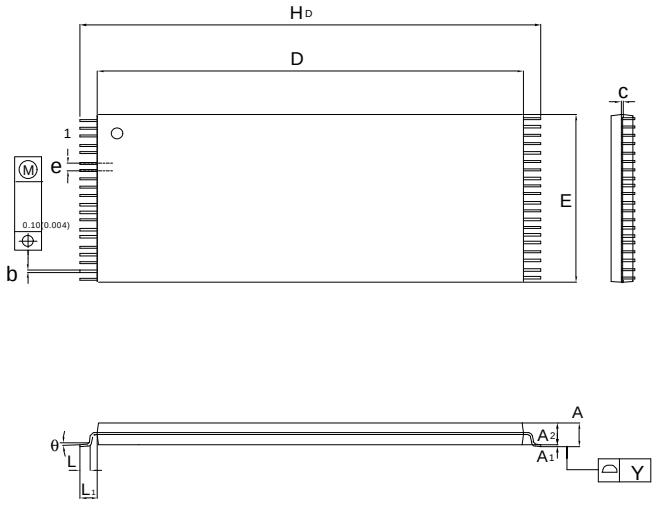
40-pin PDIP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.540	0.545	0.550	13.72	13.84	13.97
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.090	—	—	2.29

Notes:
1. Dimensions D Max & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

40-pin TSOP

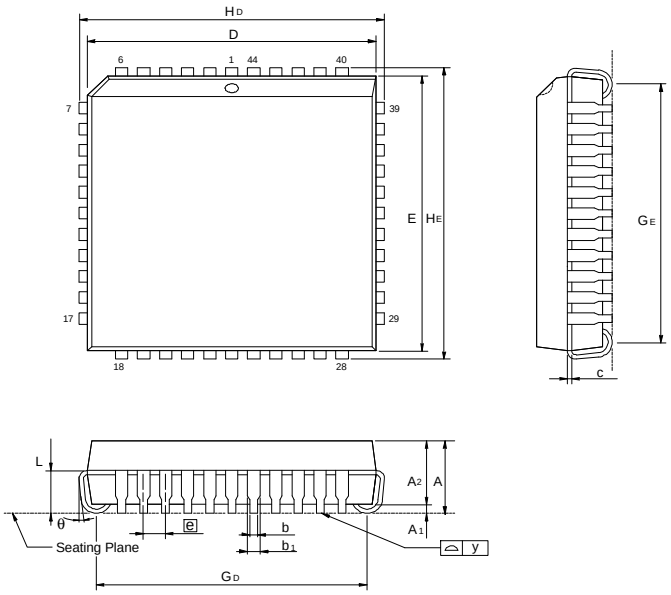


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.72	0.724	0.728	18.3	18.4	18.5
E	0.390	0.394	0.398	9.90	10	10.10
H_D	0.780	0.787	0.795	19.8	20.0	20.2
e		0.020	—	—	0.50	—
L	0.020	0.024	0.028	0.50	0.60	0.70
L_1	—	0.031	—	—	0.8	—
Y	0.000	—	0.004	0.00	—	0.10
θ	0	3	5	0	3	5

Controlling dimension: Millimeters

Package Dimensions, continued

44-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.70
A_1	0.020	—	—	0.51	—	—
A_2	0.145	0.150	0.155	3.68	3.81	3.94
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.29	2.54	2.79
y	—	—	0.004	—	—	0.10

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Mar. 1999		Initial Issued

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-7197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798