Winbond Electronics Corp.

256K × 8 CMOS FLASH MEMORY

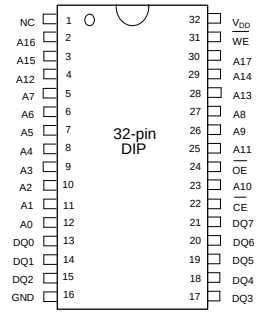
GENERAL DESCRIPTION

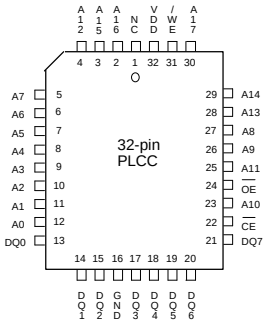
The W29C020 is a 2-megabit, 5-volt only CMOS flash memory organized as 256K × 8 bits. The device can be written (erased and programmed) in-system with a standard 5V power supply. A 12-volt V_{PP} is not required. The unique cell architecture of the W29C020 results in fast write (erase/program) operations with extremely low current consumption compared to other comparable 5-volt flash memory products. The device can also be written (erased and programmed) by using standard EPROM programmers.

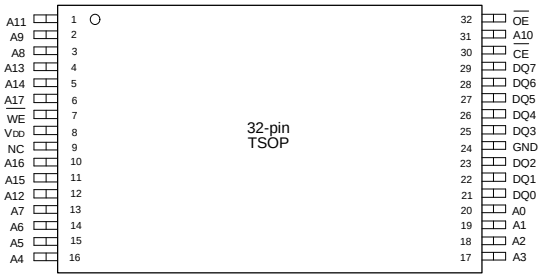
FEATURES

- Single 5-volt write (erase and program) operations
- Fast page-write operations
  - 128 bytes per page
  - Page write (erase/program) cycle: 10 mS (max.)
  - Effective byte-write (erase/program) cycle time: 39 μS
  - Optional software-protected data write
- Fast chip-erase operation: 50 mS
- Two 8 KB boot blocks with lockout
- Typical page write (erase/program) cycles: 100/1K/10K
- Read access time: 70/90/120 nS
- Ten-year data retention
- Software and hardware data protection
- Low power consumption
  - Active current: 25 mA (typ.)
  - Standby current: 20 μA (typ.)
- Automatic write (erase/program) timing with internal V_{PP} generation
- End of write (erase/program) detection
  - Toggle bit
  - Data polling
- Latched address and data
- All inputs and outputs directly TTL compatible
- JEDEC standard byte-wide pinouts
- Available packages: 32-pin 600 mil DIP, 450 mil SOP, TSOP, and 32-pin PLCC

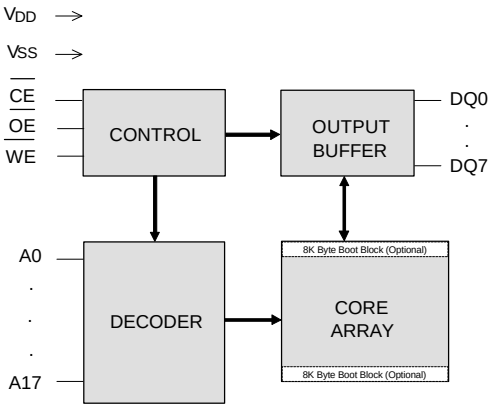
PIN CONFIGURATIONS







BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A17	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VDD	Power Supply
GND	Ground
NC	No Connection

FUNCTIONAL DESCRIPTION

Read Mode

The read operation of the W29C020 is controlled by $\overline{CE}$ and $\overline{OE}$, both of which have to be low for the host to obtain data from the outputs. $\overline{CE}$ is used for device selection. When $\overline{CE}$ is high, the chip is de-selected and only standby power will be consumed. $\overline{OE}$ is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high.

Refer to the read cycle timing waveforms for further details.

Page Write Mode

The W29C020 is written (erased/programmed) on a page basis. Every page contains 128 bytes of data. If a byte of data within a page is to be changed, data for the entire page must be loaded into the device. Any byte that is not loaded will be erased to "FF hex" during the write operation of the page.

The write operation is initiated by forcing $\overline{CE}$ and $\overline{WE}$ low and $\overline{OE}$ high. The write procedure consists of two steps. Step 1 is the byte-load cycle, in which the host writes to the page buffer of the device.

Step 2 is an internal write (erase/program) cycle, during which the data in the page buffers are simultaneously written into the memory array for non-volatile storage.

During the byte-load cycle, the addresses are latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data are latched by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. If the host loads a second byte into the page buffer within a byte-load cycle time (T_{BLC}) of 200 μS after the initial byte-load cycle, the W29C020 will stay in the page load cycle. Additional bytes can then be loaded consecutively. The page load cycle will be terminated and the internal write (erase/program) cycle will start if no additional byte is loaded into the page buffer A7 to A17 specify the page address. All bytes that are loaded into the page buffer must have the same page address. A0 to A6 specify the byte address within the page. The bytes may be loaded in any order; sequential loading is not required.

In the internal write cycle, all data in the page buffers, i.e., 128 bytes of data, are written simultaneously into the memory array. Before the completion of the internal write cycle, the host is free to perform other tasks such as fetching data from other locations in the system to prepare to write the next page.

Software-protected Data Write

The device provides a JEDEC-approved optional software-protected data write. Once this scheme is enabled, any write operation requires a three-byte command sequence (with specific data to a specific address) to be performed before the data load operation. The three-byte load command sequence begins the page load cycle, without which the write operation will not be activated. This write scheme provides optimal protection against inadvertent write cycles, such as cycles triggered by noise during system power-up and power-down.

The W29C020 is shipped with the software data protection enabled. To enable the software data protection scheme, perform the three-byte command cycle at the beginning of a page load cycle. The device will then enter the software data protection mode, and any subsequent write operation must be preceded by the three-byte command sequence cycle. Once enabled, the software data protection

will remain enabled unless the disable commands are issued. A power transition will not reset the software data protection feature. To reset the device to unprotected mode, a six-byte command sequence is required. For information about specific codes, see the Command Codes for Software Data Protection in the Table of Operating Modes. For information about timing waveforms, see the timing diagrams below.

Hardware Data Protection

The integrity of the data stored in the W29C020 is also hardware protected in the following ways:

(1) Noise/Glitch Protection: A $\overline{WE}$ pulse of less than 15 nS in duration will not initiate a write cycle.

(2) V_{DD} Power Up/Down Detection: The write operation is inhibited when V_{DD} is less than 2.5V.

(3) Write Inhibit Mode: Forcing $\overline{OE}$ low, $\overline{CE}$ high, or $\overline{WE}$ high will inhibit the write operation. This prevents inadvertent writes during power-up or power-down periods.

(4) V_{DD} power-on delay: When V_{DD} reaches its sense level, the device will automatically timeout for 5 mS before any write (erase/program) operation.

Chip Erase Modes

The entire device can be erased by using a six-byte software command code. See the Software Chip Erase Timing Diagram.

Boot Block Operation

There are two boot blocks (8K bytes each) in this device, which can be used to store boot code. One of them is located in the first 8K bytes and the other is located in the last 8K bytes of the memory. The first 8K or last 8K of the memory can be set as a boot block by using a seven-byte command sequence.

See Command Codes for Boot Block Lockout Enable for the specific code. Once this feature is set the data for the designated block cannot be erased or programmed (programming lockout); other memory locations can be changed by the regular programming method. Once the boot block programming lockout feature is activated, the chip erase function will be disabled. In order to detect whether the boot block feature is set on the two 8K blocks, users can perform a six-byte command sequence: enter the product identification mode (see Command Codes for Identification/Boot Block Lockout Detection for specific code), and then read from address "00002 hex" (for the first 8K bytes) or "3FFF2 hex" (for the last 8K bytes). If the output data is "FF hex," the boot block programming lockout feature is activated; if the output data is "FE hex," the lockout feature is deactivated and the block can be programmed.

To return to normal operation, perform a three-byte command sequence to exit the identification mode. For the specific code, see Command Codes for Identification/Boot Block Lockout Detection.

Data Polling (DQ7)- Write Status Detection

The W29C020 includes a data polling feature to indicate the end of a write cycle. When the W29C020 is in the internal write cycle, any attempt to read DQ7 from the last byte loaded during the page/byte-load cycle will receive the complement of the true data. Once the write cycle is completed. DQ7 will show the true data. See the $\overline{DATA}$ Polling Timing Diagram.

Toggle Bit (DQ6)- Write Status Detection

In addition to data polling, the W29C020 provides another method for determining the end of a write cycle. During the internal write cycle, any consecutive attempts to read DQ6 will produce alternating 0's and 1's. When the write cycle is completed, this toggling between 0's and 1's will stop. The device is then ready for the next operation. See Toggle Bit Timing Diagram.

Product Identification

The product ID operation outputs the manufacturer code and device code. The programming equipment automatically matches the device with its proper erase and programming algorithms.

The manufacturer and device codes can be accessed through software or by hardware operation. In the software access mode, a six-byte command sequence can be used to access the product ID. A read from address "00000 hex" outputs the manufacturer code "DA hex." A read from address "00001 hex" outputs the device code "45 hex." The product ID operation can be terminated by a three-byte command sequence.

In the hardware access mode, access to the product ID is activated by forcing $\overline{CE}$ and $\overline{OE}$ low, $\overline{WE}$ high, and raising A9 to 12 volts.

TABLE OF OPERATING MODES

Operating Mode Selection

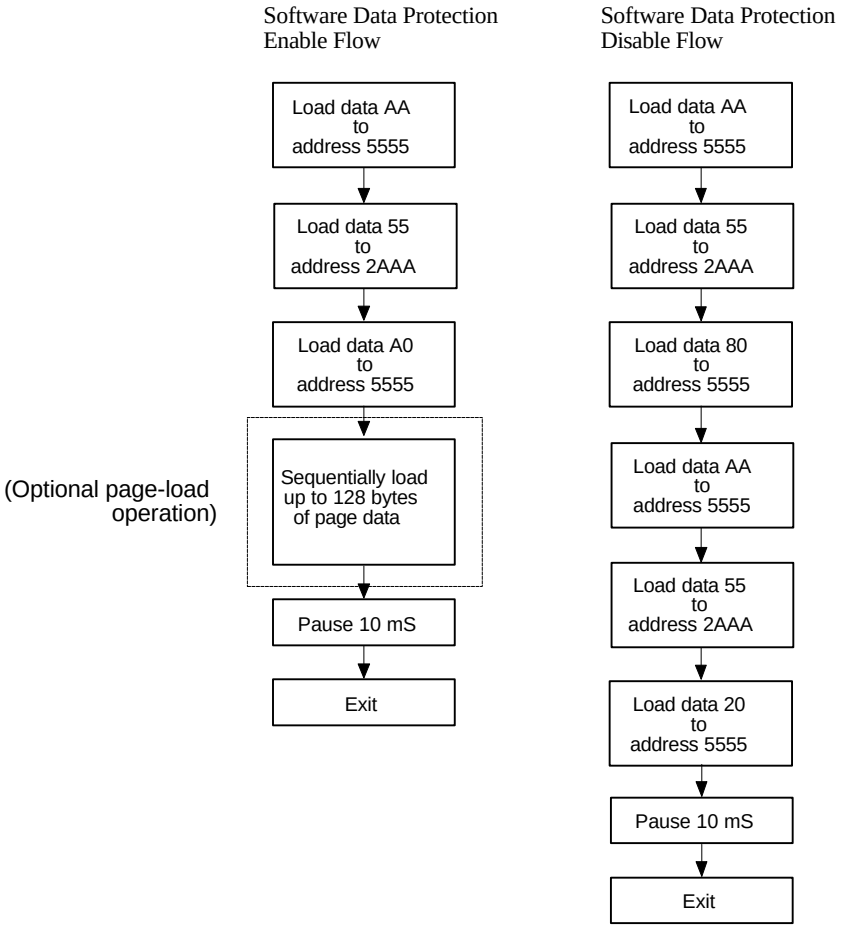
Operating Range: 0 to 70° C (Ambient Temperature), V_{DD} = 5V ±10%, V_{SS} = 0V, V_{HH} = 12V

MODE	PINS				
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	ADDRESS	DQ.
Read	V_{IL}	V_{IL}	V_{IH}	A_{IN}	Dout
Write	V_{IL}	V_{IH}	V_{IL}	A_{IN}	Din
Standby	V_{IH}	X	X	X	High Z
Write Inhibit	X	V_{IL}	X	X	High Z/D_{OUT}
	X	X	V_{IH}	X	High Z/D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
5-Volt Software Chip Erase	V_{IL}	V_{IH}	V_{IL}	A_{IN}	D_{IN}
Product ID	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}; A1–A17 = V_{IL}; A9 = V_{HH}	Manufacturer Code DA (Hex)
	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}; A1–A17 = V_{IL}; A9 = V_{HH}	Device Code 45 (Hex)

Command Codes for Software Data Protection

BYTE SEQUENCE	TO ENABLE PROTECTION		TO DISABLE PROTECTION	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	A0H	5555H	80H
3 Write	-	-	5555H	AAH
4 Write	-	-	2AAAH	55H
5 Write	-	-	5555H	20H

Software Data Protection Acquisition Flow

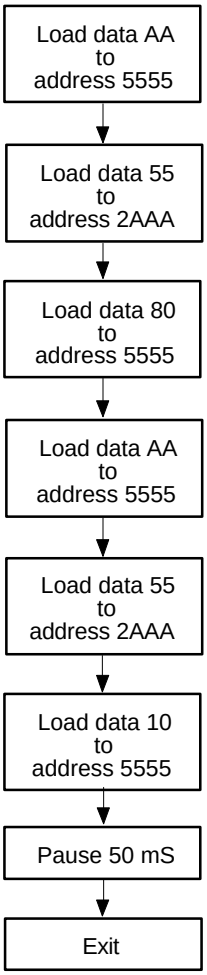


Notes for software program code:
Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Software Chip Erase

BYTE SEQUENCE	ADDRESS	DATA
0 Write	5555H	AAH
1 Write	2AAAH	55H
2 Write	5555H	80H
3 Write	5555H	AAH
4 Write	2AAAH	55H
5 Write	5555H	10H

Software Chip Erase Acquisition Flow

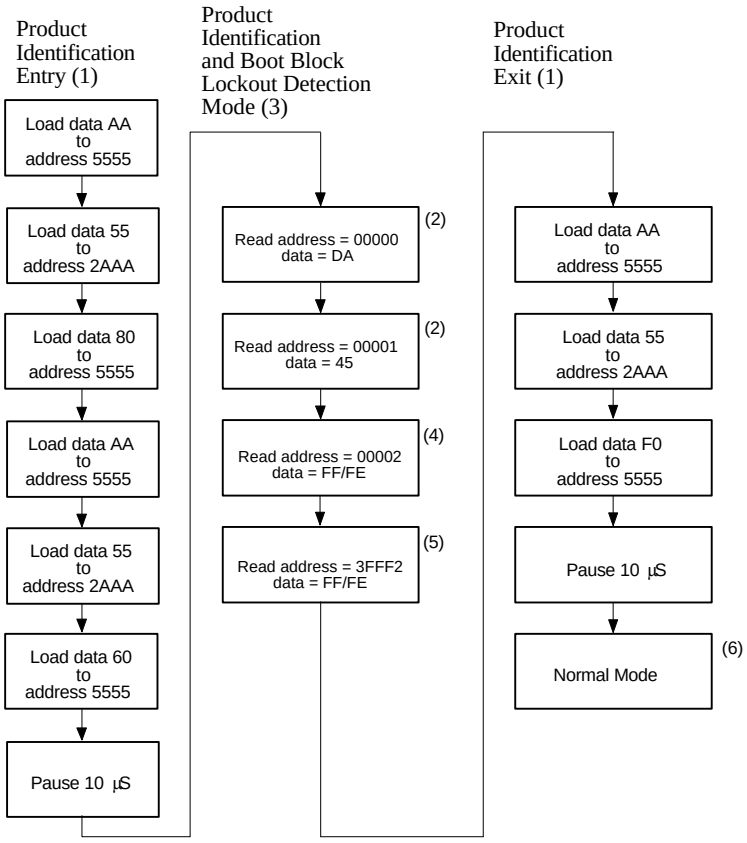


Notes for software chip erase:
Data Format: DQ7–DQ0 (Hex)
Address Format: A14–A0 (Hex)

Command Codes for Product Identification and Boot Block Lockout Detection

BYTE SEQUENCE	ALTERNATE PRODUCT (7) IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION ENTRY		SOFTWARE PRODUCT IDENTIFICATION/BOOT BLOCK LOCKOUT DETECTION EXIT	
	ADDRESS	DATA	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555	AA	5555H	AAH	5555H	AAH
1 Write	2AAA	55	2AAAH	55H	2AAAH	55H
2 Write	5555	90	5555H	80H	5555H	F0H
3 Write	-	-	5555H	AAH	-	-
4 Write	-	-	2AAAH	55H	-	-
5 Write	-	-	5555H	60H	-	-
	Pause 10 µS		Pause 10 µS		Pause 10 µS	

Software Product Identification and Boot Block Lockout Detection Acquisition Flow



Notes for software product identification/boot block lockout detection:

(1) Data Format: DQ7–DQ0 (Hex); Address Format: A14–A0 (Hex)

(2) A1–A16 = V_{IL}; manufacture code is read for A0 = V_{IL}; device code is read for A0 = V_{IH}.

(3) The device does not remain in identification and boot block (address 0002 Hex/3FFF2 Hex respond to first 8K/last 8K) lockout detection mode if power down.

(4), (5) If the output data is "FF Hex," the boot block programming lockout feature is activated; if the output data "FE Hex," the lockout feature is inactivated and the block can be programmed.

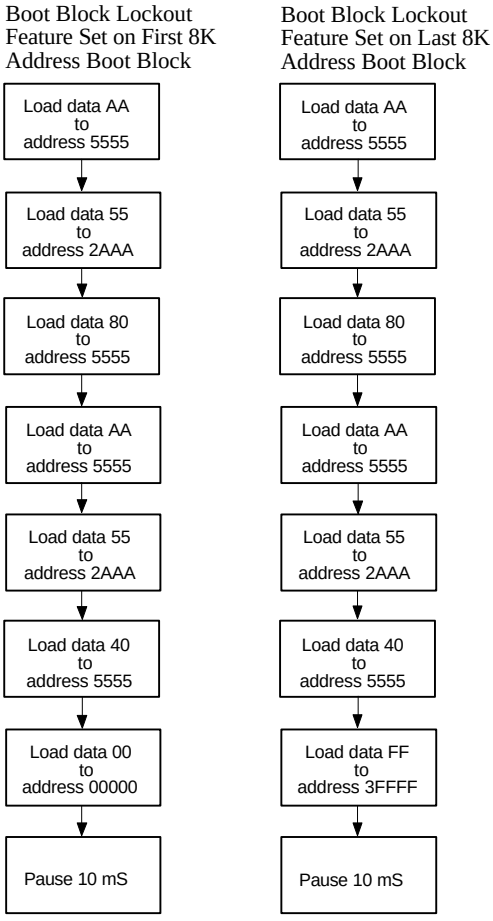
(6) The device returns to standard operation mode.

(7) This product supports both the JEDEC standard 3 byte command code sequence and original 6 byte command code sequence. For new designs, Winbond recommends that the 3 byte command code sequence be used.

Command Codes for Boot Block Lockout Enable

BYTE SEQUENCE	BOOT BLOCK LOCKOUT FEATURE SET ON FIRST 8K ADDRESS BOOT BLOCK		BOOT BLOCK LOCKOUT FEATURE SET ON LAST 8K ADDRESS BOOT BLOCK	
	ADDRESS	DATA	ADDRESS	DATA
0 Write	5555H	AAH	5555H	AAH
1 Write	2AAAH	55H	2AAAH	55H
2 Write	5555H	80H	5555H	80H
3 Write	5555H	AAH	5555H	AAH
4 Write	2AAAH	55H	2AAAH	55H
5 Write	5555H	40H	5555H	40H
6 Write	00000H	00H	3FFFFH	FFH
	Pause 10 mS		Pause 10 mS	

Boot Block Lockout Enable Acquisition Flow



Notes for boot block lockout enable:

1. Data Format: DQ7–DQ0 (Hex)
2. Address Format: A14–A0 (Hex)
3. If you have any questions about this commend sequence, please contact the local distributor or Winbond Electronics Corp.

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage to V_{SS} Potential	-0.5 to +7.0	V
Operating Temperature	0 to +70	°C
Storage Temperature	-65 to +150	°C
D.C. Voltage on Any Pin to Ground Potential Except A9	-0.5 to V_{DD} +1.0	V
Transient Voltage (<20 nS) on Any Pin to Ground Potential	-1.0 to V_{DD} +1.0	V
Voltage on A9 and $\overline{OE}$ Pin to Ground Potential	-0.5 to 12.5	V

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	TEST CONDITIONS	LIMITS			UNIT
			MIN.	TYP.	MAX.	
Power Supply Current	I_{CC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, all DQs open Address inputs = V_{IL}/V_{IH}, at f = 5 MHz	-	-	50	mA
Standby V_{DD} Current (TTL input)	I_{SB1}	$\overline{CE}$ = V_{IH}, all DQs open Other inputs = V_{IL}/V_{IH}	-	2	3	mA
Standby V_{DD} Current (CMOS input)	I_{SB2}	$\overline{CE}$ = V_{DD} -0.3V, all DQs open	-	20	100	µA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	-	-	10	µA
Output Leakage Current	I_{LO}	V_{IN} = GND to V_{DD}	-	-	10	µA
Input Low Voltage	V_{IL}	-	-	-	0.8	V
Input High Voltage	V_{IH}	-	2.0	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2.0 mA	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -400 µA	2.4	-	-	V
Output High Voltage CMOS	V_{OH2}	I_{OH} = -100 µA; V_{CC} = 4.5V	4.2	-	-	V

Power-up Timing

PARAMETER	SYMBOL	TYPICAL	UNIT
Power-up to Read Operation	TPU. READ	100	µS
Power-up to Write Operation	TPU. WRITE	5	mS

CAPACITANCE

(V_{DD} = 5.0V, T_A = 25° C, f = 1 MHz)

PARAMETER	SYMBOL	CONDITIONS	MAX.	UNIT
DQ Pin Capacitance	C_{DQ}	V_{DQ} = 0V	12	pF
Input Pin Capacitance	C_{IN}	V_{IN} = 0V	6	pF

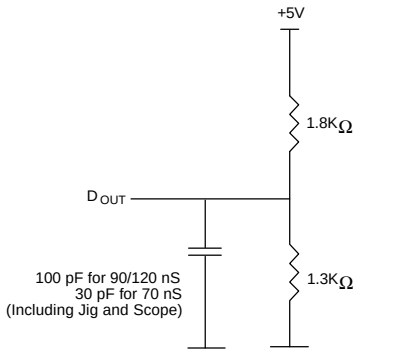
AC CHARACTERISTICS

AC Test Conditions

(V_{DD} = 5.0V ±10% for 90 nS and 120 nS; V_{DD} = 5.0V ±5% for 70 nS)

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise/Fall Time	<5 nS
Input/Output Timing Level	1.5V/1.5V
Output Load	1 TTL Gate and C_L = 100 pF for 90/120 nS C_L = 30 pF for 70 nS

AC Test Load and Waveform



AC Characteristics, continued

Read Cycle Timing Parameters

(V_{DD} = 5.0V ±10% for 90 nS and 120 nS; V_{DD} = 5.0V ±5% for 70 nS, V_{SS} = 0V, T_A = 0 to 70° C)

PARAMETER	SYM.	W29C020-70		W29C020-90		W29C020-12		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	T_{RC}	70	-	90	-	120	-	nS
Chip Enable Access Time	T_{CE}	-	70	-	90	-	120	nS
Address Access Time	T_{AA}	-	70	-	90	-	120	nS
Output Enable Access Time	T_{OE}	-	35	-	40	-	50	nS
$\overline{CE}$ High to High-Z Output	T_{CHZ}	-	25	-	25	-	30	nS
$\overline{OE}$ High to High-Z Output	T_{OHZ}	-	25	-	25	-	30	nS
Output Hold from Address change	T_{OH}	0	-	0	-	0	-	nS

Byte/Page-write Cycle Timing Parameters

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Write Cycle (erase and program)	T_{WC}	-	-	10	mS
Address Setup Time	T_{AS}	0	-	-	nS
Address Hold Time	T_{AH}	50	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Setup Time	T_{CS}	0	-	-	nS
$\overline{WE}$ and $\overline{CE}$ Hold Time	T_{CH}	0	-	-	nS
$\overline{OE}$ High Setup Time	T_{OES}	0	-	-	nS
$\overline{OE}$ High Hold Time	T_{OEH}	0	-	-	nS
$\overline{CE}$ Pulse Width	T_{CP}	70	-	-	nS
$\overline{WE}$ Pulse Width	T_{WP}	70	-	-	nS
$\overline{WE}$ High Width	T_{WPH}	100	-	-	nS
Data Setup Time	T_{DS}	50	-	-	nS
Data Hold Time	T_{DH}	0	-	-	nS
Byte Load Cycle Time	T_{BLC}	-	-	150	µS

Note: All AC timing signals observe the following guideline for determining setup and hold times:
Reference level is V_{IH} for high-level signal and V_{IL} for low-level signal.

AC Characteristics, continued

$\overline{DA}$ $\overline{TA}$ Polling Characteristics (1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T_{DH}	10	-	-	nS
$\overline{OE}$ Hold Time	T_{OEH}	10	-	-	nS
$\overline{OE}$ to Output Delay (2)	T_{OE}	-	-	-	nS
Write Recovery Time	T_{WR}	0	-	-	nS

Notes:

(1) These parameters are characterized and not 100% tested.

(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

Toggle Bit Characteristics (1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Data Hold Time	T_{DH}	10	-	-	nS
$\overline{OE}$ Hold Time	T_{OEH}	10	-	-	nS
$\overline{OE}$ to Output Delay (2)	T_{OE}	-	-	-	nS
$\overline{OE}$ High Pulse	T_{OEHP}	150	-	-	nS
Write Recovery Time	T_{WR}	0	-	-	nS

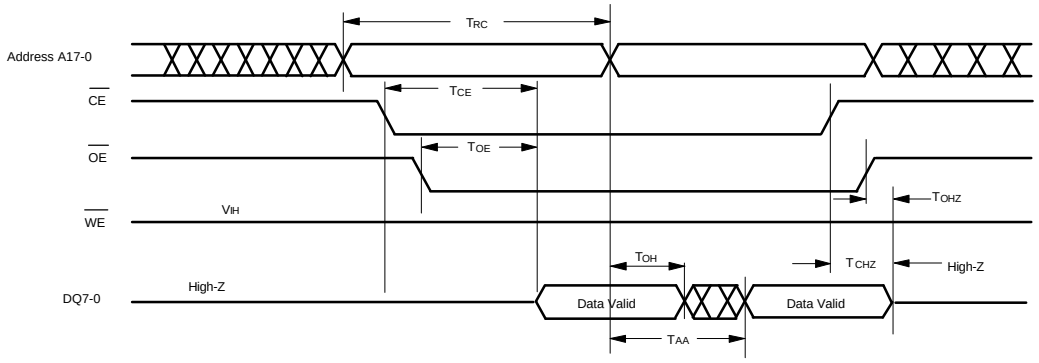
Notes:

(1) These parameters are characterized and not 100% tested.

(2) See T_{OE} spec in A.C. Read Cycle Timing Parameters.

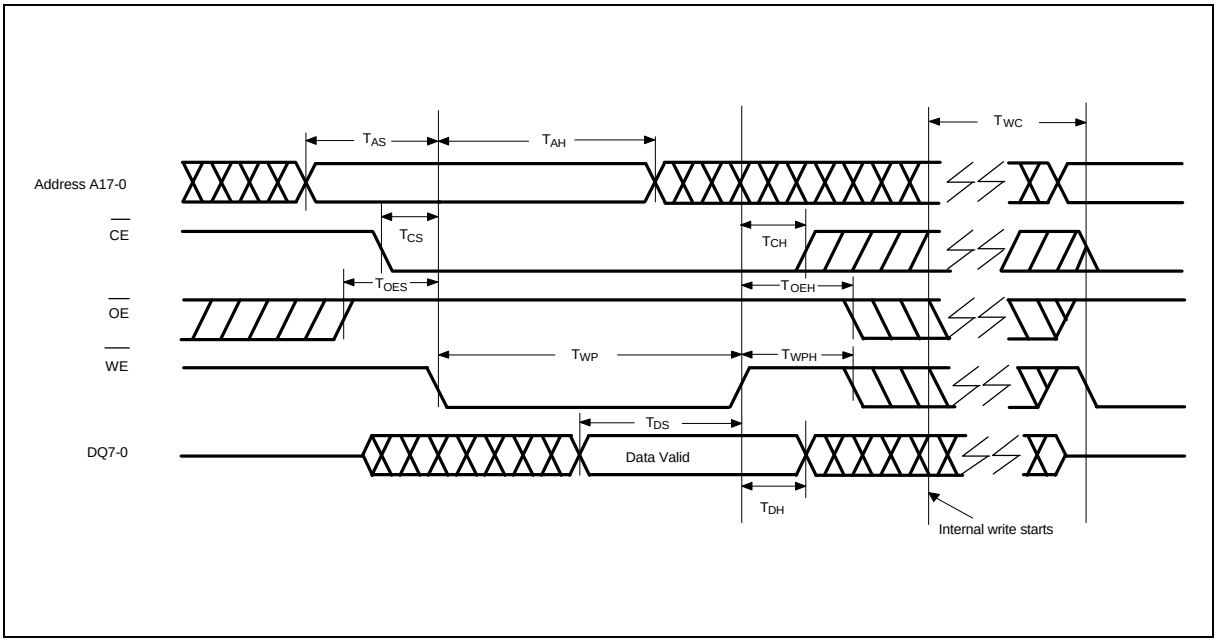
TIMING WAVEFORMS

Read Cycle Timing Diagram

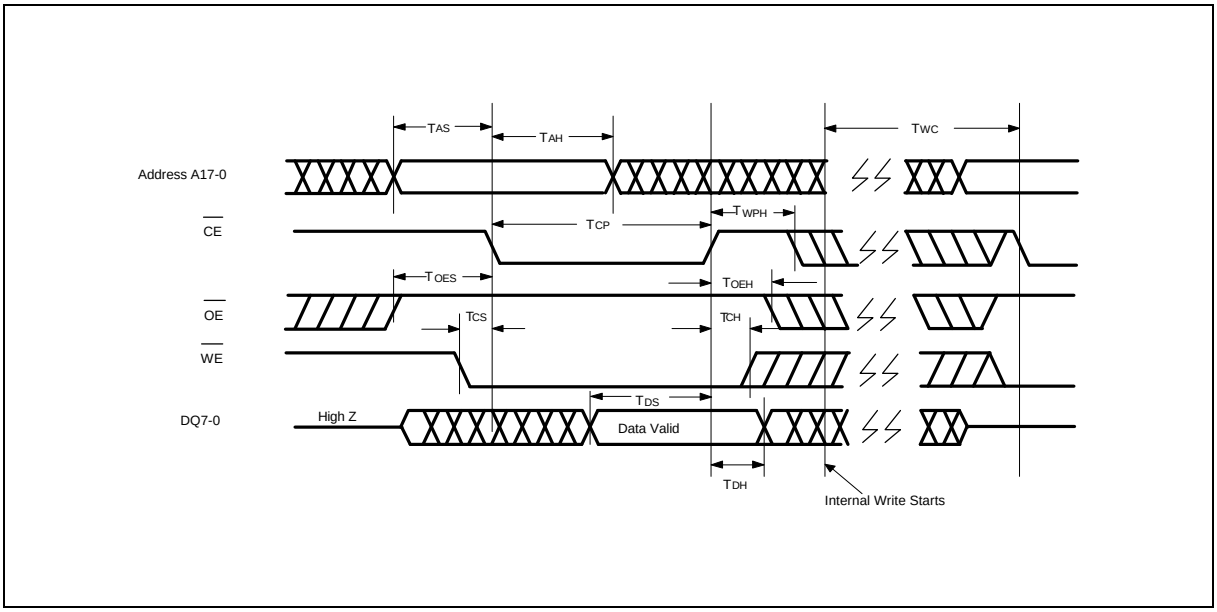


Timing Waveforms, continued

$\overline{WE}$ Controlled Write Cycle Timing Diagram

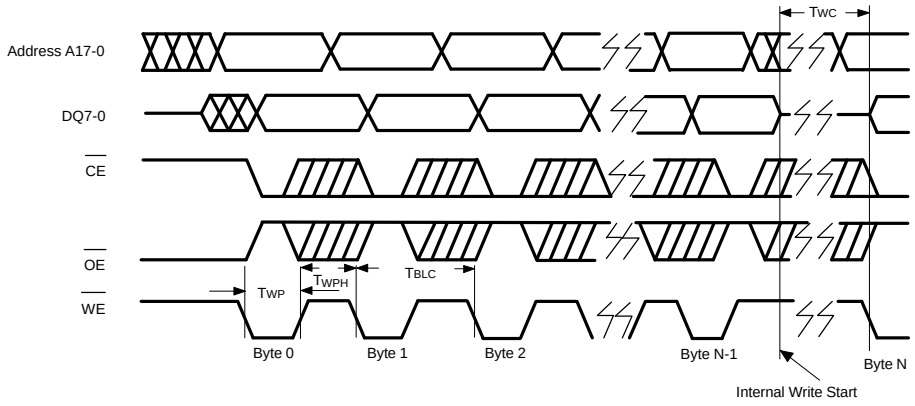


$\overline{CE}$ Controlled Write Cycle Timing Diagram

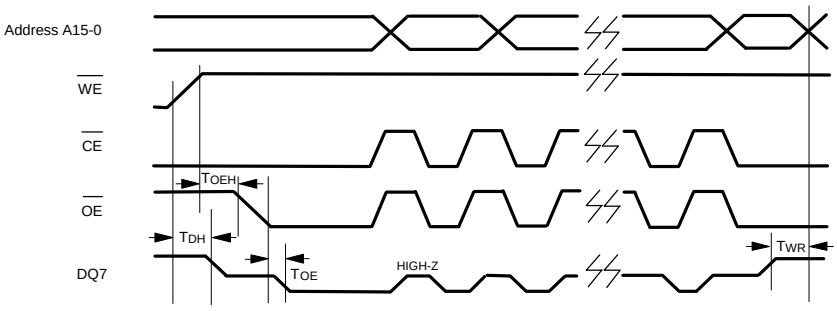


Timing Waveforms, continued

Page Write Cycle Timing Diagram

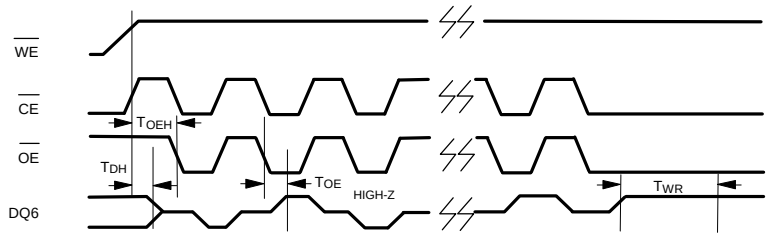


DA TA Polling Timing Diagram

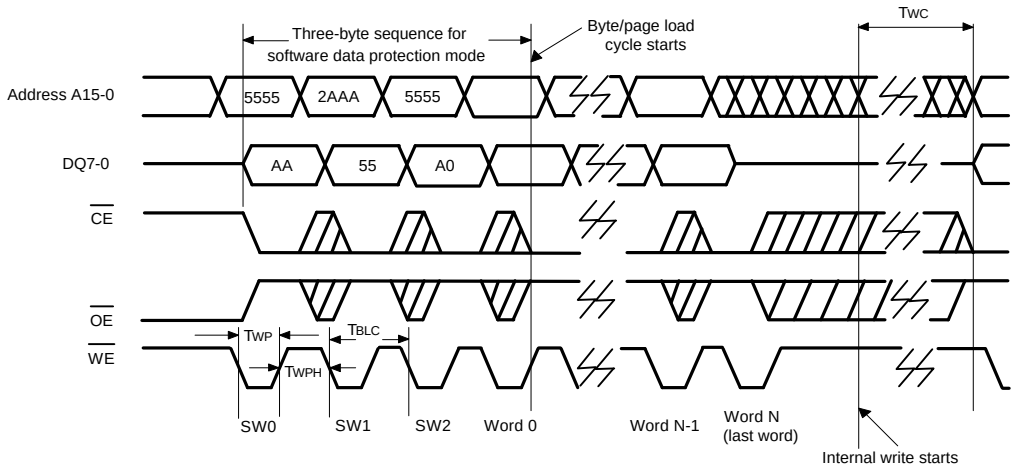


Timing Waveforms, continued

Toggle Bit Timing Diagram

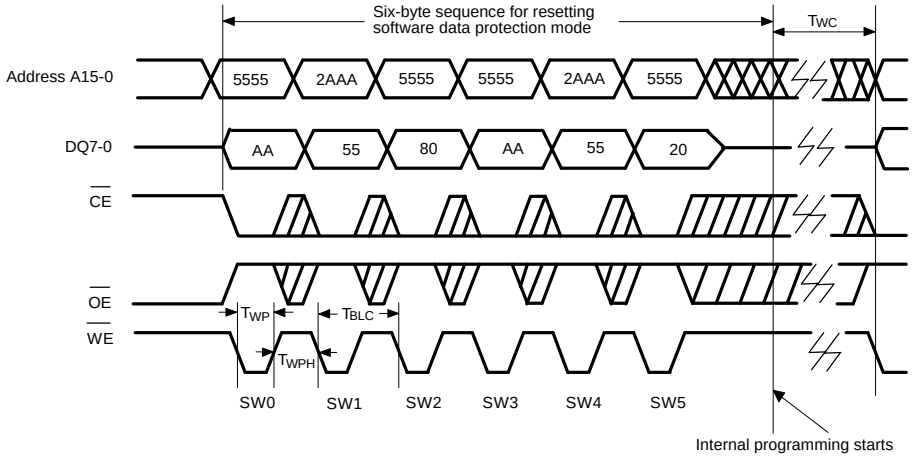


Page Write Timing Diagram Software Data Protection Mode

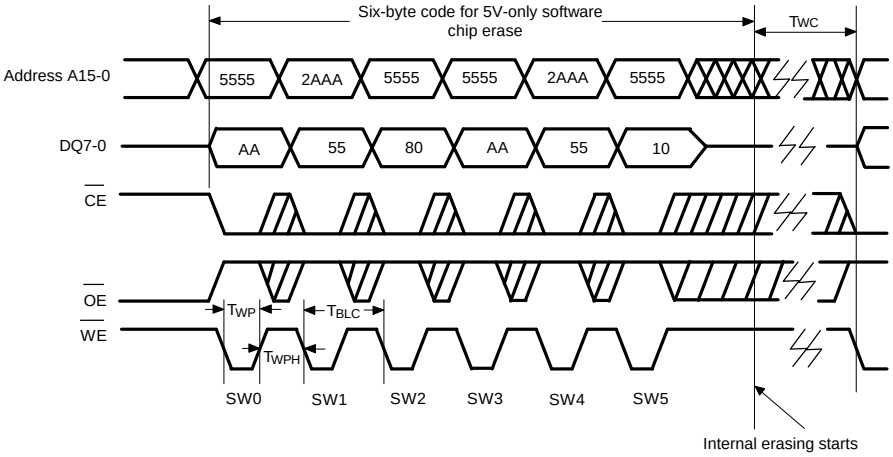


Timing Waveforms, continued

Reset Software Data Protection Timing Diagram



Software Chip Erase Timing Diagram



ORDERING INFORMATION

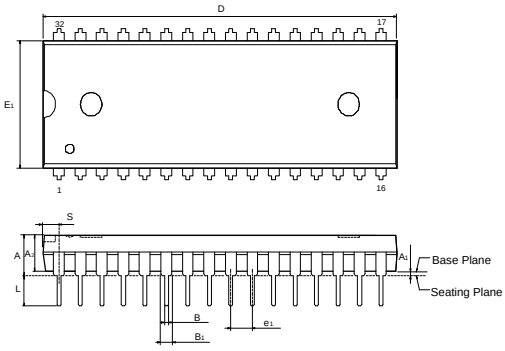
PART NO.	ACCESS TIME (nS)	POWER SUPPLY CURRENT MAX. (mA)	STANDBY V_{DD} CURRENT MAX. (mA)	PACKAGE	CYCLING
W29C020-70A	70	50	100	600 mil DIP	100
W29C020-90A	90	50	100	600 mil DIP	100
W29C020-12A	120	50	100	600 mil DIP	100
W29C020S-70A	70	50	100	450 mil SOP	100
W29C020S-90A	90	50	100	450 mil SOP	100
W29C020S-12A	120	50	100	450 mil SOP	100
W29C020T-70A	70	50	100	Type one TSOP	100
W29C020T-90A	90	50	100	Type one TSOP	100
W29C020T-12A	120	50	100	Type one TSOP	100
W29C020P-70A	70	50	100	32-pin PLCC	100
W29C020P-90A	90	50	100	32-pin PLCC	100
W29C020P-12A	120	50	100	32-pin PLCC	100
W29C020-70	70	50	100	600 mil DIP	1K
W29C020-90	90	50	100	600 mil DIP	1K
W29C020-12	120	50	100	600 mil DIP	1K
W29C020S-70	70	50	100	450 mil SOP	1K
W29C020S-90	90	50	100	450 mil SOP	1K
W29C020S-12	120	50	100	450 mil SOP	1K
W29C020T-70	70	50	100	Type one TSOP	1K
W29C020T-90	90	50	100	Type one TSOP	1K
W29C020T-12	120	50	100	Type one TSOP	1K
W29C020P-70	70	50	100	32-pin PLCC	1K
W29C020P-90	90	50	100	32-pin PLCC	1K
W29C020P-12	120	50	100	32-pin PLCC	1K
W29C020-70B	70	50	100	600 mil DIP	10K
W29C020-90B	90	50	100	600 mil DIP	10K
W29C020-12B	120	50	100	600 mil DIP	10K
W29C020S-70B	70	50	100	450 mil SOP	10K
W29C020S-90B	90	50	100	450 mil SOP	10K
W29C020S-12B	120	50	100	450 mil SOP	10K
W29C020T-70B	70	50	100	Type one TSOP	10K
W29C020T-90B	90	50	100	Type one TSOP	10K
W29C020T-12B	120	50	100	Type one TSOP	10K
W29C020P-70B	70	50	100	32-pin PLCC	10K
W29C020P-90B	90	50	100	32-pin PLCC	10K
W29C020P-12B	120	50	100	32-pin PLCC	10K

Notes:

1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

PACKAGE DIMENSIONS

32-pin P-DIP

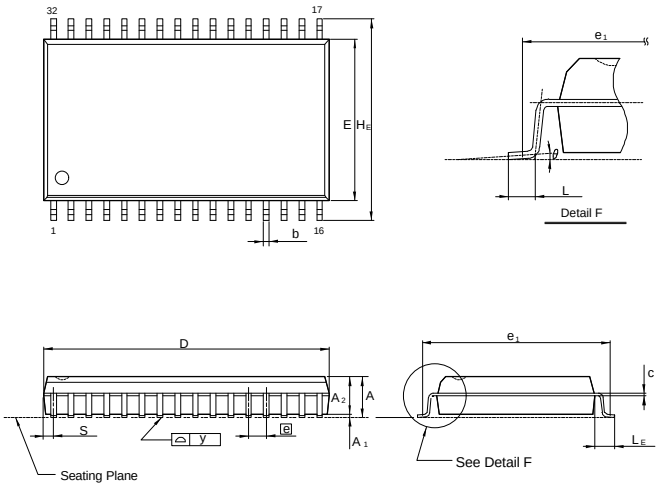


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.33
A_1	0.010	—	—	0.25	—	—
A_2	0.150	0.155	0.160	3.81	3.94	4.06
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.048	0.050	0.054	1.22	1.27	1.37
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.650	1.660	—	41.91	42.16
E	0.590	0.600	0.610	14.99	15.24	15.49
E_1	0.545	0.550	0.555	13.84	13.97	14.10
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
a	0	—	15	0	—	15
e_A	0.630	0.650	0.670	16.00	16.51	17.02
S	—	—	0.085	—	—	2.16

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimensions D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

32-pin SO Wide Body



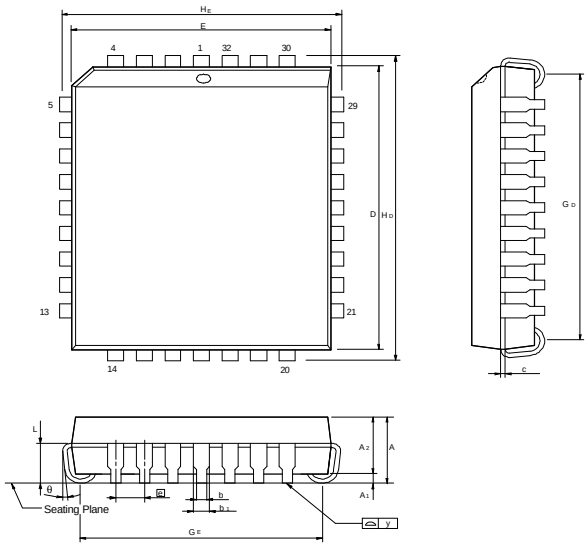
Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.118	—	—	3.00
A_1	0.004	—	—	0.10	—	—
A_2	0.101	0.106	0.111	2.57	2.69	2.82
b	0.014	0.016	0.020	0.36	0.41	0.51
c	0.006	0.008	0.012	0.15	0.20	0.31
D	—	0.805	0.817	—	20.45	20.75
E	0.440	0.445	0.450	11.18	11.30	11.43
e	0.044	0.050	0.056	1.12	1.27	1.42
H_E	0.546	0.556	0.556	13.87	14.12	14.38
L	0.023	0.031	0.039	0.58	0.79	0.99
L_E	0.047	0.055	0.063	1.19	1.40	1.60
S	—	—	0.036	—	—	0.91
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D Max. & S include mold flash or tie bar burrs.
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimensions D & E include mold mismatch and determined at the mold parting line.
4. Controlling dimension: Inches.
5. General appearance spec should be based on final visual inspection spec.

Package Dimensions, continued

32-pin PLCC

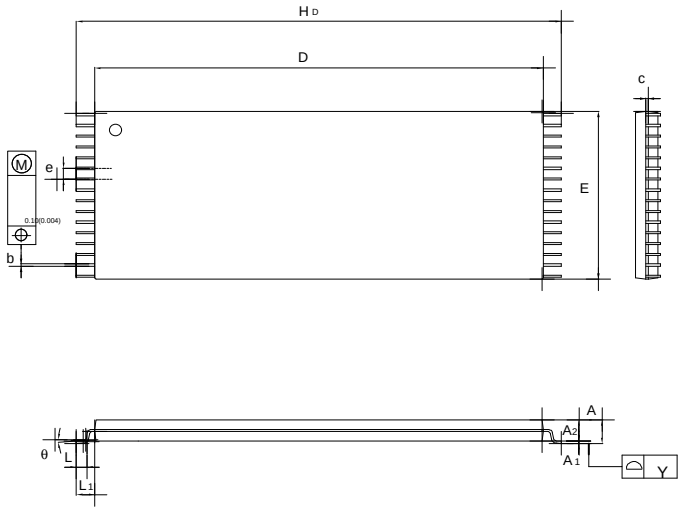


Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.140	—	—	3.56
A_1	0.020	—	—	0.50	—	—
A_2	0.105	0.110	0.115	2.67	2.80	2.93
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.35
D	0.547	0.550	0.553	13.89	13.97	14.05
E	0.447	0.450	0.453	11.35	11.43	11.51
e	0.044	0.050	0.056	1.12	1.27	1.42
G_D	0.490	0.510	0.530	12.45	12.95	13.46
G_E	0.390	0.410	0.430	9.91	10.41	10.92
H_D	0.585	0.590	0.595	14.86	14.99	15.11
H_E	0.485	0.490	0.495	12.32	12.45	12.57
L	0.075	0.090	0.095	1.91	2.29	2.41
y	—	—	0.004	—	—	0.10
θ	0°	—	10°	0°	—	10°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches.
4. General appearance spec. should be based on final visual inspection sepc.

32-pin TSOP



Symbol	Dimension in Inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.047	—	—	1.20
A_1	0.002	—	0.006	0.05	—	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.007	0.008	0.009	0.17	0.20	0.23
c	0.005	0.006	0.007	0.12	0.15	0.17
D	0.720	0.724	0.728	18.30	18.40	18.50
E	0.311	0.315	0.319	7.90	8.00	8.10
H_D	0.780	0.787	0.795	19.80	20.00	20.20
e	—	0.020	—	—	0.50	—
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	—	0.031	—	—	0.80	—
Y	0.000	—	0.004	0.00	—	0.10
θ	1	3	5	1	3	5

Note:

Controlling dimension: Millimeters

VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Apr. 1997		Initial Issued
A2	Nov. 1997	4, 8	Correct the address from 3FFF2 to 7FFF2
		9	Correct the boot block from 8K to 16K
		15	Modify page write cycle timing diagram waveform
		1, 18	Delete cycling 100K item
A3	Feb. 1998	6	Add. pause 10 mS
		7	Add. pause 50 mS
		8	Correct the time from 10 mS to 10 µS
		1, 18	Add. cycling 100 item

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
http://www.winbond.com.tw/
Voice & Fax-on-demand: 886-2-27197006

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.
Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.
2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798