STK11C88-3
32K x 8 nvSRAM
3.3V *QuantumTrap*™ CMOS
Nonvolatile Static RAM

ADVANCE

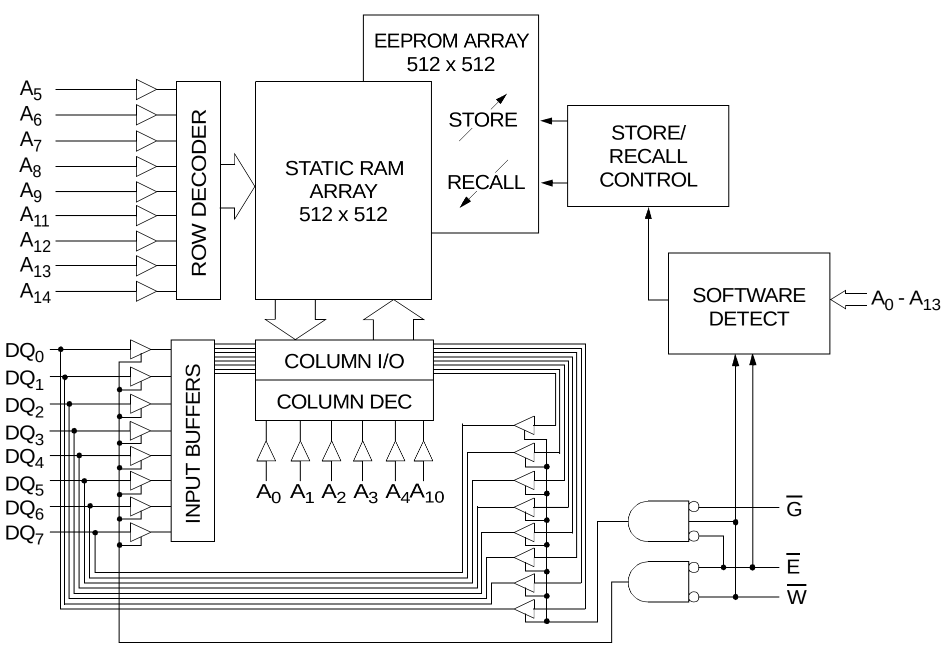
FEATURES

- **Operating V_{CC} Range: 3.0V-3.6V**
- **45ns and 55ns Access Times**
- ***STORE* to EEPROM Initiated by Software**
- ***RECALL* to SRAM Initiated by Software or Power Restore**
- **8mA Typical I_{cc} at 200ns Cycle Time**
- **Unlimited READ, WRITE and *RECALL* Cycles**
- **1,000,000 *STORE* Cycles to EEPROM**
- **100-Year Data Retention in EEPROM**
- **Commercial and Industrial Temperatures**
- **28-Pin DIP and SOIC Packages**

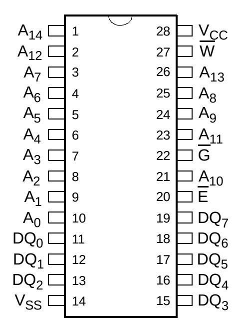
DESCRIPTION

The Simtek STK11C88-3 is a fast static RAM with a nonvolatile, electrically erasable PROM element incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM. Data transfers from the SRAM to the EEPROM (the *STORE* operation), or from EEPROM to SRAM (the *RECALL* operation) take place using a software sequence. Transfers from the EEPROM to the SRAM (the *RECALL* operation) also take place automatically on restoration of power.

BLOCK DIAGRAM



PIN CONFIGURATIONS



28 - 300 PDIP
28 - 600 PDIP
28 - 300 SOIC
28 - 350 SOIC

PIN NAMES

A_0 - A_{14}	Address Inputs
$\overline{W}$	Write Enable
DQ_0 - DQ_7	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
V_{CC}	Power (+ 3.3V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS[a]

Voltage on Input Relative to V_{SS} . . . . –0.6V to (V_{CC} + 0.5V)
Voltage on DQ_{0-7} . . . . –0.5V to (V_{CC} + 0.5V)
Temperature under Bias . . . . –55°C to 125°C
Storage Temperature . . . . –65°C to 150°C
Power Dissipation 1W
DC Output Current (1 output at a time, 1s duration) 15mA

Note a: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (V_{CC} = 3.0V-3.6V)

SYMBOL	PARAMETER	COMMERCIAL		INDUSTRIAL		UNITS	NOTES
		MIN	MAX	MIN	MAX		
I_{CC_1}[b]	Average V_{CC} Current		35 30		37 32	mA mA	t_{AVAV} = 45ns t_{AVAV} = 55ns
I_{CC_2}[c]	Average V_{CC} Current During *STORE*		3		3	mA	All Inputs Don’t Care, V_{CC} = max
I_{CC_3}[b]	Average V_{CC} Current at t_{AVAV} = 200ns 3.3V, 25°C, Typical		8		8	mA	$\overline{W}$ ≥ (V_{CC} – 0.2V) All Others Cycling, CMOS Levels
I_{SB_1}[d]	Average V_{CC} Current (Standby, Cycling TTL Input Levels)		9 8		10 9	mA mA	t_{AVAV} = 45ns, $\overline{E}$ ≥ V_{IH} t_{AVAV} = 55ns, $\overline{E}$ ≥ V_{IH}
I_{SB_2}[d]	V_{CC} Standby Current (Standby, Stable CMOS Input Levels)		1		1	mA	$\overline{E}$ ≥ (V_{CC} - 0.2V) All Others V_{IN} ≤ 0.2V or ≥ (V_{CC} – 0.2V)
I_{ILK}	Input Leakage Current		±1		±1	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}
I_{OLK}	Off-State Output Leakage Current		±5		±5	μA	V_{CC} = max V_{IN} = V_{SS} to V_{CC}, $\overline{E}$ or $\overline{G}$ ≥ V_{IH}
V_{IH}	Input Logic “1” Voltage	2.2	V_{CC} + .5	2.2	V_{CC} + .5	V	All Inputs
V_{IL}	Input Logic “0” Voltage	V_{SS} – .5	0.8	V_{SS} – .5	0.8	V	All Inputs
V_{OH}	Output Logic “1” Voltage	2.4		2.4		V	I_{OUT} = – 1mA
V_{OL}	Output Logic “0” Voltage		0.4		0.4	V	I_{OUT} = 2mA
T_A	Operating Temperature	0	70	–40	85	°C	

Note b: I_{CC_1} and I_{CC_3} are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: I_{CC_2} is the average current required for the duration of the *STORE* cycle (t_{STORE}).
Note d: $\overline{E}$ ≥ V_{IH} will not produce standby current levels until any nonvolatile cycle in progress has timed out.

AC TEST CONDITIONS

Input Pulse Levels . . . . 0V to 3.0V
Input Rise and Fall Times . . . . ≤ 5ns
Input and Output Timing Reference Levels 1.5V
Output Load . . . . See Figure 1

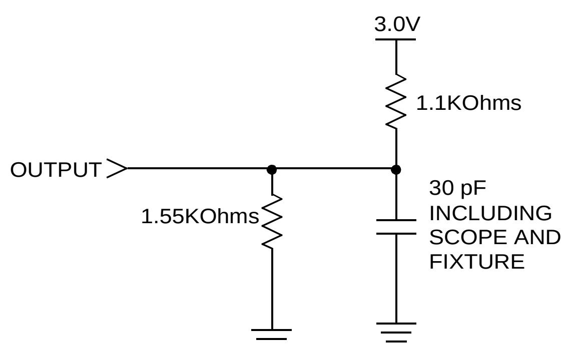


Figure 1: AC Output Loading

CAPACITANCE[e] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV = 0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV = 0 to 3V

Note e: These parameters are guaranteed but not tested.

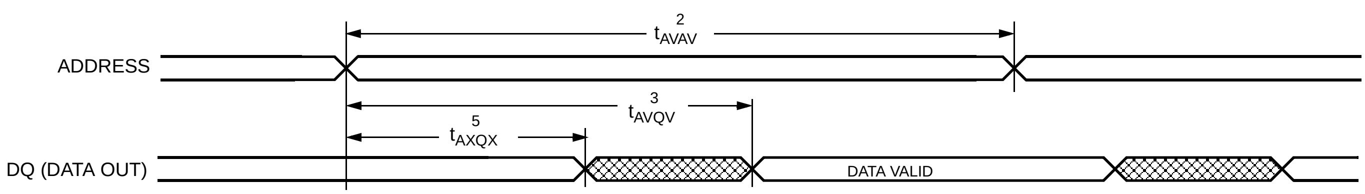
SRAM READ CYCLES #1 & #2

(V_{CC} = 3.0V-3.6V)

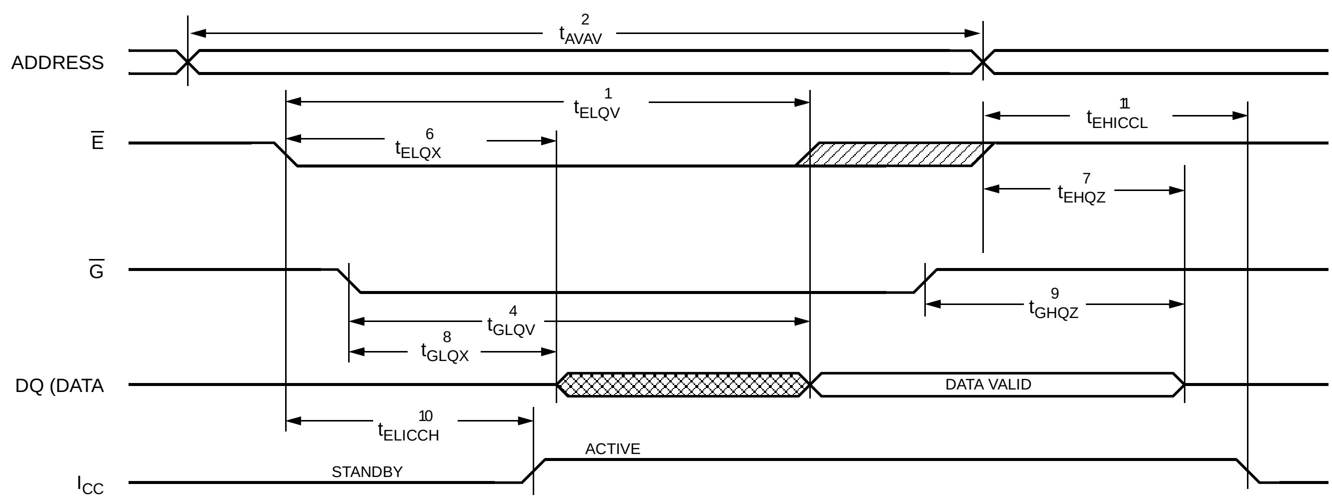
NO.	SYMBOLS #1, #2	SYMBOLS Alt.	PARAMETER	STK11C88-3-45 MIN	STK11C88-3-45 MAX	STK11C88-3-55 MIN	STK11C88-3-55 MAX	UNITS
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55	ns
2	t_{AVAV}[f]	t_{RC}	Read Cycle Time	45		55		ns
3	t_{AVQV}[g]	t_{AA}	Address Access Time		45		55	ns
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		20		25	ns
5	t_{AXQX}[g]	t_{OH}	Output Hold after Address Change	5		3		ns
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		ns
7	t_{EHQZ}[h]	t_{HZ}	Chip Disable to Output Inactive		15		20	ns
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		ns
9	t_{GHQZ}[h]	t_{OHZ}	Output Disable to Output Inactive		15		20	ns
10	t_{ELICCH}[e]	t_{PA}	Chip Enable to Power Active	0		0		ns
11	t_{EHICCL}[d, e]	t_{PS}	Chip Disable to Power Standby		45		55	ns

Note f: $\overline{W}$ must be high during SRAM READ cycles and low during SRAM WRITE cycles.
Note g: I/O state assumes $\overline{E}$ and $\overline{G}$ < V_{IL} and $\overline{W}$ > V_{IH}; device is continuously selected.
Note h: Measured ± 200mV from steady state output voltage.

SRAM READ CYCLE #1: Address Controlled[f, g]



SRAM READ CYCLE #2: $\overline{E}$ Controlled[f]



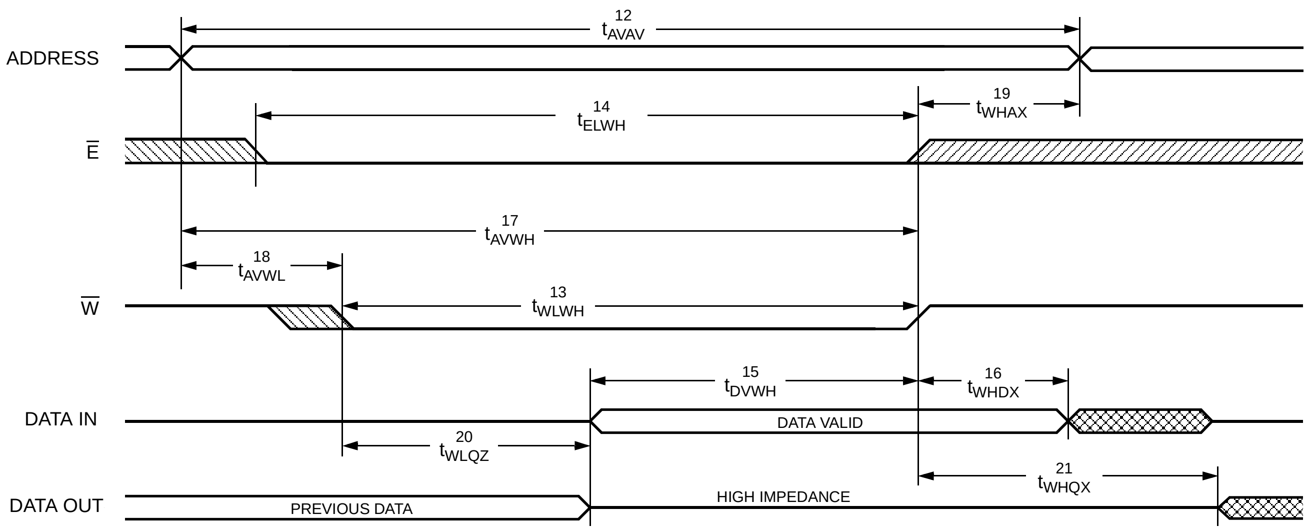
SRAM WRITE CYCLES #1 & #2

(V_{CC} = 3.0V-3.6V)

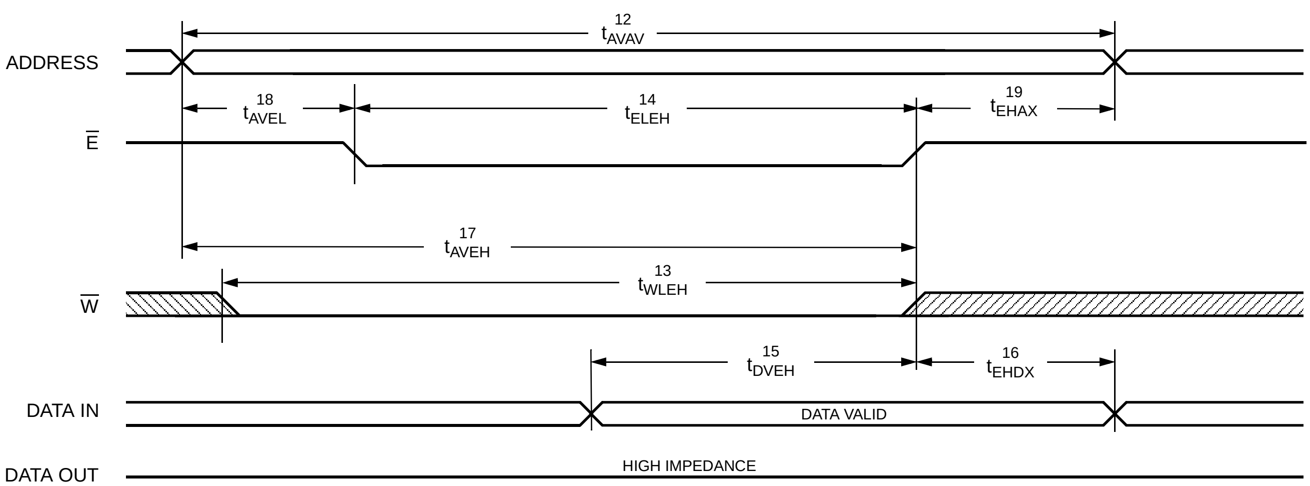
NO.	SYMBOLS			PARAMETER	STK11C88-3-45		STK11C88-3-55		UNITS
	#1	#2	Alt.		MIN	MAX	MIN	MAX	
12	t_{AVAV}	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		ns
13	t_{WLWH}	t_{WLEH}	t_{WP}	Write Pulse Width	30		40		ns
14	t_{ELWH}	t_{ELEH}	t_{CW}	Chip Enable to End of Write	30		40		ns
15	t_{DVWH}	t_{DVEH}	t_{DW}	Data Set-up to End of Write	15		25		ns
16	t_{WHDX}	t_{EHDX}	t_{DH}	Data Hold after End of Write	0		0		ns
17	t_{AVWH}	t_{AVEH}	t_{AW}	Address Set-up to End of Write	30		40		ns
18	t_{AVWL}	t_{AVEL}	t_{AS}	Address Set-up to Start of Write	0		0		ns
19	t_{WHAX}	t_{EHAX}	t_{WR}	Address Hold after End of Write	0		0		ns
20	t_{WLQZ}[h, i]		t_{WZ}	Write Enable to Output Disable		15		20	ns
21	t_{WHQX}		t_{OW}	Output Active after End of Write	5		5		ns

Note i: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high-impedance state.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥ V_{IH} during address transitions.

SRAM WRITE CYCLE #1: $\overline{W}$ Controlled[j]



SRAM WRITE CYCLE #2: $\overline{E}$ Controlled[j]

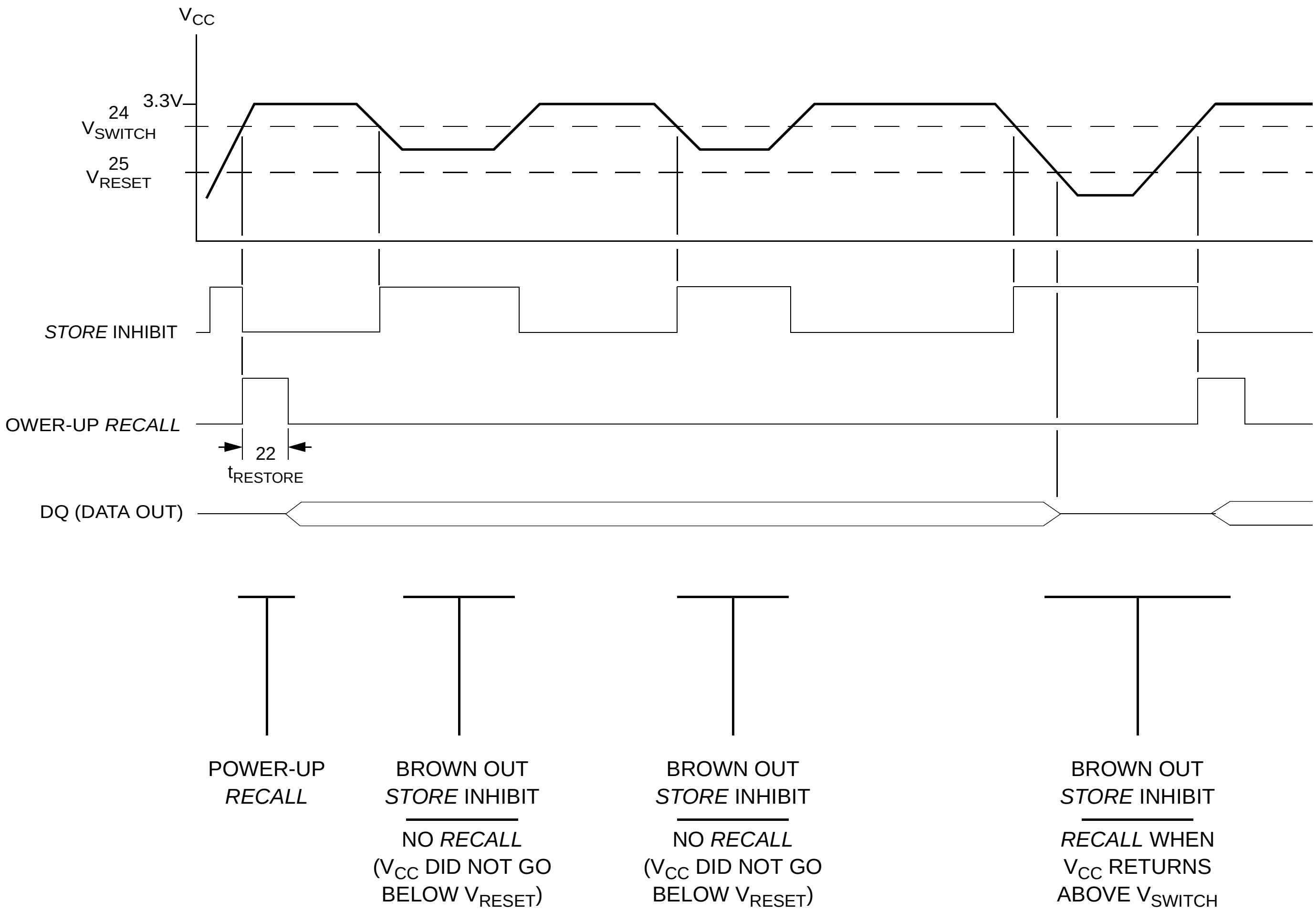


STORE INHIBIT/POWER-UP *RECALL* (V_{CC} = 3.0V-3.6V)

NO.	SYMBOLS Standard	PARAMETER	STK11C88-3 MIN	STK11C88-3 MAX	UNITS	NOTES
22	$t_{RESTORE}$	Power-up *RECALL* Duration		550	μs	k
23	t_{STORE}	*STORE* Cycle Duration		10	ms	
24	V_{SWITCH}	Low Voltage Trigger Level	2.7	3.0	V	
25	V_{RESET}	Low Voltage Reset Level		2.6	V	

Note k: $t_{RESTORE}$ starts from the time V_{CC} rises above V_{SWITCH}.

STORE INHIBIT/POWER-UP *RECALL*



SOFTWARE *STORE/RECALL* MODE SELECTION

$\overline{E}$	$\overline{W}$	A_{13} - A_0 (hex)	MODE	I/O	NOTES
L	H	0E38 31C7 03E0 3C1F 303F 0FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *STORE*	Output Data Output Data Output Data Output Data Output Data Output High Z	l, m
L	H	0E38 31C7 03E0 3C1F 303F 0C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile *RECALL*	Output Data Output Data Output Data Output Data Output Data Output High Z	l, m

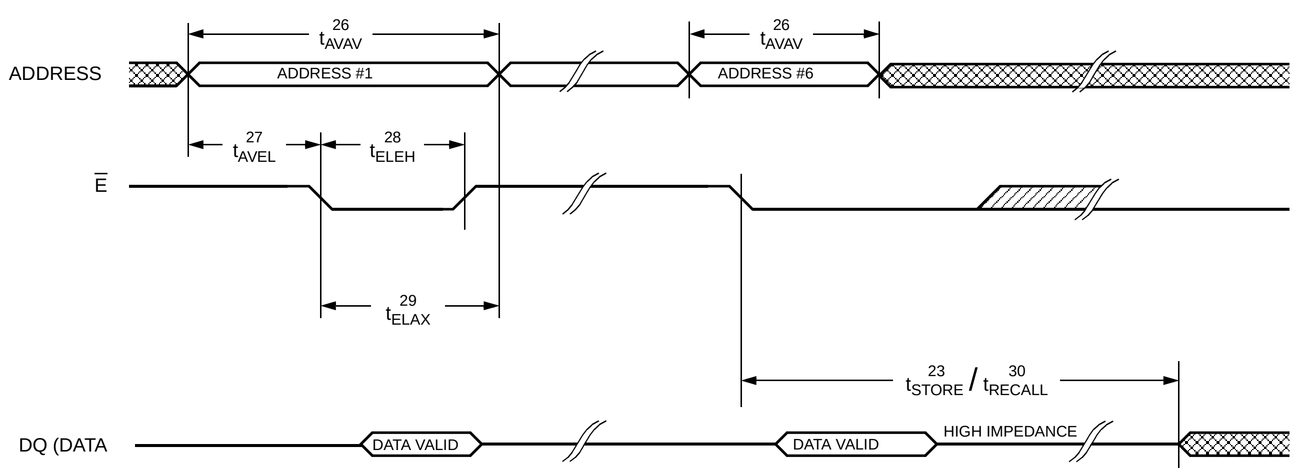
Note l: The six consecutive addresses must be in order listed. $\overline{W}$ must be high during all six consecutive cycles to enable a nonvolatile cycle.
Note m: While there are 15 addresses on the STK11C88-3, only the lower 14 are used to control software modes.

SOFTWARE *STORE/RECALL* CYCLE$^{n, o}$ (V_{CC} = 3.0V-3.6V)

NO.	SYMBOLS	PARAMETER	STK11C88-3-45		STK11C88-3-55		UNITS
			MIN	MAX	MIN	MAX	
26	t_{AVAV}	*STORE*/*RECALL* Initiation Cycle Time	45		55		ns
27	$t_{AVEL}{}^{n}$	Address Set-up Time	0		0		ns
28	$t_{ELEH}{}^{n}$	Clock Pulse Width	30		45		ns
29	$t_{ELAX}{}^{n}$	Address Hold Time	20		45		ns
30	$t_{RECALL}{}^{n}$	*RECALL* Duration		20		20	μs

Note n: The software sequence is clocked with $\overline{E}$ controlled READs.
Note o: The six consecutive addresses must be in the order listed in the Software *STORE/RECALL* Mode Selection Table: (0E38, 31C7, 03E0, 3C1F, 303F, 0FC0) for a *STORE* cycle or (0E38, 31C7, 03E0, 3C1F, 303F, 0C63) for a *RECALL* cycle. $\overline{W}$ must be high during all six consecutive cycles.

SOFTWARE *STORE/RECALL* CYCLE: $\overline{E}$ Controlled^{o}



DEVICE OPERATION

The STK11C88-3 is a versatile 3.3V V_{CC} memory chip that provides several modes of operation. The STK11C88-3 can operate as a standard 32K x 8 SRAM. It has a 32K x 8 EEPROM shadow to which the SRAM information can be copied or from which the SRAM can be updated in nonvolatile mode.

NOISE CONSIDERATIONS

Note that the STK11C88-3 is a high-speed memory and so must have a high frequency bypass capacitor of approximately 0.1µF connected between V_{CC} and V_{SS}, using leads and traces that are as short as possible. As with all high-speed CMOS ICs, normal careful routing of power, ground and signals will help prevent noise problems.

SRAM READ

The STK11C88-3 performs a READ cycle whenever $\overline{E}$ and $\overline{G}$ are low and $\overline{W}$ is high. The address specified on pins A_{0-14} determines which of the 32,768 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t_{AVQV} (READ cycle #1). If the READ is initiated by $\overline{E}$ or $\overline{G}$, the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t_{AVQV} access time without the need for transitions on any control input pins, and will remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought high.

SRAM WRITE

A WRITE cycle is performed whenever $\overline{E}$ and $\overline{W}$ are low. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ goes high at the end of the cycle. The data on the common I/O pins DQ_{0-7} will be written into the memory if it is valid t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE.

It is recommended that $\overline{G}$ be kept high during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If $\overline{G}$ is left low, internal circuitry will turn off the output buffers t_{WLQZ} after $\overline{W}$ goes low.

SOFTWARE NONVOLATILE *STORE*

The STK11C88-3 software *STORE* cycle is initiated by executing sequential READ cycles from six specific address locations. During the *STORE* cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. The program operation copies the SRAM data into nonvolatile memory. Once a *STORE* cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of reads from specific addresses is used for *STORE* initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no *STORE* or *RECALL* will take place.

To initiate the software *STORE* cycle, the following READ sequence must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0FC0 (hex)	Initiate *STORE* cycle

The software sequence is clocked with $\overline{E}$ controlled READs.

Once the sixth address in the sequence has been entered, the *STORE* cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that $\overline{G}$ be low for the sequence to be valid. After the t_{STORE} cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

SOFTWARE NONVOLATILE *RECALL*

A software *RECALL* cycle is initiated with a sequence of READ operations in a manner similar to the software *STORE* initiation. To initiate the *RECALL* cycle, the following sequence of READ operations must be performed:

1.	Read address	0E38 (hex)	Valid READ
2.	Read address	31C7 (hex)	Valid READ
3.	Read address	03E0 (hex)	Valid READ
4.	Read address	3C1F (hex)	Valid READ
5.	Read address	303F (hex)	Valid READ
6.	Read address	0C63 (hex)	Initiate *RECALL* cycle

Internally, *RECALL* is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time the SRAM will once again be ready for READ and WRITE operations. The *RECALL* operation in no way alters the data in the EEPROM cells. The nonvolatile data can be recalled an unlimited number of times.

POWER-UP *RECALL*

During power up, or after any low-power condition ($V_{CC} < V_{RESET}$), an internal *RECALL* request will be latched. When V_{CC} once again exceeds the sense voltage of V_{SWITCH}, a *RECALL* cycle will automatically be initiated and will take $t_{RESTORE}$ to complete.

If the STK11C88-3 is in a WRITE state at the end of power-up *RECALL*, the SRAM data will be corrupted. To help avoid this situation, a 10K Ohm resistor should be connected either between $\overline{W}$ and system V_{CC} or between $\overline{E}$ and system V_{CC}.

HARDWARE PROTECT

The STK11C88-3 offers hardware protection against inadvertent *STORE* operation during low-voltage conditions. When $V_{CC} < V_{SWITCH}$, all software *STORE* operations are inhibited.

LOW AVERAGE ACTIVE POWER

The STK11C88-3 draws significantly less current when it is cycled at times longer than 55ns. Figure 2 shows the relationship between I_{CC} and READ cycle time. Worst-case current consumption is shown for both CMOS and TTL input levels (commercial temperature range, V_{CC} = 3.6V, 100% duty cycle on chip enable). Figure 3 shows the same relationship for WRITE cycles.If the chip enable duty cycle is less than 100%, only standby current is drawn when the chip is disabled. The overall average current drawn by the STK11C88-3 depends on the following items: 1) CMOS vs. TTL input levels; 2) the duty cycle of chip enable; 3) the overall cycle rate for accesses; 4) the ratio of READs to WRITEs; 5) the operating temperature; 6) the V_{CC} level; and 7) I/O loading.

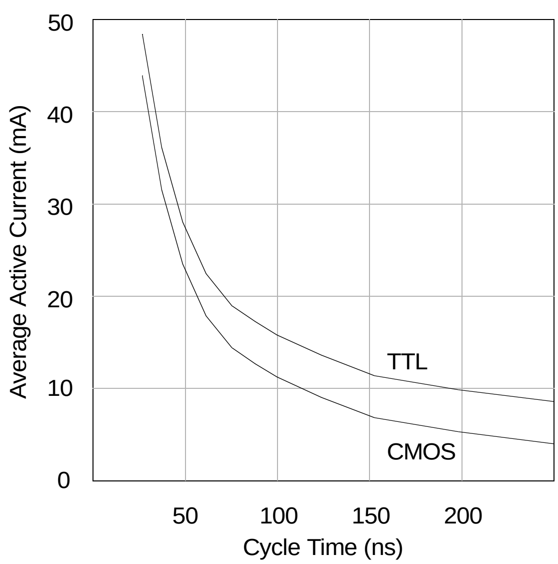


Figure 2: I_{CC} (max) Reads

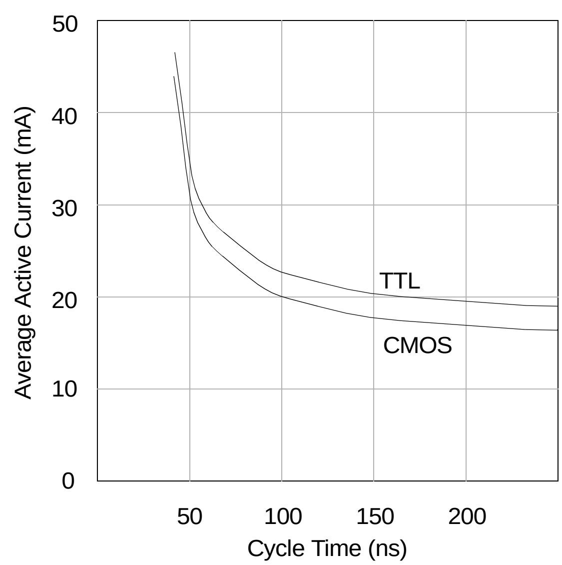


Figure 3: I_{CC} (max) Writes

ORDERING INFORMATION

STK11C88-3 W 45 I

Temperature Range

Blank = Commercial (0 to 70°C)

I = Industrial (–40 to 85°C)

Access Time

45 = 45ns

55 = 55ns

Package

W = Plastic 28-pin 600 mil DIP

P = Plastic 28-pin 300 mil DIP

N = Plastic 28-pin 350 mil SOIC

S = Plastic 28-pin 300 mil SOIC