M28W320FSU
M28W640FSU

32Mbit (2Mb x16) and 64Mbit (4Mb x16) 3V Supply, Uniform Block, Secure Flash Memories

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 2.7V to 3.6V Core Power Supply
  - V_{DDQ}= 2.7V to 3.6V for Input/Output
  - V_{PP} = 12V for fast Program (optional)
- ACCESS TIME: 70ns
- PROGRAMMING TIME:
  - 10µs typical
  - Double Word Programming Option
  - Quadruple Word Programming Option
- COMMON FLASH INTERFACE
- UNIFORM BLOCKS
- 64-KWord UNIFORM MEMORY BLOCKS
  - M28W320FSU: 32 Blocks
  - M28W640FSU: 64 Blocks
- HARDWARE PROTECTION
  - V_{PP} Pin for Write protect of All Blocks
- SECURITY FEATURES
  - 128 bit User-programmable OTP segment
  - 64 bit Unique Device Identifier
  - KRYPTO Features:
    Modify Protection,
    Read Protection,
    Device Authentication
- AUTOMATIC STAND-BY MODE
- PROGRAM and ERASE SUSPEND
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Codes:
    M28W320FSU: 880Ch,
    M28W640FSU: 8857h
- PACKAGE
  - Compliant with Lead-Free Soldering Processes
  - Lead-Free Version

Figure 1. Package

TBGA64 (ZA)
10 x 13mm

TABLE OF CONTENTS

FEATURES SUMMARY 1
Figure 1. Package 1
SUMMARY DESCRIPTION 5
Figure 2. M28W320FSU Logic Diagram 6
Figure 3. M28W640FSU Logic Diagram 6
Table 1. Signal Names 6
Figure 4. TBGA Connections (Top view through package) 7
Figure 5. M28W320FSU and M28W640FSU Block Addresses 8
Figure 6. Protection Register Memory Map 8
SIGNAL DESCRIPTIONS 9
Address Inputs 9
Data Input/Output (DQ0-DQ15) 9
Chip Enable ($\overline{E}$) 9
Output Enable ($\overline{G}$) 9
Write Enable ($\overline{W}$) 9
Reset ($\overline{RP}$) 9
V_{DD} Supply Voltage 9
V_{DDQ} Supply Voltage 9
V_{PP} Program Supply Voltage 9
V_{SS} Ground 9
BUS OPERATIONS 10
Read 10
Write 10
Output Disable 10
Standby 10
Automatic Standby 10
Reset 10
Table 2. Bus Operations 10
HARDWARE PROTECTION 11
$V_{PP} \leq V_{PPLK}$ 11
SECURITY FEATURES 11
COMMAND INTERFACE 12
Read Memory Array Command 12
Read Status Register Command 12
Read Electronic Signature Command 12
Table 3. Command Codes 12
Read CFI Query Command 12

Block Erase Command . . . 12
Program Command . . . 13
Double Word Program Command . . . 13
Quadruple Word Program Command . . . 13
Clear Status Register Command . . . 13
Program/Erase Suspend Command . . . 13
Program/Erase Resume Command . . . 14
Protection Register Program Command . . . 14
Table 4. Commands . . . 15
Table 5. Read Electronic Signature . . . 15
Table 6. Read Protection Register and Protection Register Lock . . . 16
Table 7. Program, Erase Times and Program/Erase Endurance Cycles . . . *17*

STATUS REGISTER . . . 18
Program/Erase Controller Status (Bit 7) . . . 18
Erase Suspend Status (Bit 6) . . . 18
Erase Status (Bit 5) . . . 18
Program Status (Bit 4) . . . 18
V_{PP} Status (Bit 3) . . . 18
Program Suspend Status (Bit 2) . . . 18
Block Protection Status (Bit 1) . . . 19
Reserved (Bit 0) . . . 19
Table 8. Status Register Bits . . . 19

MAXIMUM RATING . . . 20
Table 9. Absolute Maximum Ratings . . . 20

DC and AC PARAMETERS . . . 21
Table 10. Operating and AC Measurement Conditions . . . 21
Figure 7. AC Measurement I/O Waveform . . . 21
Figure 8. AC Measurement Load Circuit . . . 21
Table 11. Capacitance . . . 21
Table 12. DC Characteristics . . . 22
Figure 9. Read AC Waveforms . . . 23
Table 13. Read AC Characteristics . . . 23
Figure 10.Write AC Waveforms, Write Enable Controlled . . . 24
Table 14. Write AC Characteristics, Write Enable Controlled . . . 25
Figure 11.Write AC Waveforms, Chip Enable Controlled . . . 26
Table 15. Write AC Characteristics, Chip Enable Controlled . . . 27
Figure 12.Power-Up and Reset AC Waveforms . . . 28
Table 16. Power-Up and Reset AC Characteristics . . . 28

PACKAGE MECHANICAL . . . 29
Figure 13.TBGA64 - 10x13 active ball array, 1mm pitch, Bottom View Package Outline . . . 29
Table 17. TBGA64 - 10x13 active ball array, 1mm pitch, Package Mechanical Data . . . 29

PART NUMBERING 30

Table 18. Ordering Information Scheme 30
Table 19. Daisy Chain Ordering Scheme 31

APPENDIX A.BLOCK ADDRESS TABLES 32

Table 20. Block Addresses, M28W320FSU 32
Table 21. Block Addresses, M28W640FSU 33

APPENDIX B.COMMON FLASH INTERFACE (CFI) 34

Table 22. Query Structure Overview 34
Table 23. CFI Query Identification String. 34
Table 24. CFI Query System Interface Information 35
Table 25. Device Geometry Definition 36
Table 26. Primary Algorithm-Specific Extended Query Table 37
Table 27. Security Code Area 38

APPENDIX C.FLOWCHARTS AND PSEUDO CODES 39

Figure 14.Program Flowchart and Pseudo Code 39
Figure 15.Double Word Program Flowchart and Pseudo Code 40
Figure 16.Quadruple Word Program Flowchart and Pseudo Code 41
Figure 17.Program Suspend & Resume Flowchart and Pseudo Code 42
Figure 18.Erase Flowchart and Pseudo Code. 43
Figure 19.Erase Suspend & Resume Flowchart and Pseudo Code 44
Figure 20.Protection Register Program Flowchart and Pseudo Code. 45

APPENDIX D.COMMAND INTERFACE AND PROGRAM/ERASE CONTROLLER STATE. 46

Table 28. Write State Machine Current/Next, sheet 1 of 2. 46
Table 29. Write State Machine Current/Next, sheet 2 of 2. 47

REVISION HISTORY 48

Table 30. Document Revision History 48

SUMMARY DESCRIPTION

The M28W320FSU and the M28W640FSU are 32 Mbit (2Mbit x 16) and 64 Mbit (4Mbit x 16) Secure Flash memories. The devices can be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 2.7V to 3.6V V_{DD} supply for the circuitry and a 2.7V to 3.6V V_{DDQ} supply for the Input/Output pins. An optional 12V V_{PP} power supply is provided to speed up customer programming.

The M28W320FSU and M28W640FSU feature 32 Mbits and 64 Mbits respectively and are divided into thirty-two and sixty-four 64-KWord Uniform blocks, respectively. Refer to Figure 5. for a detailed description of the devices memory architecture and map.

All devices are equipped with hardware and software block protection features to avoid unwanted program/erase (modify) or read of the Flash memory content:

- Hardware Protection:
  - When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase.
- Software Protection thanks to KRYPTO Security Features:
  - Modify Protection: volatile and non-volatile.
  - Read Protection.

The KRYPTO Security features are described in a dedicated Application Note. Please contact STMicroelectronics for further details.

Two registers are available for protection purpose:

- The Protection Register
- The KRYPTO Protection Register.

The Protection Register is a 192 bit Protection Register to increase the protection of a system design. The Protection Register is divided into a 64 bit segment and a 128 bit segment. The 64 bit segment contains a unique device number written by ST, while the second one is one-time-programmable by the user. The user programmable segment can be permanently protected. Figure 6., shows the Protection Register Memory Map.

The KRYPTO Protection Register is used to manage the Modify and Read protection modes. It also features a Device Authentication mechanism. The KRYPTO Protection Register is described in a dedicated Application Note. Please contact STMicroelectronics for further details.

Each block can be erased separately. Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

All the devices are offered in a TBGA64 (10 x 13mm) package. In addition to the standard version, the package is also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECOPACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive. The package is compliant with Lead-free soldering processes.

All devices are supplied with all the bits erased (set to '1').

Figure 2. M28W320FSU Logic Diagram

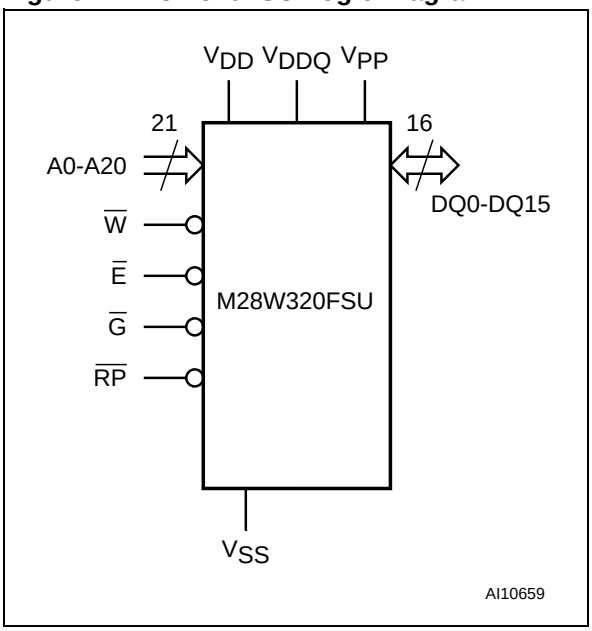


Figure 3. M28W640FSU Logic Diagram

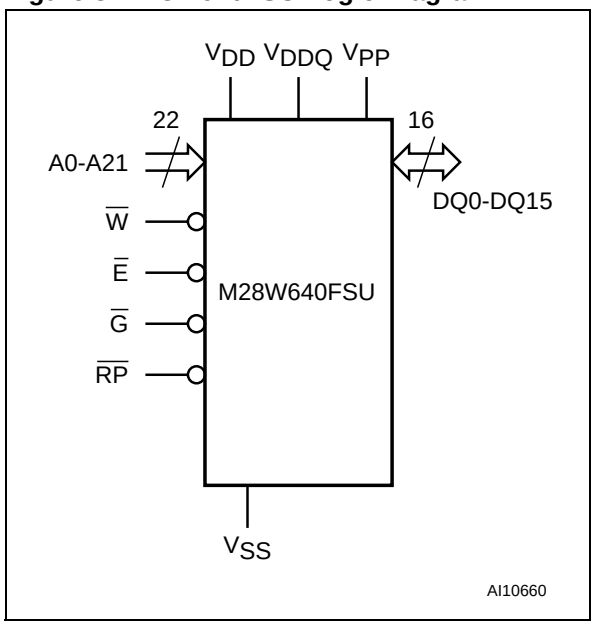
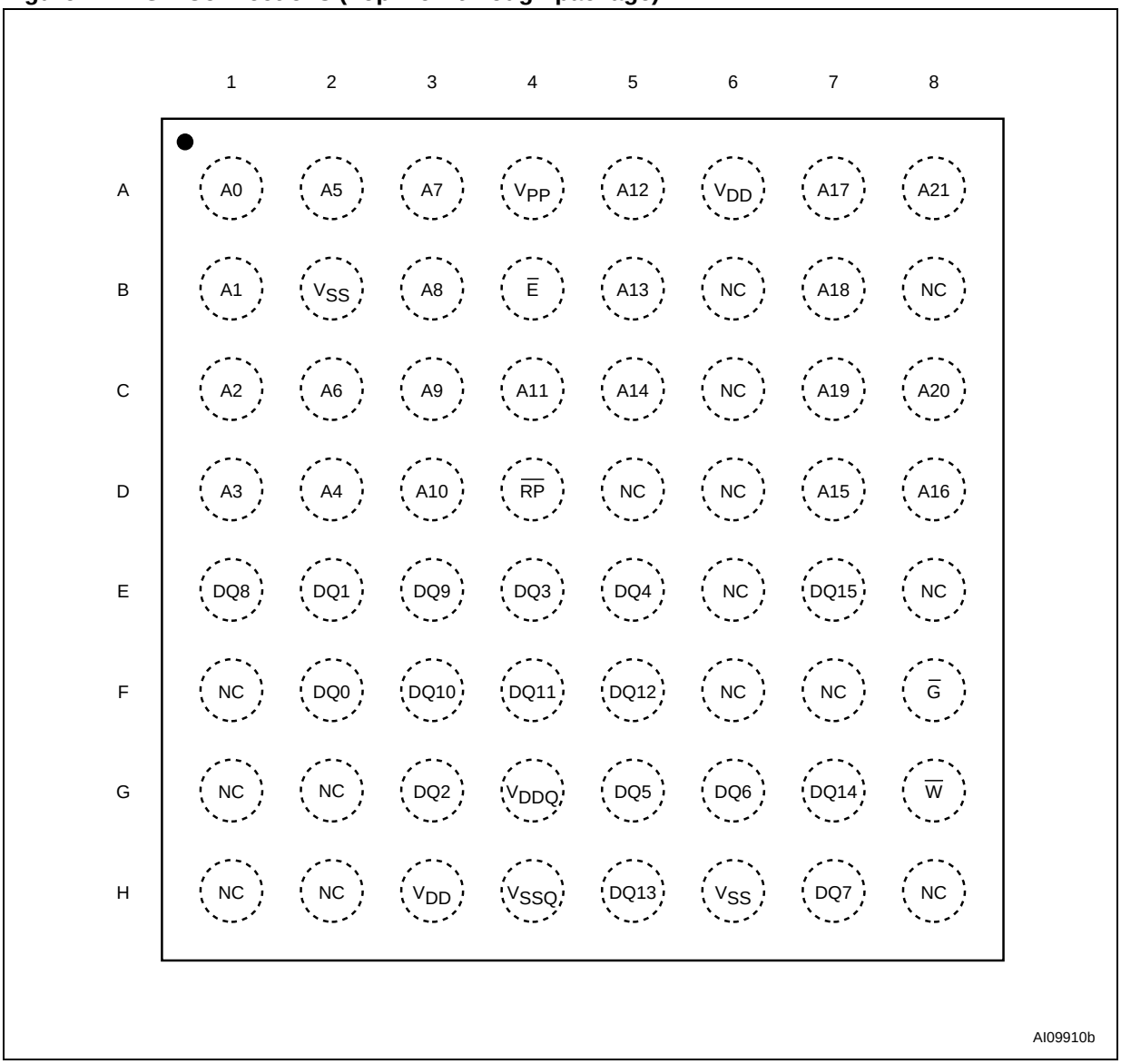


Table 1. Signal Names

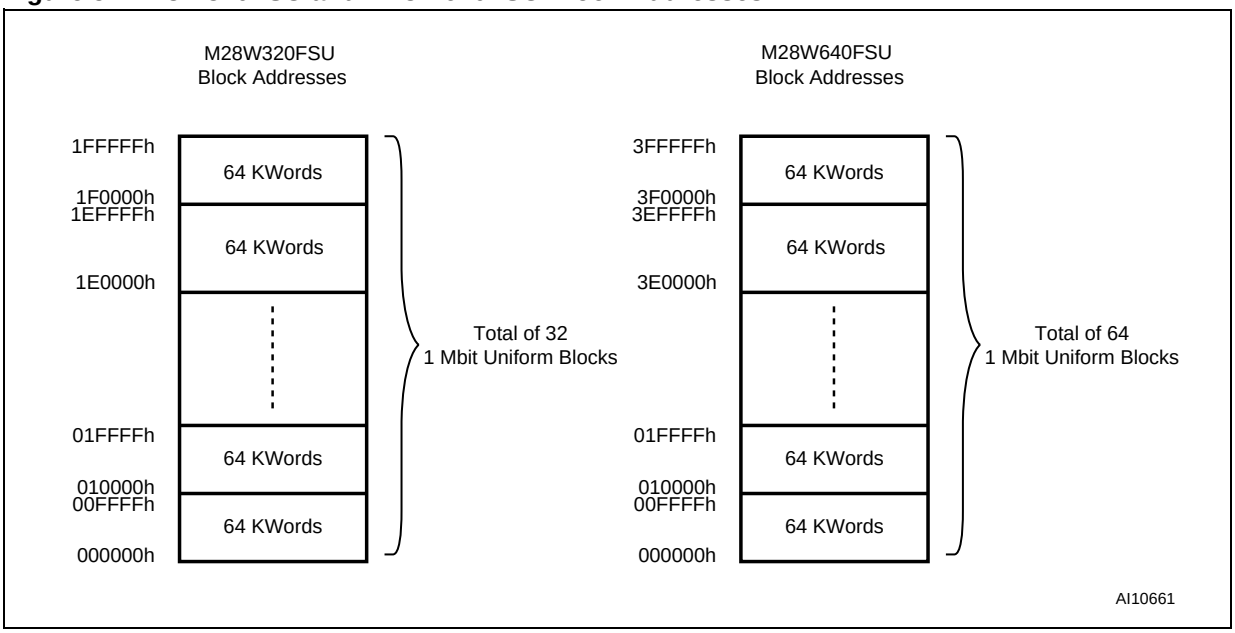
M28W320FSU	M28W640FSU	Signal Names
A0-A20	A0-A21	Address Inputs
DQ0-DQ15		Data Input/Output
$\overline{E}$		Chip Enable
$\overline{G}$		Output Enable
$\overline{W}$		Write Enable
$\overline{RP}$		Reset
V_{DD}		Core Power Supply
V_{DDQ}		Power Supply for Input/Output
V_{PP}		Optional Supply Voltage for Fast Program & Erase
V_{SS}		Ground
NC		Not Connected Internally

Figure 4. TBGA Connections (Top view through package)



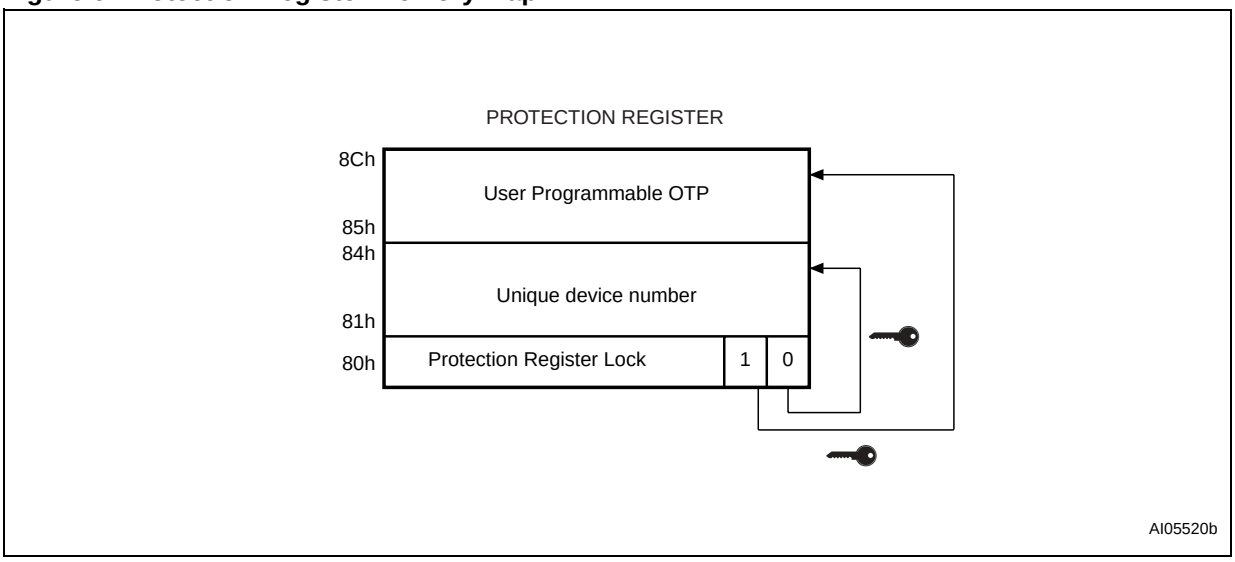
Note: 1. The above figure gives the TBGA connections for M28W640FSU. On M28W320FSU, A21 is NC.

Figure 5. M28W320FSU and M28W640FSU Block Addresses



Note: 1. Also see APPENDIX A., Tables 21 and 20 for a full listing of the Block Addresses.

Figure 6. Protection Register Memory Map



SIGNAL DESCRIPTIONS

See Figures 2 and 3, Logic Diagrams and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs. The Address Inputs select the cells in the memory array to access during Bus Read operations. Address Inputs range from A0 to A20 for the M28W320FSU. The M28W640FSU has an additional A21 address line. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Input/Output (DQ0-DQ15). The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Write Bus operation.

Chip Enable ($\overline{E}$). The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

Output Enable ($\overline{G}$). The Output Enable controls data outputs during the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable, E, or Write Enable, W, whichever occurs first.

Reset ($\overline{RP}$). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is minimized. After Reset all blocks are in the Locked state. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters read array mode, but a negative transition of Chip Enable or a change of the address is required to ensure valid data outputs.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

V_{PP} Program Supply Voltage. V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. The Supply Voltage V_{DD} and the Program Supply Voltage V_{PP} can be applied in any order.

If V_{PP} is kept in a low voltage range (0V to 3.6V) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions (see Table 12., DC Characteristics, for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect on Program or Erase.

If V_{PP} is set to V_{PPH}, it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed (see Table 14. and Table 15.). A Quadruple Word Program command will be ignored if V_{PP} is not set to V_{PPH} while a Double Word Program can be performed even if V_{PP} is set to V_{DD}.

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1µF capacitor close to the pin. See Figure 8., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby, Automatic Standby and Reset. See Table 2., Bus Operations, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Read. Read Bus operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at V_{IL} in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See Figure 9., Read AC Waveforms, and Table 13., Read AC Characteristics, for details of when the output becomes valid.

Read mode is the default state of the device when exiting Reset or after power-up.

Write. Bus Write operations write Commands to the memory or latch Input Data to be programmed. A write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

See Figure 10. and Figure 11., Write AC Waveforms, and Table 14. and Table 15., Write AC Characteristics, for details of the timing requirements.

Output Disable. The data outputs are high impedance when the Output Enable is at V_{IH}.

Standby. Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable is at V_{IH} and the device is in read mode. The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Automatic Standby. Automatic Standby provides a low power consumption state during Read mode. Following a read operation, the device enters Automatic Standby after 150ns of bus inactivity even if Chip Enable is Low, V_{IL}, and the supply current is reduced to I_{DD1}. The data Inputs/Outputs will still output data if a bus Read operation is in progress.

Reset. During Reset mode when Output Enable is Low, V_{IL}, the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at V_{IL}. The power consumption is reduced to the Standby level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SS} during a Program or Erase, this operation is aborted and the memory content is no longer valid.

Table 2. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	V_{PP}	DQ0-DQ15
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Don't Care	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{DD} or V_{PPH}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	Don't Care	Hi-Z
Standby	V_{IH}	X	X	V_{IH}	Don't Care	Hi-Z
Reset	X	X	X	V_{IL}	Don't Care	Hi-Z

Note: X = V_{IL} or V_{IH}, V_{PPH} = 12V ± 5%.

HARDWARE PROTECTION

All devices feature hardware protection. Refer to SIGNAL DESCRIPTIONS section for a detailed description of these signals.

$V_{PP} \leq V_{PPLK}$. The V_{PP} pin protects all the memory blocks from program and erase operations. Refer to SIGNAL DESCRIPTIONS section for a detailed description of these signals.

SECURITY FEATURES

The M28W320FSU and M28W640FSU are equipped with KRYPTO Security features performing software protection. They allow any block to be protected from program/erase or read operations:

- Modify Protection including Volatile Block Lock/Unlock, Non-Volatile Block Modify Protection, Non-Volatile Password Modify Protection and Irreversible Protection.
- Read Protection.

The KRYPTO features (Modify Protection mode, Read Protection mode and Device Authentication mechanism) are not described in this Datasheet. For further details concerning these additional protection modes please contact ST Sales Offices.

The devices also feature a 64 bit Unique Device Identifier and a 128 bit user-programmable OTP segment (see Figure 6., Protection Register Memory Map and Protection Register Program Command).

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time, to monitor the progress of the operation, or the Program/Erase states. See Table 3., Command Codes, for a summary of the commands and see APPENDIX D., Table 28., Write State Machine Current/Next, sheet 1 of 2., for a summary of the Command Interface.

The Command Interface is reset to Read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands will reset the device to Read mode. Refer to Table 4., Commands, in conjunction with the text descriptions below.

Read Memory Array Command

The Read command returns the memory to its Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Subsequent read operations will read the addressed location and output the data. When a device Reset occurs, the memory defaults to Read mode.

Read Status Register Command

The Status Register indicates when a program or erase operation is complete and the success or failure of the operation itself. Issue a Read Status Register command to read the Status Register's contents. Subsequent Bus Read operations read the Status Register at any address, until another command is issued. See Table 8., Status Register Bits, for details on the definitions of the bits.

The Read Status Register command may be issued at any time, even during a Program/Erase operation. Any Read attempt during a Program/Erase operation will automatically output the content of the Status Register.

Read Electronic Signature Command

The Read Electronic Signature command reads the Manufacturer and Device Codes, and the Protection Register.

The Read Electronic Signature command consists of one write cycle, a subsequent read will output the Manufacturer Code, the Device Code and the Protection Register. See Tables 5, and 6 for the valid address.

Table 3. Command Codes

Hex Code	Command
01h	Block Lock confirm
10h	Program
20h	Erase
30h	Double Word Program
40h	Program
50h	Clear Status Register
56h	Quadruple Word Program
70h	Read Status Register
90h	Read Electronic Signature
98h	Read CFI Query
B0h	Program/Erase Suspend
C0h	Protection Register Program
D0h	Program/Erase Resume
FFh	Read Memory Array

Read CFI Query Command

The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area, allowing programming equipment or applications to automatically match their interface to the characteristics of the device. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See APPENDIX B., COMMON FLASH INTERFACE (CFI), Tables 22, 23, 24, 25, 26 and 27 for details on the information contained in the Common Flash Interface memory area.

Block Erase Command

The Block Erase command can be used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.
- The second latches the block address in the internal state machine and starts the Program/Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits b4 and b5 are set and the command aborts.

Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

During Erase operations the memory will accept the Read Status Register command and the Program/Erase Suspend command, all other commands will be ignored. Typical Erase times are given in Table 7., Program, Erase Times and Program/Erase Endurance Cycles.

See APPENDIX C., Figure 18., Erase Flowchart and Pseudo Code, for a suggested flowchart for using the Erase command.

Program Command

The memory array can be programmed word-by-word. Two bus write cycles are required to issue the Program Command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

During Program operations the memory will accept the Read Status Register command and the Program/Erase Suspend command. Typical Program times are given in Table 7., Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See APPENDIX C., Figure 14., Program Flowchart and Pseudo Code, for the flowchart for using the Program command.

Double Word Program Command

This feature is offered to improve the programming throughput, writing a page of two adjacent words in parallel.The two words must differ only for the address A0.

The Double Word Program command can be issued either with V_{PP} set to V_{PPH} or to V_{DD}.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started. Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See APPENDIX C., Figure 15., Double Word Program Flowchart and Pseudo Code for the flowchart for using the Double Word Program command.

Quadruple Word Program Command

This feature is offered to improve the programming throughput, writing a page of four adjacent words in parallel.The four words must differ only for the addresses A0 and A1.

A Quadruple word Program command will be ignored if V_{PP} is not set to V_{PPH}.

Five bus write cycles are necessary to issue the Quadruple Word Program command.

- The first bus cycle sets up the Quadruple Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written.
- The fourth bus cycle latches the Address and the Data of the third word to be written.
- The fifth bus cycle latches the Address and the Data of the fourth word to be written and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started. Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the block containing the memory location must be erased and reprogrammed.

See APPENDIX C., Figure 16., Quadruple Word Program Flowchart and Pseudo Code, for the flowchart for using the Quadruple Word Program command.

Clear Status Register Command

The Clear Status Register command can be used to reset bits 1, 3, 4 and 5 in the Status Register to '0'. One bus write cycle is required to issue the Clear Status Register command.

The bits in the Status Register do not automatically return to '0' when a new Program or Erase command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

Program/Erase Suspend Command

The Program/Erase Suspend command is used to pause a Program or Erase operation. One bus write cycle is required to issue the Program/Erase

command and pause the Program/Erase controller.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read Array, Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Program, Double Word Program, Quadruple Word Program, Block Lock, or Protection Program commands will also be accepted. The block being erased may be protected by issuing the Block Protect, Block Lock or Protection Program commands. When the Program/Erase Resume command is issued the operation will complete. Only the blocks not being erased may be read or programmed correctly.

During a Program/Erase Suspend, the device can be placed in a pseudo-standby mode by taking Chip Enable to V_{IH}. Program/Erase is aborted if Reset turns to V_{IL}.

See APPENDIX C., Figure 17., Program Suspend & Resume Flowchart and Pseudo Code, and Figure 19., Erase Suspend & Resume Flowchart and Pseudo Code, for flowcharts for using the Program/Erase Suspend command.

Program/Erase Resume Command

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the command. Once the command is issued subsequent Bus Read operations read the Status Register.

See APPENDIX C., Figure 17., Program Suspend & Resume Flowchart and Pseudo Code, and Figure 19., Erase Suspend & Resume Flowchart and Pseudo Code, for flowcharts for using the Program/Erase Resume command.

Protection Register Program Command

The Protection Register Program command is used to Program the 128 bit user One-Time-Programmable (OTP) segment of the Protection Register. The segment is programmed 16 bits at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The segment can be protected by programming bit 1 of the Protection Lock Register (see Figure 6., Protection Register Memory Map). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register is not reversible.

The Protection Register Program cannot be suspended.

Table 4. Commands

Commands	Cycles	Bus Write Operations														
		1st Cycle			2nd Cycle			3rd Cycle			4th Cycle			5th Cycle		
		Op.	Add	Data	Op.	Add	Data	Op.	Add	Data	Op.	Add	Data	Op.	Add	Data
Read Memory Array	1+	Write	X	FFh	Read	RA	RD									
Read Status Register	1+	Write	X	70h	Read	X	SRD									
Read Electronic Signature	1+	Write	X	90h	Read	SA(2)	IDh									
Read CFI Query	1+	Write	X	98h	Read	QA	QD									
Erase	2	Write	X	20h	Write	BA	D0h									
Program	2	Write	X	40h or 10h	Write	PA	PD									
Double Word Program(3)	3	Write	X	30h	Write	PA1	PD1	Write	PA2	PD2						
Quadruple Word Program(4)	5	Write	X	56h	Write	PA1	PD1	Write	PA2	PD2	Write	PA3	PD3	Write	PA4	PD4
Clear Status Register	1	Write	X	50h												
Program/Erase Suspend	1	Write	X	B0h												
Program/Erase Resume	1	Write	X	D0h												
Protection Register Program	2	Write	X	C0h	Write	PRA	PRD									

Note: 1. X = Don't Care, RA=Read Address, RD=Read Data, SRD=Status Register Data, ID=Identifier (Manufacture and Device Code), QA=Query Address, QD=Query Data, BA=Block Address, PA=Program Address, PD=Program Data, PRA=Protection Register Address, PRD=Protection Register Data.
2. The signature addresses are listed in Tables 5 and 6.
3. Program Addresses 1 and 2 must be consecutive Addresses differing only for A0.
4. Program Addresses 1,2,3 and 4 must be consecutive Addresses differing only for A0 and A1.

Table 5. Read Electronic Signature

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A2-A7	A8-A20 A8-A21(2)	DQ0-DQ7	DQ8-DQ15
Manufacture Code		V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	0	Don't Care	20h	00h
Device Code	M28W320FSU	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	0Ch	88h
	M28W640FSU	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	0	Don't Care	57h	88h

Note: 1. $\overline{RP} = V_{IH}$.
2. Addresses range from A0 to A20 for the M28W320FSU and from A0 to A21 for the M28W640FSU.

Table 6. Read Protection Register and Protection Register Lock

Word	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0-A7	A8-A21(1)	DQ0	DQ1	DQ2	DQ3-DQ7	DQ8-DQ15
Lock	V_{IL}	V_{IL}	V_{IH}	80h	Don't Care	0	OTP Prot. data	0	00h	00h
Unique ID 0	V_{IL}	V_{IL}	V_{IH}	81h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 1	V_{IL}	V_{IL}	V_{IH}	82h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 2	V_{IL}	V_{IL}	V_{IH}	83h	Don't Care	ID data	ID data	ID data	ID data	ID data
Unique ID 3	V_{IL}	V_{IL}	V_{IH}	84h	Don't Care	ID data	ID data	ID data	ID data	ID data
OTP 0	V_{IL}	V_{IL}	V_{IH}	85h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 1	V_{IL}	V_{IL}	V_{IH}	86h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 2	V_{IL}	V_{IL}	V_{IH}	87h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 3	V_{IL}	V_{IL}	V_{IH}	88h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 4	V_{IL}	V_{IL}	V_{IH}	89h	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 5	V_{IL}	V_{IL}	V_{IH}	8Ah	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 6	V_{IL}	V_{IL}	V_{IH}	8Bh	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data
OTP 7	V_{IL}	V_{IL}	V_{IH}	8Ch	Don't Care	OTP data	OTP data	OTP data	OTP data	OTP data

Note: 1. Addresses range from A0 to A20 for the M28W320FSU and from A0 to A21 for the M28W640FSU.

Table 7. Program, Erase Times and Program/Erase Endurance Cycles

Parameter		Test Conditions	M28W320FSU, M28W640FSU			Unit
			Min	Typ	Max	
Word Program		$V_{PP} = V_{DD}$		10	200	µs
Double Word Program		$V_{PP} = V_{PPH}$ or $V_{PP} = V_{DD}$		10	200	µs
Quadruple Word Program		$V_{PP} = V_{PPH}$		10	200	µs
Block Program	Using Word Program command	$V_{PP} = V_{DD}$		0.64	5	s
	Using Double Word Program command	$V_{PP} = V_{PPH}$ or $V_{PP} = V_{DD}$		0.32		s
	Using Quadruple Word Program command	$V_{PP} = V_{PPH}$		0.16		s
Block Erase		$V_{PP} = V_{PPH}$ or $V_{PP} = V_{DD}$		1	10	s
Program/Erase Cycles (per Block)			100,000			cycles
Data Retention			20			years

STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operation. The various bits convey information and errors on the operation. To read the Status register the Read Status Register command can be issued, refer to Read Status Register Command section. To output the contents, the Status Register is latched on the falling edge of the Chip Enable or Output Enable signals, and can be read until Chip Enable or Output Enable returns to V_{IH}. Either Chip Enable or Output Enable must be toggled to update the latched data.

Bus Read operations from any address always read the Status Register during Program and Erase operations.

The bits in the Status Register are summarized in Table 8., Status Register Bits. Refer to Table 8. in conjunction with the following text descriptions.

Program/Erase Controller Status (Bit 7). The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive. When the Program/Erase Controller Status bit is Low (set to '0'), the Program/Erase Controller is active; when the bit is High (set to '1'), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, operations the Program/Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, V_{PP} Status and Block Lock Status bits should be tested for errors.

Erase Suspend Status (Bit 6). The Erase Suspend Status bit indicates that an Erase operation has been suspended or is going to be suspended. When the Erase Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 7 is set within 30µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

Erase Status (Bit 5). The Erase Status bit can be used to identify if the memory has failed to verify that the block has erased correctly. When the Erase Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the block and still failed to verify that the block has erased correctly. The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Status (Bit 4). The Program Status bit is used to identify a Program failure. When the Program Status bit is High (set to '1'), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly. The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

V_{PP} Status (Bit 3). The V_{PP} Status bit can be used to identify an invalid voltage on the V_{PP} pin during Program and Erase operations. The V_{PP} pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low (set to '0'), the voltage on the V_{PP} pin was sampled at a valid voltage; when the V_{PP} Status bit is High (set to '1'), the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected and Program and Erase operations cannot be performed.

Once set High, the V_{PP} Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

Program Suspend Status (Bit 2). The Program Suspend Status bit indicates that a Program operation has been suspended. When the Program Suspend Status bit is High (set to '1'), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command. The Program Suspend Status should only be considered valid when the Pro-

gram/Erase Controller Status bit is High (Program/Erase Controller inactive). Bit 2 is set within 5µs of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

Block Protection Status (Bit 1). The Block Protection Status bit can be used to identify if a Program or Erase operation has tried to modify the contents of a locked block.

When the Block Protection Status bit is High (set to '1'), a Program or Erase operation has been attempted on a locked block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

Reserved (Bit 0). Bit 0 of the Status Register is reserved. Its value must be masked.

Note: Refer to APPENDIX C., FLOWCHARTS AND PSEUDO CODES, for using the Status Register.

Table 8. Status Register Bits

Bit	Name	Logic Level	Definition
7	P/E.C. Status	'1'	Ready
		'0'	Busy
6	Erase Suspend Status	'1'	Suspended
		'0'	In progress or Completed
5	Erase Status	'1'	Erase Error
		'0'	Erase Success
4	Program Status	'1'	Program Error
		'0'	Program Success
3	V_{PP} Status	'1'	V_{PP} Invalid, Abort
		'0'	V_{PP} OK
2	Program Suspend Status	'1'	Suspended
		'0'	In Progress or Completed
1	Block Protection Status	'1'	Program/Erase on protected Block, Abort
		'0'	No operation to protected blocks
0	Reserved		

Note: Logic level '1' is High, '0' is Low.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature (1)	– 40	85	°C
T_{BIAS}	Temperature Under Bias	– 40	125	°C
T_{STG}	Storage Temperature	– 55	155	°C
T_{LEAD}	Lead Temperature during Soldering		(2)	°C
V_{IO}	Input or Output Voltage	– 0.6	V_{DDQ}+0.6	V
V_{DD}, V_{DDQ}	Supply Voltage	– 0.6	4.1	V
V_{PP}	Program Voltage	– 0.6	13	V

Note: 1. Depends on range.
2. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 10., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 10. Operating and AC Measurement Conditions

Parameter	M28W320FSU, M28W640FSU		
	70		Units
	Min	Max	
V_{DD} Supply Voltage	2.7	3.6	V
V_{DDQ} Supply Voltage	2.7	3.6	V
Ambient Operating Temperature	–40	85	°C
Load Capacitance (C_L)	50		pF
Input Rise and Fall Times		5	ns
Input Pulse Voltages	0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		V

Figure 7. AC Measurement I/O Waveform

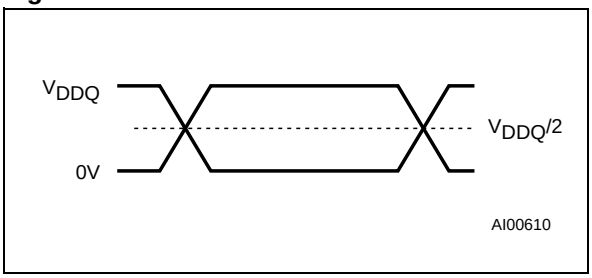


Figure 8. AC Measurement Load Circuit

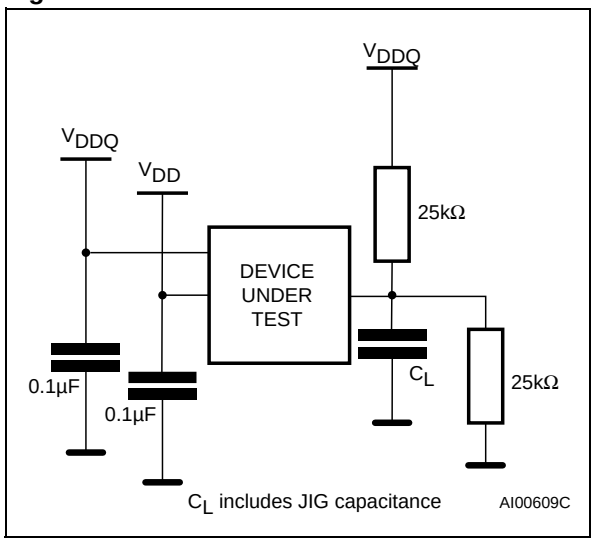


Table 11. Capacitance

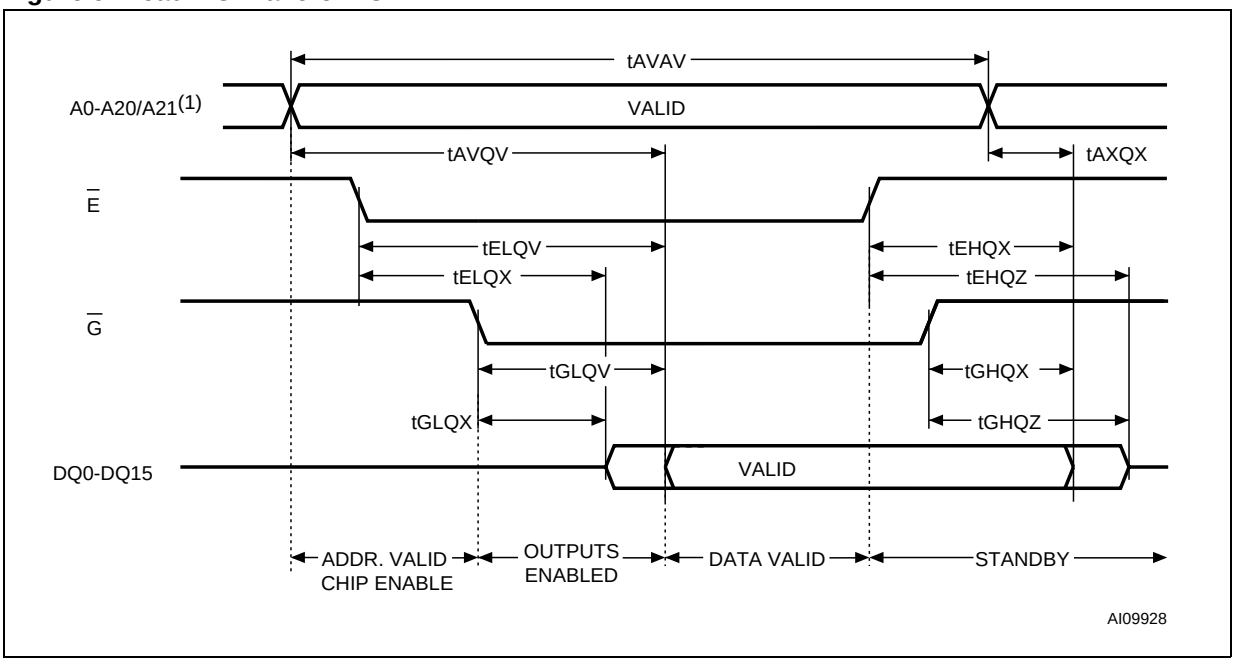
Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 12. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±10	µA
I_{DD}	Supply Current (Read)	$\overline{E} = V_{SS}$, $\overline{G} = V_{IH}$, f = 5MHz		9	18	mA
I_{DD1}	Supply Current (Stand-by or Automatic Stand-by)	$\overline{E} = V_{DDQ} \pm 0.2V$, $\overline{RP} = V_{DDQ} \pm 0.2V$		15	50	µA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		15	50	µA
I_{DD3}	Supply Current (Program)	Program in progress $V_{PP} = 12V \pm 5\%$		5	10	mA
		Program in progress $V_{PP} = V_{DD}$		10	20	mA
I_{DD4}	Supply Current (Erase)	Erase in progress $V_{PP} = 12V \pm 5\%$		5	20	mA
		Erase in progress $V_{PP} = V_{DD}$		10	20	mA
I_{DD5}	Supply Current (Program/Erase Suspend)	$\overline{E} = V_{DDQ} \pm 0.2V$, Erase suspended		15	50	µA
I_{PP}	Program Current (Read or Stand-by)	$V_{PP} > V_{DD}$			400	µA
I_{PP1}	Program Current (Read or Stand-by)	$V_{PP} \le V_{DD}$		1	5	µA
I_{PP2}	Program Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$		1	5	µA
I_{PP3}	Program Current (Program)	Program in progress $V_{PP} = 12V \pm 5\%$		1	10	mA
		Program in progress $V_{PP} = V_{DD}$		1	5	µA
I_{PP4}	Program Current (Erase)	Erase in progress $V_{PP} = 12V \pm 5\%$		3	10	mA
		Erase in progress $V_{PP} = V_{DD}$		1	5	µA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{DDQ}		V_{DDQ} +0.4	V
V_{OL}	Output Low Voltage	$I_{OL} = 100µA$, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min			0.1	V
V_{OH}	Output High Voltage	$I_{OH} = –100µA$, $V_{DD} = V_{DD}$ min, $V_{DDQ} = V_{DDQ}$ min	V_{DDQ} –0.1			V
V_{PP1}	Program Voltage (Program or Erase operations)		2.7		3.6	V
V_{PPH}	Program Voltage (Program or Erase operations)		11.4		12.6	V
V_{PPLK}	Program Voltage (Program and Erase lock-out)				1	V
V_{LKO}	V_{DD} Supply Voltage (Program and Erase lock-out)				2	V

Figure 9. Read AC Waveforms



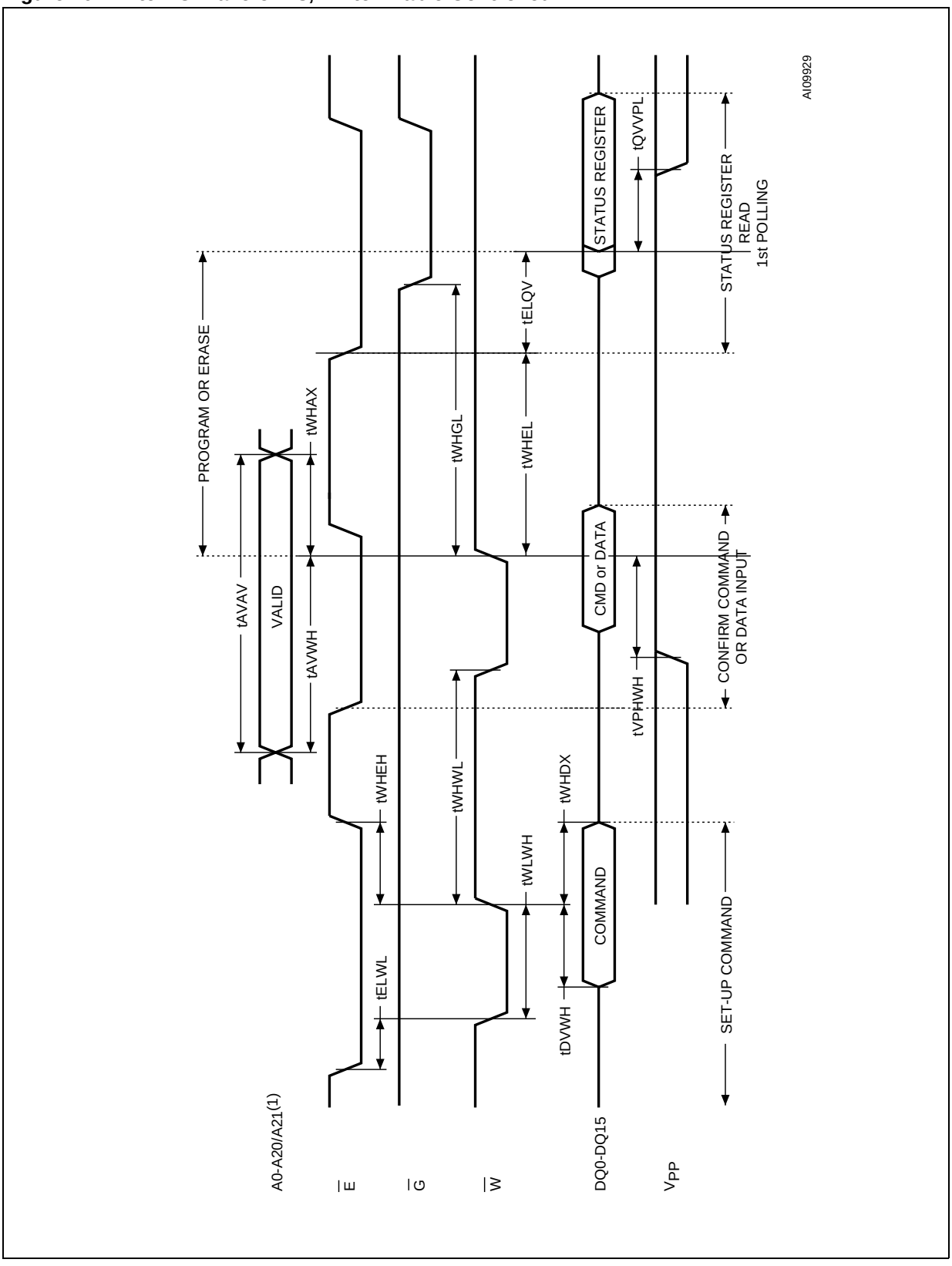
Note: 1. Addresses range from A0 to A20 for the M28W320FSU and from A0 to A21 for the M28W640FSU.

Table 13. Read AC Characteristics

Symbol	Alt	Parameter		M28W320FSU	M28W640FSU	Unit
				70	70	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	70	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	Max	70	70	ns
t_{AXQX} (1)	t_{OH}	Address Transition to Output Transition	Min	0	0	ns
t_{EHQX} (1)	t_{OH}	Chip Enable High to Output Transition	Min	0	0	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	Max	20	20	ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	Max	70	70	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	Min	0	0	ns
t_{GHQX} (1)	t_{OH}	Output Enable High to Output Transition	Min	0	0	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	Max	20	20	ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	Max	20	20	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	Min	0	0	ns

Note: 1. Sampled only, not 100% tested.
2. G may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of E without increasing t_{ELQV}.

Figure 10. Write AC Waveforms, Write Enable Controlled



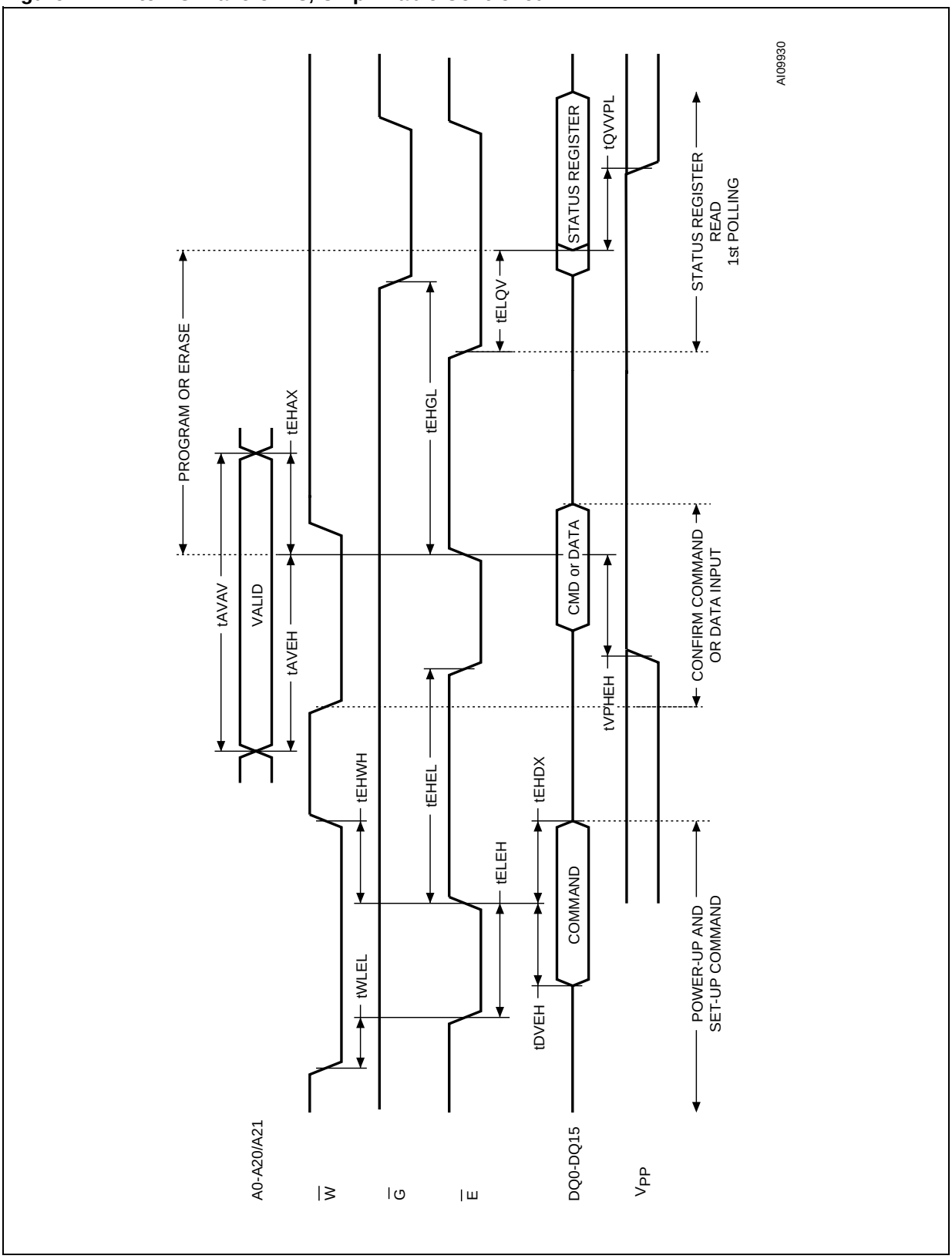
Note: 1. Addresses range from A0 to A20 for the M28W320FSU and from A0 to A21 for the M28W640FSU.

Table 14. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter		M28W320FSU	M28W640FSU	Unit
				70	70	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	70	ns
t_{AVWH}	t_{AS}	Address Valid to Write Enable High	Min	45	45	ns
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Min	45	45	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{ELQV}		Chip Enable Low to Output Valid	Min	70	70	ns
t_{QVVPL} (1,2)		Output Valid to V_{PP} Low	Min	0	0	ns
t_{VPHWH} (1)	t_{VPS}	V_{PP} High to Write Enable High	Min	200	200	ns
t_{WHAX}	t_{AH}	Write Enable High to Address Transition	Min	0	0	ns
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHEL}		Write Enable High to Chip Enable Low	Min	25	25	ns
t_{WHGL}		Write Enable High to Output Enable Low	Min	20	20	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	25	25	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

Figure 11. Write AC Waveforms, Chip Enable Controlled



Note: 1. Addresses range from A0 to A20 for the M28W320FSU and from A0 to A21 for the M28W640FSU.

Table 15. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter		M28W320FSU	M28W640FSU	Unit
				70	70	
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	70	ns
t_{AVEH}	t_{AS}	Address Valid to Chip Enable High	Min	45	45	ns
t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	Min	45	45	ns
t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	Min	0	0	ns
t_{EHDX}	t_{DH}	Chip Enable High to Data Transition	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	25	25	ns
t_{EHGL}		Chip Enable High to Output Enable Low	Min	25	25	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	ns
t_{ELQV}		Chip Enable Low to Output Valid	Min	70	70	ns
t_{QVVPL} (1,2)		Output Valid to V_{PP} Low	Min	0	0	ns
t_{VPHEH} (1)	t_{VPS}	V_{PP} High to Chip Enable High	Min	200	200	ns
t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	Min	0	0	ns

Note: 1. Sampled only, not 100% tested.
2. Applicable if V_{PP} is seen as a logic input (V_{PP} < 3.6V).

Figure 12. Power-Up and Reset AC Waveforms

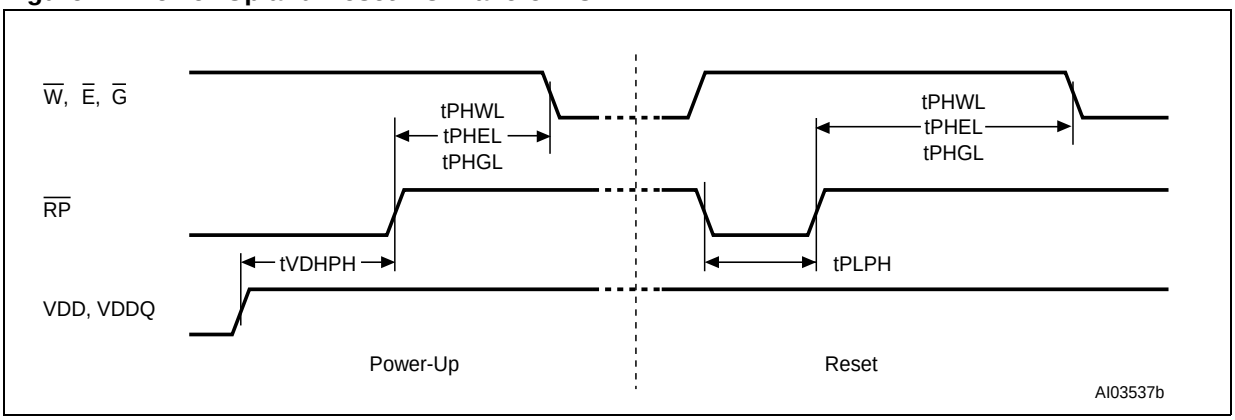


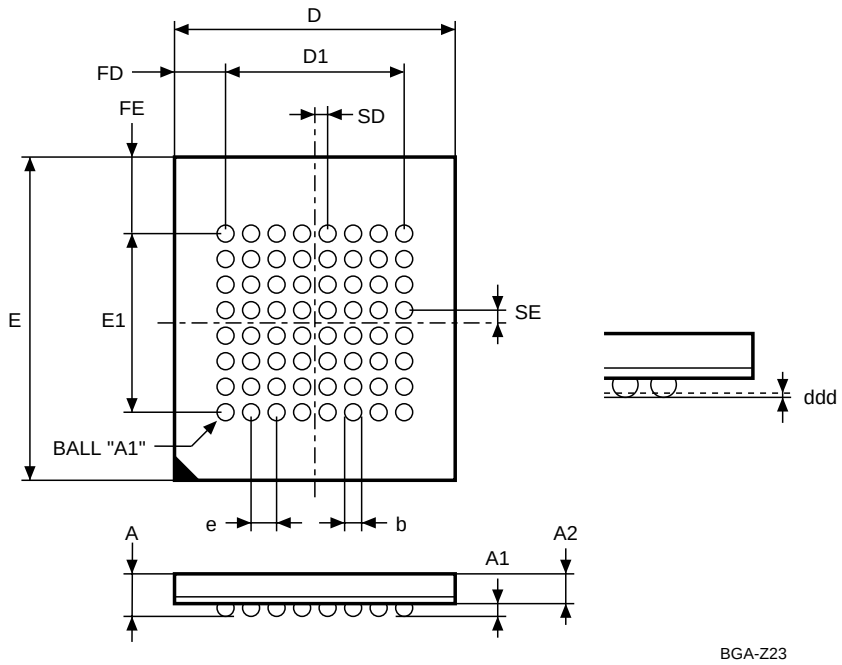
Table 16. Power-Up and Reset AC Characteristics

Symbol	Parameter	Test Condition		M28W320FSU, M28W640FSU	Unit
				70	
t_{PHWL} t_{PHEL} t_{PHGL}	Reset High to Write Enable Low, Chip Enable Low, Output Enable Low	During Program and Erase	Min	50	µs
		others	Min	30	ns
t_{PLPH}(1,2)	Reset Low to Reset High		Min	100	ns
t_{VDHPH}(3)	Supply Voltages High to Reset High		Min	50	µs

Note: 1. The device Reset is possible but not guaranteed if t_{PLPH} < 100ns.
2. Sampled only, not 100% tested.
3. It is important to assert RP in order to allow proper CPU initialization during power up or reset.

PACKAGE MECHANICAL

Figure 13. TBGA64 - 10x13 active ball array, 1mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 17. TBGA64 - 10x13 active ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2	0.800			0.0315		
b		0.350	0.500		0.0138	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000	–	–	0.2756	–	–
ddd			0.100			0.0039
e	1.000	–	–	0.0394	–	–
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	7.000	–	–	0.2756	–	–
FD	1.500	–	–	0.0591	–	–
FE	3.000	–	–	0.1181	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

PART NUMBERING

Table 18. Ordering Information Scheme

Example: M28W320FSU 70 ZA 6 T

Device Type
M28

Operating Voltage
W = V_{DD} = 2.7V to 3.6V; V_{DDQ} = 2.7V to 3.6V

Device Function
320FSU = 32 Mbit (2 Mb x16), Uniform Block, Secure, 0.13µm
640FSU = 64 Mbit (4 Mb x16), Uniform Block, Secure, 0.13µm

Speed
70 = 70ns

Package
ZA = TBGA64:10 x 13mm, 1mm pitch

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-Free and RoHS Package, Standard Packing
F = Lead-Free and RoHS Package, Tape & Reel Packing

Table 19. Daisy Chain Ordering Scheme

Example: M28W640FSU -ZA T

Device Type

M28W320FSU
M28W640FSU

Daisy Chain

-ZA = TBGA64: 10 x 13, 1mm pitch

Option

Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-Free and RoHS Package, Standard Packing
F = Lead-Free and RoHS Package, Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

APPENDIX A. BLOCK ADDRESS TABLES

Table 20. Block Addresses, M28W320FSU

Block Number	Address Range
31	1F0000h-1FFFFFh
30	1E0000h-1EFFFFh
29	1D0000h-1DFFFFh
28	1C0000h-1CFFFFh
27	1B0000h-1BFFFFh
26	1A0000h-1AFFFFh
25	190000h-19FFFFh
24	180000h-18FFFFh
23	170000h-17FFFFh
22	160000h-16FFFFh
21	150000h-15FFFFh
20	140000h-14FFFFh
19	130000h-13FFFFh
18	120000h-12FFFFh
17	110000h-11FFFFh
16	100000h-10FFFFh
15	0F0000h-0FFFFFh
14	0E0000h-0EFFFFh
13	0D0000h-0DFFFFh
12	0C0000h-0CFFFFh
11	0B0000h-0BFFFFh
10	0A0000h-0AFFFFh
9	090000h-09FFFFh
8	080000h-08FFFFh
7	070000h-07FFFFh
6	060000h-06FFFFh
5	050000h-05FFFFh
4	040000h-04FFFFh
3	030000h-03FFFFh
2	020000h-02FFFFh
1	010000h-01FFFFh
0	000000h-00FFFFh

Table 21. Block Addresses, M28W640FSU

Block Number	Address Range
63	3F0000h-3FFFFFh
62	3E0000h-3EFFFFh
61	3D0000h-3DFFFFh
60	3C0000h-3CFFFFh
59	3B0000h-3BFFFFh
58	3A0000h-3AFFFFh
57	390000h-39FFFFh
56	380000h-38FFFFh
55	370000h-37FFFFh
54	360000h-36FFFFh
53	350000h-35FFFFh
52	340000h-34FFFFh
51	330000h-33FFFFh
50	320000h-32FFFFh
49	310000h-31FFFFh
48	300000h-30FFFFh
47	2F0000h-2FFFFFh
46	2E0000h-2EFFFFh
45	2D0000h-2DFFFFh
44	2C0000h-2CFFFFh
43	2B0000h-2BFFFFh
42	2A0000h-2AFFFFh
41	290000h-29FFFFh
40	280000h-28FFFFh
39	270000h-27FFFFh
38	260000h-26FFFFh
37	250000h-25FFFFh
36	240000h-24FFFFh
35	230000h-23FFFFh
34	220000h-22FFFFh
33	210000h-21FFFFh
32	200000h-20FFFFh
31	1F0000h-1FFFFFh
30	1E0000h-1EFFFFh
29	1D0000h-1DFFFFh
28	1C0000h-1CFFFFh
27	1B0000h-1BFFFFh
26	1A0000h-1AFFFFh
25	190000h-19FFFFh
24	180000h-18FFFFh
23	170000h-17FFFFh
22	160000h-16FFFFh
21	150000h-15FFFFh
20	140000h-14FFFFh
19	130000h-13FFFFh
18	120000h-12FFFFh
17	110000h-11FFFFh
16	100000h-10FFFFh
15	0F0000h-0FFFFFh
14	0E0000h-0EFFFFh
13	0D0000h-0DFFFFh
12	0C0000h-0CFFFFh
11	0B0000h-0BFFFFh
10	0A0000h-0AFFFFh
9	090000h-09FFFFh
8	080000h-08FFFFh
7	070000h-07FFFFh
6	060000h-06FFFFh
5	050000h-05FFFFh
4	040000h-04FFFFh
3	030000h-03FFFFh
2	020000h-02FFFFh
1	010000h-01FFFFh
0	000000h-00FFFFh

APPENDIX B. COMMON FLASH INTERFACE (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command (RCFI) is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 22, 23, 24, 25, 26 and 27 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 27., Security Code Area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read command to return to Read mode.

Table 22. Query Structure Overview

Offset	Sub-section Name	Description
00h	Reserved	Reserved for algorithm-specific information
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)

Note: Query data are always presented on the lowest order data outputs.

Table 23. CFI Query Identification String

Offset	Data	Description	Value
00h	0020h	Manufacturer Code	ST
01h	880Ch 8857h	M28W320FSU Device Code M28W640FSU Device Code	Uniform
02h-0Fh	reserved	Reserved	
10h	0051h	Query Unique ASCII String "QRY"	"Q"
11h	0052h		"R"
12h	0059h		"Y"
13h	0003h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	Intel compatible
14h	0000h		
15h	0035h	Address for Primary Algorithm extended Query table (see Table 26.)	P = 35h
16h	0000h		
17h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported (0000h means none exists)	NA
18h	0000h		
19h	0000h	Address for Alternate Algorithm extended Query table (0000h means none exists)	NA
1Ah	0000h		

Note: Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are '0'.

Table 24. CFI Query System Interface Information

Offset	Data	Description	Value
1Bh	0027h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100mV	2.7V
1Ch	0036h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100mV	3.6V
1Dh	00B4h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100mV	11.4V
1Eh	00C6h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100mV	12.6V
1Fh	0004h	Typical time-out per single word program = 2^n µs	16µs
20h	0004h	Typical time-out for Double/Quadruple Word Program = 2^n µs	16µs
21h	000Ah	Typical time-out per individual block erase = 2^n ms	1s
22h	0000h	Typical time-out for full chip erase = 2^n ms	NA
23h	0005h	Maximum time-out for Word program = 2^n times typical	512µs
24h	0005h	Maximum time-out for Double/Quadruple Word Program = 2^n times typical	512µs
25h	0003h	Maximum time-out per individual block erase = 2^n times typical	8s
26h	0000h	Maximum time-out for chip erase = 2^n times typical	NA

Table 25. Device Geometry Definition

Offset Word Mode		Data	Description	Value
M28W320FSU	27h	0016h	Device Size = 2^n in number of bytes	4 MBytes
M28W640FSU	27h	0017h	Device Size = 2^n in number of bytes	8 MBytes
28h 29h		0001h 0000h	Flash Device Interface Code description	x16 Async.
2Ah 2Bh		0003h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	8
2Ch		0001h	Number of Erase Block Regions within the device. It specifies the number of regions within the device containing contiguous Erase Blocks of the same size.	1
M28W320FSU	2Dh 2Eh	001Fh 0000h	Region 1 Information Number of identical-size erase blocks = 001Fh+1	32
M28W320FSU	2Fh 30h	0000h 0002h	Region 1 Information Block size in Region 1 = 0200h * 256 byte	128 KBytes
M28W640FSU	2Dh 2Eh	003Fh 0000h	Region 1 Information Number of identical-size erase blocks = 003Fh+1	64
M28W640FSU	2Fh 30h	0000h 0002h	Region 1 Information Block size in Region 1 = 0200h * 256 byte	128 KBytes
31h to 34h			Reserved	

Table 26. Primary Algorithm-Specific Extended Query Table

Offset P = 35h (1)	Data	Description	Value
(P+0)h = 35h	0050h		"P"
(P+1)h = 36h	0052h	Primary Algorithm extended Query table unique ASCII string “PRI”	"R"
(P+2)h = 37h	0049h		"I"
(P+3)h = 38h	0031h	Major version number, ASCII	"1"
(P+4)h = 39h	0030h	Minor version number, ASCII	"0"
(P+5)h = 3Ah	0066h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte.	
(P+6)h = 3Bh	0000h	bit 0Chip Erase supported(1 = Yes, 0 = No)	No
		bit 1Suspend Erase supported(1 = Yes, 0 = No)	Yes
(P+7)h = 3Ch	0000h	bit 2Suspend Program supported(1 = Yes, 0 = No)	Yes
		bit 3Legacy Lock/Unlock supported(1 = Yes, 0 = No)	No
(P+8)h = 3Dh	0000h	bit 4Queued Erase supported(1 = Yes, 0 = No)	No
		bit 5Instant individual block locking supported(1 = Yes, 0 = No)	Yes
		bit 6Protection bits supported(1 = Yes, 0 = No)	Yes
		bit 7Page mode read supported(1 = Yes, 0 = No)	No
		bit 8Synchronous read supported(1 = Yes, 0 = No)	No
		bit 31 to 9 Reserved; undefined bits are ‘0’	
(P+9)h = 3Eh	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query are always supported during Erase or Program operation	
		bit 0Program supported after Erase Suspend (1 = Yes, 0 = No)	
		bit 7 to 1Reserved; undefined bits are ‘0’	Yes
(P+A)h = 3Fh	0003h	Block Lock Status Defines which bits in the Block Status Register section of the Query are implemented. Address (P+A)h contains less significant byte	
(P+B)h = 40h	0000h		
		bit 0 Block Lock Status Register Lock/Unlock bit active(1 = Yes, 0 = No)	Yes
		bit 15 to 1Reserved for future use; undefined bits are ‘0’	
(P+C)h = 41h	0030h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100mV	3V
(P+D)h = 42h	00C0h	V_{PP} Supply Optimum Program/Erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100mV	12V
(P+E)h = 43h	0001h	Number of Protection register fields in JEDEC ID space. "00h," indicates that 256 protection bytes are available	01
(P+F)h = 44h	0080h	Protection Field 1: Protection Description	80h
(P+10)h = 45h	0000h	This field describes user-available One Time Programmable (OTP) Protection Register bytes. Some are pre-programmed with device unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection Register Lock byte, the section’s first byte.	00h
(P+11)h = 46h	0003h		8 Bytes
(P+12)h = 47h	0004h	The following bytes are factory pre-programmed and user-programmable.	16 Bytes
		bit 0 to 7 Lock/bytes JEDEC-plane physical low address	
		bit 8 to 15Lock/bytes JEDEC-plane physical high address	
		bit 16 to 23 "n" such that 2^n = factory pre-programmed bytes	
		bit 24 to 31 "n" such that 2^n = user programmable bytes	
(P+13)h = 48h		Reserved	

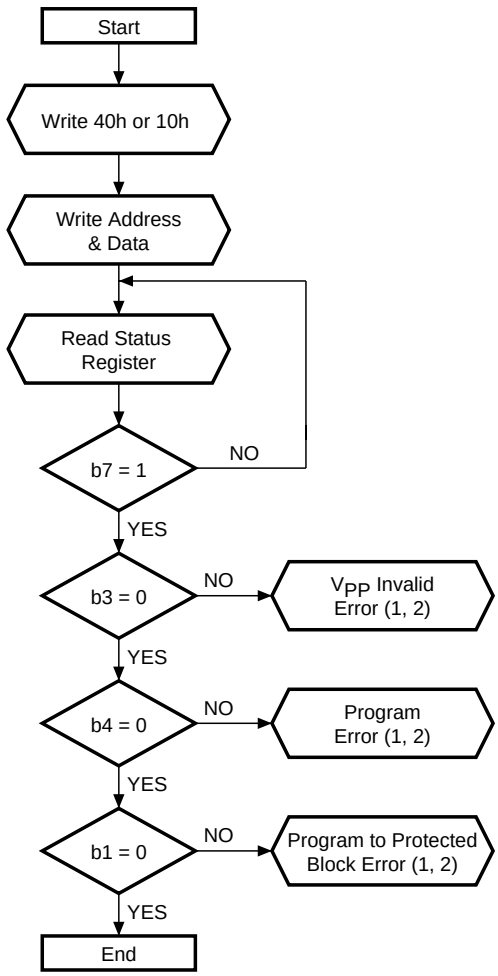
Note: 1. See Table 23., offset 15 for P pointer definition.

Table 27. Security Code Area

Offset	Data	Description
80h	00XX	Protection Register Lock
81h	XXXX	64 bits: unique device number
82h	XXXX	
83h	XXXX	
84h	XXXX	
85h	XXXX	128 bits: User Programmable OTP
86h	XXXX	
87h	XXXX	
88h	XXXX	
89h	XXXX	
8Ah	XXXX	
8Bh	XXXX	
8Ch	XXXX	

APPENDIX C. FLOWCHARTS AND PSEUDO CODES

Figure 14. Program Flowchart and Pseudo Code

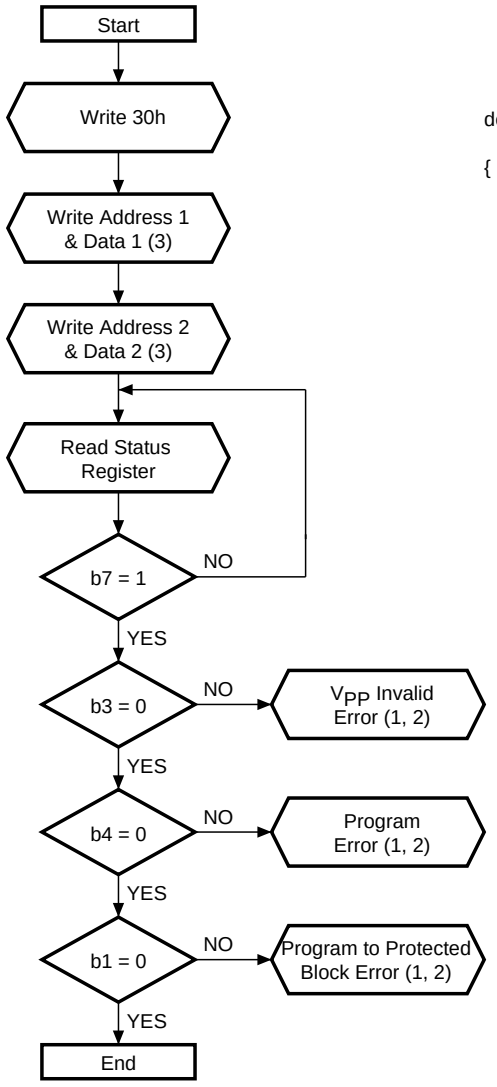



```
program_command (addressToProgram, dataToProgram) {:
        writeToFlash (any_address, 0x40) ;
        /*or writeToFlash (any_address, 0x10) ; */

         writeToFlash (addressToProgram, dataToProgram) ;
         /*Memory enters read status state after
         the Program Command*/

      do {
         status_register=readFlash (any_address) ;
         /* Ē or Ḡ must be toggled*/

         } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI03538b

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

Figure 15. Double Word Program Flowchart and Pseudo Code

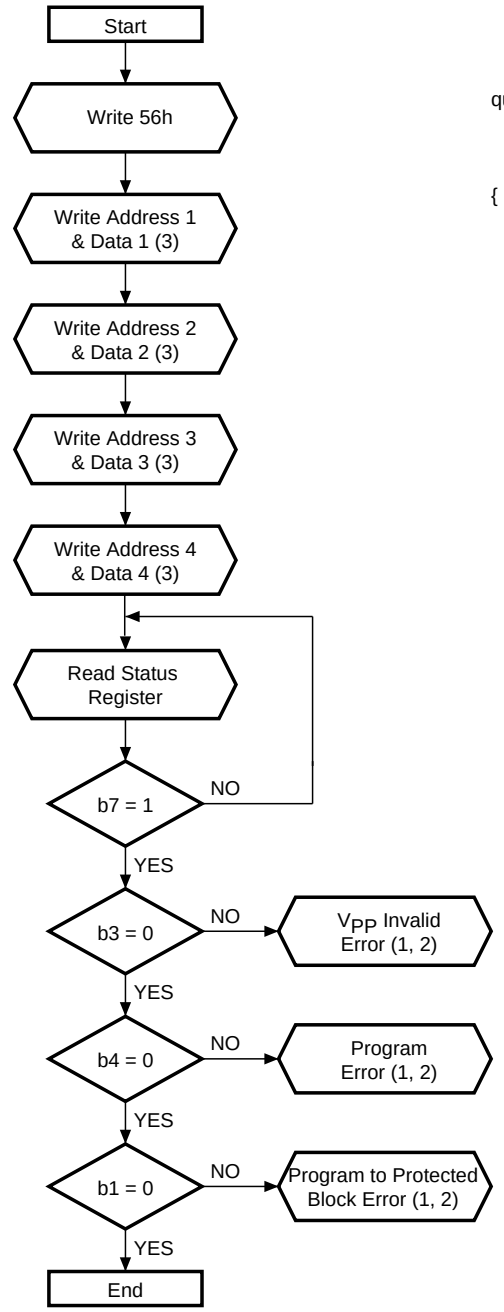



```
double_word_program_command (addressToProgram1, dataToProgram1,
                                        addressToProgram2, dataToProgram2)
{
        writeToFlash (any_address, 0x30) ;
        writeToFlash (addressToProgram1, dataToProgram1) ;
                                        /*see note (3) */
        writeToFlash (addressToProgram2, dataToProgram2) ;
                                        /*see note (3) */
         /*Memory enters read status state after
        the Program command*/

      do {
        status_register=readFlash (any_address) ;
        /* Ē or Ḡ must be toggled*/

        } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI03539b

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 and Address 2 must be consecutive addresses differing only for bit A0.

Figure 16. Quadruple Word Program Flowchart and Pseudo Code

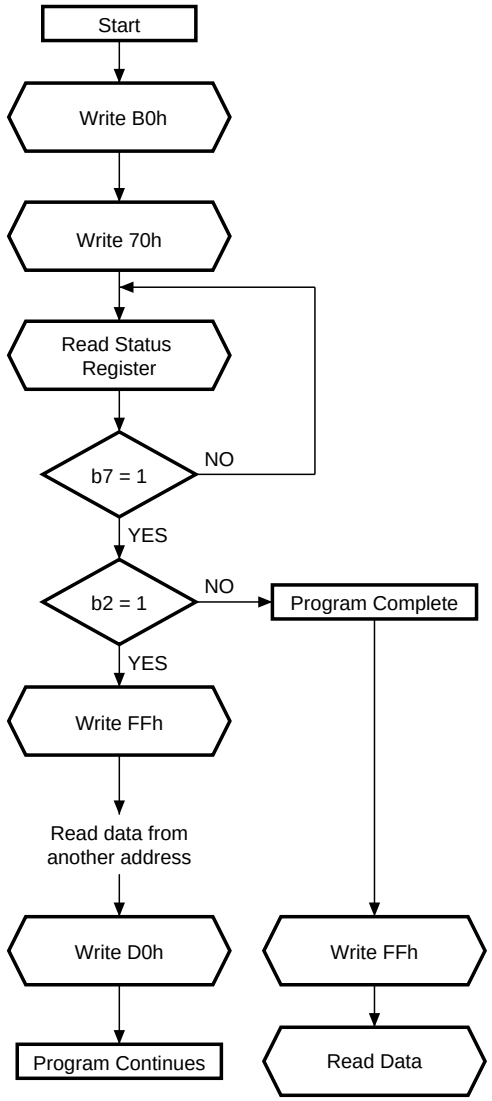



```
quadruple_word_program_command (addressToProgram1, dataToProgram1,
                                addressToProgram2, dataToProgram2,
                                addressToProgram3, dataToProgram3,
                                addressToProgram4, dataToProgram4)
{
        writeToFlash (any_address, 0x56) ;

        writeToFlash (addressToProgram1, dataToProgram1) ;
                                /*see note (3) */

        writeToFlash (addressToProgram2, dataToProgram2) ;
                                /*see note (3) */

        writeToFlash (addressToProgram3, dataToProgram3) ;
                                /*see note (3) */

        writeToFlash (addressToProgram4, dataToProgram4) ;
                                /*see note (3) */

         /*Memory enters read status state after
        the Program command*/

      do {
        status_register=readFlash (any_address) ;
        /* E or G must be toggled*/

        } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI06233

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase operations.
3. Address 1 to Address 4 must be consecutive addresses differing only for bits A0 and A1.

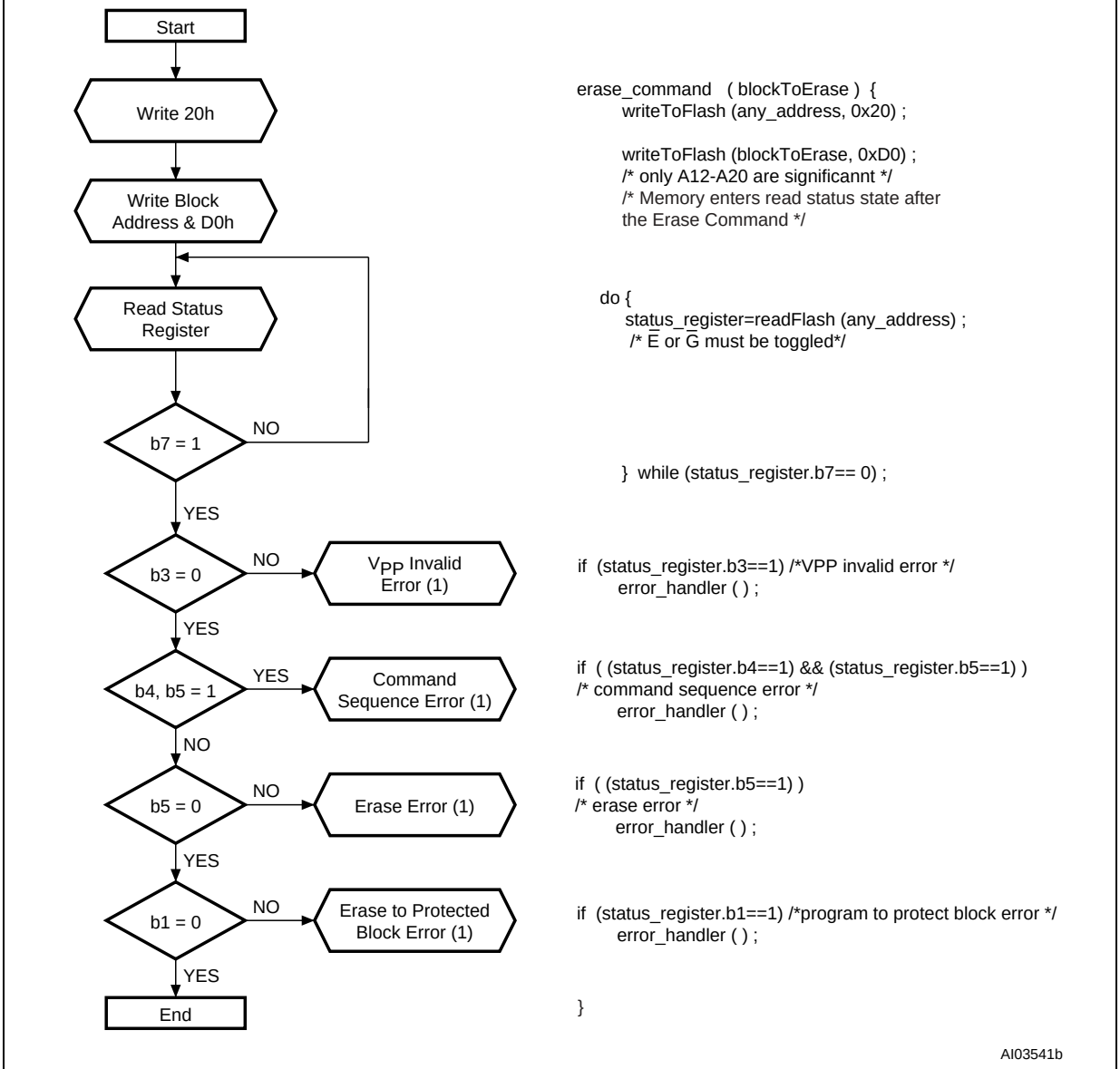
Figure 17. Program Suspend & Resume Flowchart and Pseudo Code




```
program_suspend_command   ( ) {
      writeToFlash (any_address, 0xB0) ;

      writeToFlash (any_address, 0x70) ;
      /* read status register to check if
      program has already completed */


  do {
      status_register=readFlash (any_address) ;
      /* E or G must be toggled*/

      } while (status_register.b7== 0) ;

if  (status_register.b2==0)  /*program completed */
      {  writeToFlash (any_address, 0xFF)  ;
        read_data ( ) ; /*read data from another block*/
        /*The device returns to Read Array
        (as if program/erase suspend was not issued).*/

       }
else
      {  writeToFlash (any_address, 0xFF)  ;
        read_data ( ); /*read data from another address*/
        writeToFlash (any_address, 0xD0) ;
        /*write 0xD0 to resume program*/
       }
}
```

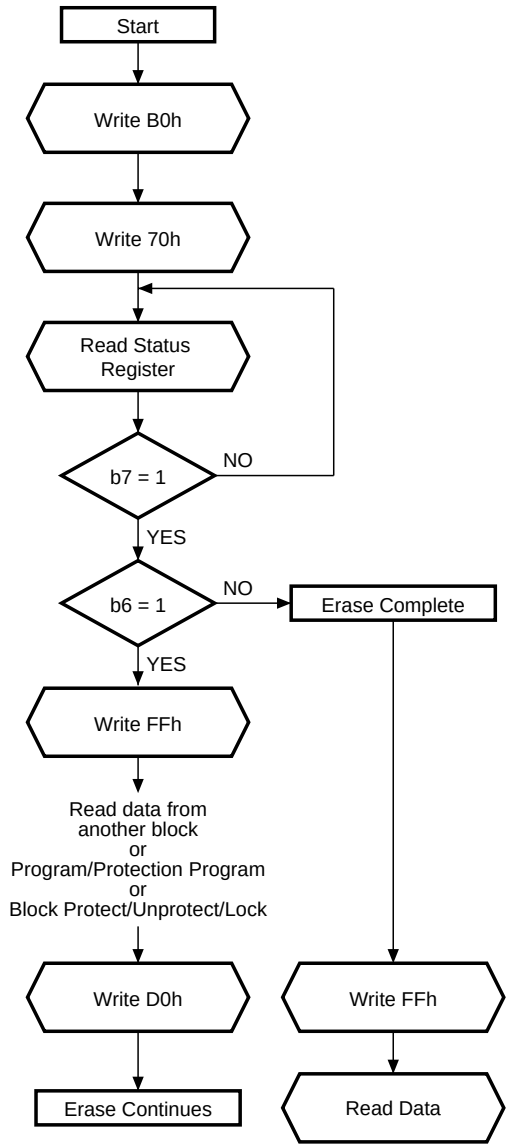
AI03540b

Figure 18. Erase Flowchart and Pseudo Code



Note: If an error is found, the Status Register must be cleared before further Program/Erase operations.

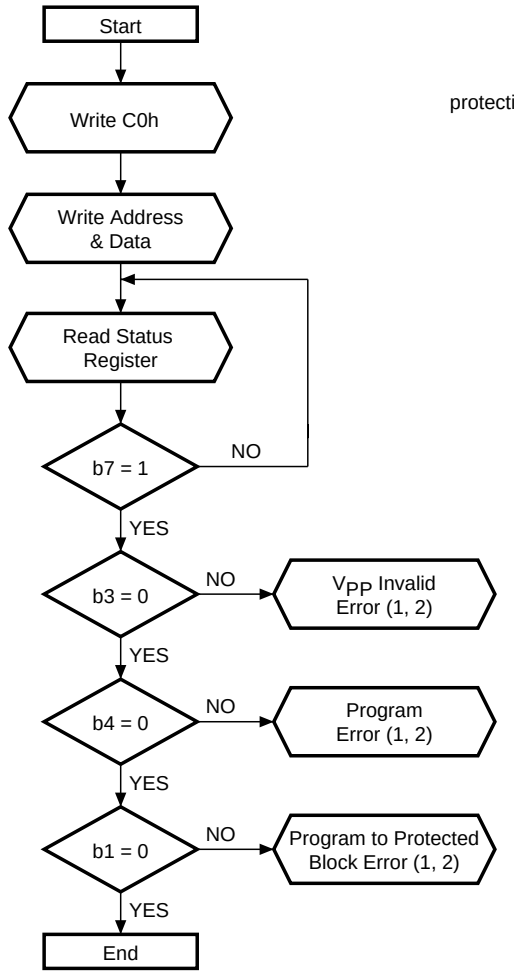
Figure 19. Erase Suspend & Resume Flowchart and Pseudo Code




```
erase_suspend_command   ( ) {
      writeToFlash (any_address, 0xB0) ;

      writeToFlash (any_address, 0x70) ;
      /* read status register to check if
      erase has already completed */


   do {
      status_register=readFlash (any_address) ;
      /* E or G must be toggled*/

      } while (status_register.b7== 0) ;

if  (status_register.b6==0)  /*erase completed */
      {  writeToFlash (any_address, 0xFF)  ;

        read_data ( ) ;
        /*read data from another block*/
        /*The device returns to Read Array
        (as if program/erase suspend was not issued).*/

      }
else
      {  writeToFlash (any_address, 0xFF)  ;
        read_program_data ( );
        /*read or program data from another address*/
        writeToFlash (any_address, 0xD0) ;
        /*write 0xD0 to resume erase*/
      }
}
```

AI03542b

Figure 20. Protection Register Program Flowchart and Pseudo Code




```
protection_register_program_command (addressToProgram, dataToProgram) {:
                        writeToFlash (any_address, 0xC0) ;

                        writeToFlash (addressToProgram, dataToProgram) ;
                        /*Memory enters read status state after
                        the Program Command*/

                    do {
                        status_register=readFlash (any_address) ;
                        /* E or G must be toggled*/

                    } while (status_register.b7== 0) ;

if  (status_register.b3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.b4==1) /*program error */
      error_handler ( ) ;

if  (status_register.b1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI04381

Note: 1. Status check of b1 (Protected Block), b3 (V_{PP} Invalid) and b4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.

APPENDIX D. COMMAND INTERFACE AND PROGRAM/ERASE CONTROLLER STATE

Table 28. Write State Machine Current/Next, sheet 1 of 2.

Current State	SR bit 7	Data When Read	Command Input (and Next State)							
			Read Array (FFh)	Program Setup (10/40h)	Erase Setup (20h)	Erase Confirm (D0h)	Prog/Ers Suspend (B0h)	Prog/Ers Resume (D0h)	Read Status (70h)	Clear Status (50h)
Read Array	“1”	Array	Read Array	Prog.Setup	Ers. Setup	Read Array			Read Sts.	Read Array
Read Status	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Read Elect.Sg.	“1”	Electronic Signature	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Read CFI Query	“1”	CFI	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Prot. Prog. Setup	“1”	Status	Protection Register Program							
Prot. Prog. (continue)	“0”	Status	Protection Register Program continue							
Prot. Prog. (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Prog. Setup	“1”	Status	Program							
Program (continue)	“0”	Status	Program (continue)				Prog. Sus Read Sts	Program (continue)		
Prog. Sus Status	“1”	Status	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Prog. Sus Read Array	“1”	Array	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Prog. Sus Read Elect.Sg.	“1”	Electronic Signature	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Prog. Sus Read CFI	“1”	CFI	Prog. Sus Read Array	Program Suspend to Read Array		Program (continue)	Prog. Sus Read Array	Program (continue)	Prog. Sus Read Sts	Prog. Sus Read Array
Program (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Erase Setup	“1”	Status	Erase Command Error			Erase (continue)	Erase CmdError	Erase (continue)	Erase Command Error	
Erase Cmd.Error	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array
Erase (continue)	“0”	Status	Erase (continue)				Erase Sus Read Sts	Erase (continue)		
Erase Sus Read Sts	“1”	Status	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase Sus Read Array	“1”	Array	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase Sus Read Elect.Sg.	“1”	Electronic Signature	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase Sus Read CFI	“1”	CFI	Erase Sus Read Array	Program Setup	Erase Sus Read Array	Erase (continue)	Erase Sus Read Array	Erase (continue)	Erase Sus Read Sts	Erase Sus Read Array
Erase (complete)	“1”	Status	Read Array	Program Setup	Erase Setup	Read Array			Read Status	Read Array

Note: Cmd = Command, Elect.Sg. = Electronic Signature, Ers = Erase, Prog. = Program, Prot = Protection, Sus = Suspend.

Table 29. Write State Machine Current/Next, sheet 2 of 2.

Current State	Command Input (and Next State)		
	Read Elect.Sg. (90h)	**Read CFI Query (98h)**	**Prot. Prog. Setup (C0h)**
Read Array	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup
Read Status	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup
Read Elect.Sg.	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup
Read CFI Query	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup
Prot. Prog. Setup	Protection Register Program		
Prot. Prog. (continue)	Protection Register Program (continue)		
Prot. Prog. (complete)	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup
Prog. Setup	Program		
Program (continue)	Program (continue)		
Prog. Suspend Read Status	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array
Prog. Suspend Read Array	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array
Prog. Suspend Read Elect.Sg.	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array
Prog. Suspend Read CFI	Prog. Suspend Read Elect.Sg.	Prog. Suspend Read CFI Query	Program Suspend Read Array
Program (complete)	Read Elect.Sg.	Read CFIQuery	Prot. Prog. Setup
Erase Setup	Erase Command Error		
Erase Cmd.Error	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup
Erase (continue)	Erase (continue)		
Erase Suspend Read Ststus	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Erase Suspend Read Array
Erase Suspend Read Array	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Erase Suspend Read Array
Erase Suspend Read Elect.Sg.	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Erase Suspend Read Array
Erase Suspend Read CFI Query	Erase Suspend Read Elect.Sg.	Erase Suspend Read CFI Query	Erase Suspend Read Array
Erase (complete)	Read Elect.Sg.	Read CFI Query	Prot. Prog. Setup

Note: Cmd = Command, Elect.Sg. = Electronic Signature, Prog. = Program, Prot = Protection.

REVISION HISTORY

Table 30. Document Revision History

Date	Version	Revision Details
07-Dec-2004	0.1	First Issue.
07-Feb-2005	0.2	Locations 31h to 34h set to reserved in Table 25., Device Geometry Definition.
16-May-2005	1.0	Datasheet status updated to “Full Datasheet”. Table 25., Device Geometry Definition updated.