Winbond Electronics Corp.

8-BIT MICROCONTROLLER

GENERAL DESCRIPTION

The W78E54 is an 8-bit microcontroller that is functionally compatible with the W78C54, except that the mask ROM is replaced by a flash EEPROM with a size of 16 KB. To facilitate programming and verification, the flash EEPROM inside the W78E54 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E54 microcontroller supplies a wider frequency range than most 8-bit microcontrollers on the market. It is functionally compatible with the industry-standard 80C52 microcontroller series, except that one extra 4-bit bit-addressable I/O port (Port 4) and two additional external interrupts ($\overline{INT2}$, $\overline{INT3}$).

The W78E54 contains four 8-bit bidirectional and bit-addressable I/O ports, three 16-bit timer/counters, and a serial port. These peripherals are supported by a eight-source, two-level interrupt capability. There are 256 bytes of RAM and an 16 KB flash EEPROM for application programs.

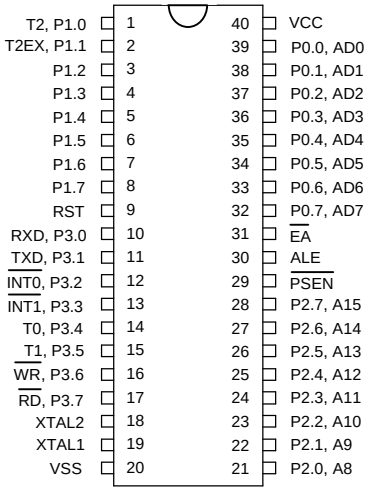
The W78E54 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

FEATURES

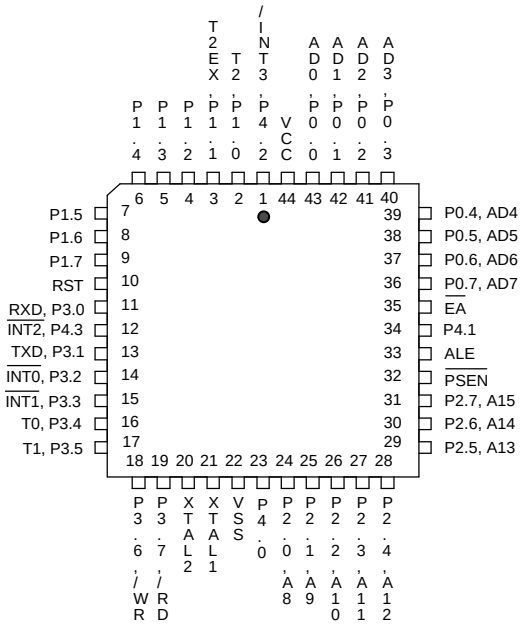
- 8-bit CMOS microcontroller
- Fully static design
- Low standby current at full supply voltage
- DC-40 MHz operation
- 256 bytes of on-chip scratchpad RAM
- 16 KB electrically erasable/programmable EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bidirectional ports
- One extra 4-bit bit-addressable I/O port, additional $\overline{INT2}$ / $\overline{INT3}$ *(available on 44-pin PLCC/QFP package)*
- Three 16-bit timer/counters
- One full duplex serial port
- Boolean processor
- Eight-source, two-level interrupt capability
- Built-in power management
- Code protection mechanism
- Packages:
  - DIP 40: W78E54-16/24/40
  - PLCC 44: W78E54P-16/24/40
  - QFP 44: W78E54F-16/24/40
  - TQFP 44: W78E54M-16/24/40

PIN CONFIGURATIONS

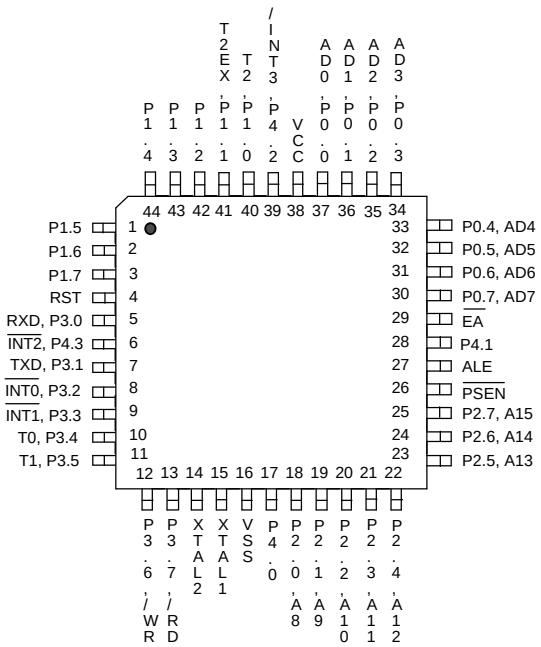
40-Pin DIP (W78E54)



44-Pin PLCC (W78E54P)



44-Pin QFP/TQFP (W78E54F/W78E54M))



PIN DESCRIPTION

The W78E54 has two operating modes, normal and flash. In normal mode, the W78E54 corresponds to the W78C54. In flash mode, the user (the maker of the flash EEPROM writer) can access the flash EEPROM.

P0.7- P0.0 Port 0, Bits 7- 0

MODE	DESCRIPTION
Normal	Port 0, Bits 0 through 7. Port 0 is a bidirectional I/O port. This port also provides a multiplexed low order address/data bus during accesses to external memory.
Flash	This port provides the data bus during access to the flash EEPROM.

P1.7- P1.0 Port 1, Bits 7- 0

MODE	DESCRIPTION
Normal	Port 1, Bits 0 through 7. Port 1 is a bidirectional I/O port with internal pull-ups. Pins P1.0 and P1.1 also serve as T2 (Timer 2 external input) and T2EX (Timer 2 capture/reload trigger), respectively.
Flash	This port provides the low-order address bus during access to the flash EEPROM.

P2.7- P2.0 Port 2, Bits 7- 0

MODE	DESCRIPTION
Normal	Port 2, Bits 0 through 7. Port 2 is a bidirectional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory..
Flash	This port provides the high-order address bus during access to the flash EEPROM.

P3.7- P3.0 Port 3, Bits 7- 0

MODE	DESCRIPTION
Normal	Port 3, Bits 0 through 7. Port 3 is a bidirectional I/O port with internal pull-ups. All bits have alternate functions.
Flash	P3.3–P3.0 and P3.7–P3.6 are the flash mode configuration pins, Input. P3.3–P3.0 and P3.7–P3.6 are configured to select or execute the flash operations. For details, see *Flash Operations*.

P4.3- P4.0 Port 4, Bits 3- 0 *(available on 44-pin PLCC/QFP package)*

MODE	DESCRIPTION
Normal	Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

Flash	No function in this mode.

$\overline{EA}$/VPP

MODE	DESCRIPTION
Normal	$\overline{EA}$, External Access, Input, active low. This pin forces the processor to execute a program from the external ROM. When the internal flash EEPROM is accessed as in the W78C54, this pin should be kept high.
Flash	VPP, Program Power supply pin, Input. This pin accepts the high voltage (12V) needed for programming the flash EEPROM.

RST

MODE	DESCRIPTION
Normal	RST, Reset, Input, active high. This pin resets the processor. It must be kept high for at least two machine cycles in order to be recognized by the processor.
Flash	Flash mode configuration pin, Input, active high. RST is used to configure the flash operations. For details, see *Flash Operations*.

ALE

MODE	DESCRIPTION
Normal	ALE, Address Latch Enable, Output, active high. ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. A single ALE pulse is skipped during external data memory accesses. ALE goes to a high impedance state with a weak pull-up during reset state.
Flash	Flash mode configuration pin, Input, active low. ALE is used to configure the flash operations. For details, see *Flash Operations*.

$\overline{PSEN}$

MODE	DESCRIPTION
Normal	$\overline{PSEN}$, Program Store Enable, Output, active low. This pin enables the external ROM onto the Port 0 address/data bus during fetch and MOVC operations. $\overline{PSEN}$ goes to a high impedance state with a weak pull-up during reset state
Flash	Flash mode configuration pin, Input, active high. $\overline{PSEN}$ is used to configure the flash operations. For details, see *Flash Operations.*

XTAL1

MODE	DESCRIPTION

Normal	Crystal 1. This is the crystal oscillator input. This pin may be driven by an external clock.
Flash	Connect to Vss.

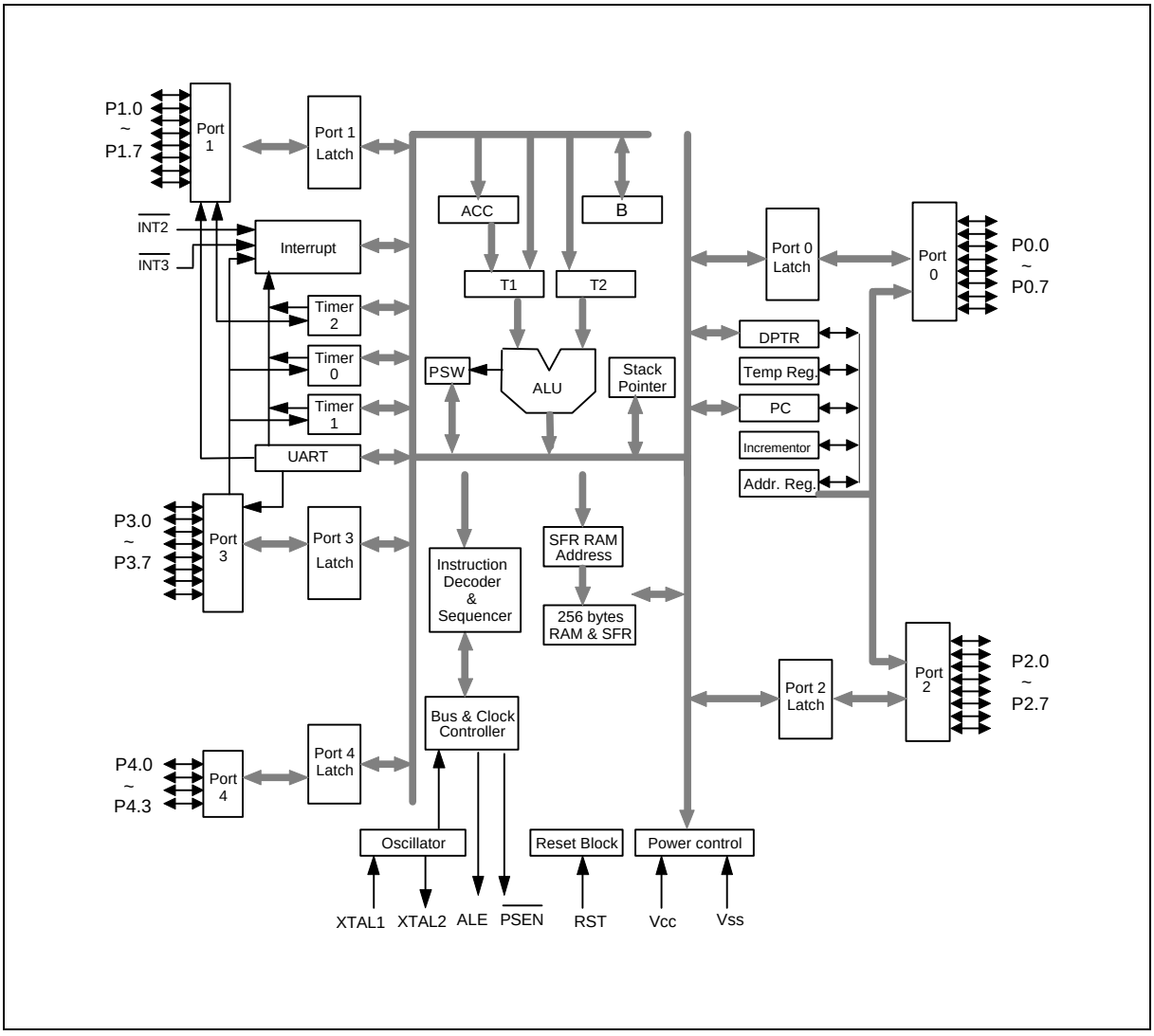
XTAL2

MODE	DESCRIPTION
Normal	Crystal 2. This is the crystal oscillator output. It is the inversion of XTAL1.
Flash	No function in this mode.

VSS, VCC

Power Supplies. These are the chip ground and positive supplies.

BLOCK DIAGRAM


P1.0
~
P1.7
Port 1
Port 1 Latch
INT2
INT3
Interrupt
Timer 2
Timer 0
Timer 1
UART
ACC
B
T1
T2
PSW
ALU
Stack Pointer
Port 0 Latch
Port 0
P0.0
~
P0.7
DPTR
Temp Reg.
PC
Incrementor
Addr. Reg.
P3.0
~
P3.7
Port 3
Port 3 Latch
Instruction Decoder & Sequencer
SFR RAM Address
256 bytes RAM & SFR
Port 2 Latch
Port 2
P2.0
~
P2.7
Bus & Clock Controller
P4.0
~
P4.3
Port 4
Port 4 Latch
Oscillator
Reset Block
Power control
XTAL1
XTAL2
ALE
PSEN
RST
Vcc
Vss

FUNCTIONAL DESCRIPTION

The W78E54 architecture consists of a core controller surrounded by various registers, five general purpose I/O ports, 256 bytes of RAM, three timer/counters, and a serial port. The processor supports 111 different opcodes and references both a 64K program address space and a 64K data storage space.

Timers 0, 1, and 2

Timers 0, 1, and 2 each consist of two 8-bit data registers. These are called TL0 and TH0 for Timer 0, TL1 and TH1 for Timer 1, and TL2 and TH2 for Timer 2. The TCON and TMOD registers provide control functions for timers 0 and 1. The T2CON register provides control functions for Timer 2. RCAP2H and RCAP2L are used as reload/capture registers for Timer 2.

The operations of Timer 0 and Timer 1 are the same as in the W78C51. Timer 2 is a special feature of the W78E54: it is a 16-bit timer/counter that is configured and controlled by the T2CON register. Like Timers 0 and 1, Timer 2 can operate as either an external event counter or as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

Clock

The W78E54 is designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used. This makes the W78E54 relatively insensitive to duty cycle variations in the clock.

Crystal Oscillator

The W78E54 incorporates a built-in crystal oscillator. To make the oscillator work, a crystal must be connected across pins XTAL1 and XTAL2. In addition, a load capacitor must be connected from each pin to ground, and a resistor must also be connected from XTAL1 to XTAL2 to provide a DC bias when the crystal frequency is above 24 MHz.

External Clock

An external clock should be connected to pin XTAL1. Pin XTAL2 should be left unconnected. The XTAL1 input is a CMOS-type input, as required by the crystal oscillator. As a result, the external clock signal should have an input one level of greater than 3.5 volts.

Power Management

Idle Mode

The idle mode is entered by setting the IDL bit in the PCON register. In the idle mode, the internal clock to the processor is stopped. The peripherals and the interrupt logic continue to be clocked. The processor will exit idle mode when either an interrupt or a reset occurs.

Power-down Mode

When the PD bit of the PCON register is set, the processor enters the power-down mode. In this mode all of the clocks are stopped, including the oscillator. The only way to exit power-down mode is by a reset.

Reset

The external RESET signal is sampled at S5P2. To take effect, it must be held high for at least two machine cycles while the oscillator is running.

An internal trigger circuit in the reset line is used to deglitch the reset line when the W78E54 is used with an external RC network. The reset logic also has a special glitch removal circuit that ignores glitches on the reset line.

During reset, the ports are initialized to FFH, the stack pointer to 07H, PCON (with the exception of bit 4) to 00H, and all of the other SFR registers except SBUF to 00H. SBUF is not reset.

Option Setting

Users write programs into the W78E54 by using the Winbond proprietary writer. The writer programs the data into an internal 16 KB region and reads the data back for verification. After confirming that the program is correct, the user can lock the data so that they can no longer be read.

Lock Bit

This bit is used to protect the customer data in the W78E54. It may be turned on after the programmer finishes the programming and verify sequence. Once this bit is set to logic 0, no flash data can be accessed again.

MOVC Execute

This bit is used to restrict the region accessible to the MOVC instruction. It can prevent the program from being downloaded using this instruction if the program needs to jump outside to get data. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code in the external memory, but it will not be able to access code in the internal memory. A MOVC instruction in internal program memory space will always be able to access code in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

New Defined Peripheral

In order to be more suitable for I/O, an extra 4-bit bit-addressable port P4 and two external interrupt $\overline{INT2}$, $\overline{INT3}$ has been added to either the PLCC or QFP 44 pin package. And description follows:

1. $\overline{INT2}$/ $\overline{INT3}$

Two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupt 0 and 1 in the standard 80C52. The functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the standard 80C52. Its address is at 0C0H. To set/clear bits in the XICON register, one can use the "SETB (/CLR) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON.

*****XICON - external interrupt control (C0H)**

PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

PX3: External interrupt 3 priority high if set

EX3: External interrupt 3 enable if set

IE3: If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced

IT3: External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software

PX2: External interrupt 2 priority high if set

EX2: External interrupt 2 enable if set

IE2: If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced

IT2: External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Eight-source interrupt informations:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

2. PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$, $\overline{INT3}$).

Example:

```
P4      REG   0D8H
MOV     P4, #0AH     ; Output data "A" through P4.0–P4.3.
MOV     A, P4        ; Read P4 status to Accumulator.
SETB    P4.0         ; Set bit P4.0
CLR     P4.1         ; Clear bit P4.1
```

3. Reduce EMI Emission

Because of the large on-chip flash EEPROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the

AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space..

The AO bit in the AUXR register, when set, disables the ALE output.

*****AUXR - Auxiliary register (8EH)**

-	-	-	-	-	-	-	AO

AO: Turn off ALE output.

4. Power-off Flag

*****PCON - Power control (87H)**

SMOD	**-**	-	**POF**	GF1	GF0	PD	IDL

SMOD: Double baud rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2, 3.

POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.

GF1, GF0: These two bits are general-purpose flag bits for the user.

PD: Power down mode bit. Set it to enter power down mode.

IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when V_{DD} has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.

Flash Operations

In normal operation, the W78E54 is functionally compatible with the W78C54. In the flash operating mode, the flash EEPROM can be programmed and verified repeatedly. Once the code inside the flash EEPROM is confirmed, the code can be protected. The flash EEPROM and the operations on it are described below.

All of the operations are configured by the pins RST, ALE, $\overline{PSEN}$, A9CTRL (P3.0), A13CTRL (P3.1), A14CTRL (P3.2), OECTRL (P3.3), $\overline{CE}$ (P3.6), $\overline{OE}$ (P3.7), A0 (P1.0) and V_{PP} ($\overline{EA}$). In these operations, A15 to A0 (P2.7 to P2.0, P1.7 to P1.0) and D7 to D0 (P0.7 to P0.0) serve as the address and data bus, respectively.

Read Operation

This operation enables customers to read their codes and the option bits. The data will not be valid if the lock bit is programmed to low.

Program Operation

This operation is used to program data to the flash EEPROM and the option bits. Programming is initiated when V_{PP} reaches V_{CP} (12.5V) level, $\overline{CE}$ is set to low, and $\overline{OE}$ is set to high.

Program Verify Operation

All data must be checked after programming. This operation should be performed after each byte is programmed, and it will ensure a substantial program margin.

OPERATION	P3.0 (A9 CTRL)	P3.1 (A13 CTRL)	P3.2 (A14 CTRL)	P3.3 (OE CTRL)	P3.6 ($\overline{CE}$)	P3.7 ($\overline{OE}$)	$\overline{EA}$ (V_{PP})	P2, P1 (A15 TO A0)	P0 (D7 TO D0)	NOTES
Read	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Address	Data Out	1, 2
Program	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{CP}	Address	Data In	1, 2
Program Verify	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{CP}	Address	Data Out	3

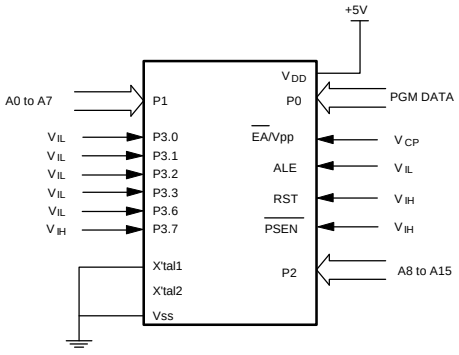
Notes:

1. During all of these operations, RST = V_{IH}, ALE = V_{IL}, and $\overline{PSEN}$ = V_{IH}.
2. V_{CP} = 12V, V_{IH} = V_{DD}, V_{IL} = Vss.
3. The program verify operation should follow the programming operaion.

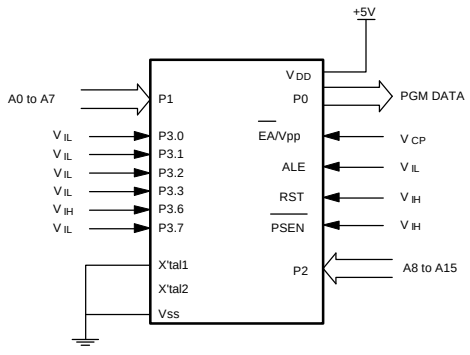
ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{ST}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.



Programming Configuration



Programming Verification

DC CHARACTERISTICS

(V_{DD}-V_{SS} = 5V ±10%, T_A = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Operating Voltage	V_{DD}	4.5	5.5	V	
Operating Current	I_{DD}	-	20	mA	No load V_{DD} = 5.5V
Idle Current	I_{IDLE}	-	6	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	50	µA	Power-down mode V_{DD} = 5.5V
Input Current P1, P2, P3, P4	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or V_{DD}
Input Current RST	I_{IN2}	-10	+300	µA	V_{DD} = 5.5V 0 < V_{IN} < V_{DD}
Input Leakage Current P0, /EA	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V <V_{IN} < V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3, P4	I_{TL} [*4]	-500	-200	µA	V_{DD} = 5.5V V_{IN} =2.0V
Input Low Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*4]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
Input High Voltage P0, P1, P2, P3, P4, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Input High Voltage XTAL1 [*4]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Output Low Voltage P1, P2, P3, P4	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +2 mA

DC Characteristics, continued

PARAMETER	SYM.	SPECIFICATION		UNIT	TEST CONDITIONS
		MIN.	MAX.		
Output Low Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +4mA
Sink Current P1, P2, P3, P4	I_{SK1}	4	12	mA	V_{DD} = 4.5V Vs = 0.45V
Sink Current P0, ALE, $\overline{PSEN}$	I_{SK2}	10	20	mA	V_{DD} = 4.5V Vs = 0.45V
Output High Voltage P1, P2, P3, P4	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -100 µA
Output High Voltage P0, ALE, $\overline{PSEN}$ [*3]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -400 µA
Source Current P1, P2, P3, P4	I_{SR1}	-120	-250	µA	V_{DD} = 4.5V Vs = 2.4V
Source Current P0, ALE, $\overline{PSEN}$	I_{SR2}	-8	-14	mA	V_{DD} = 4.5V Vs = 2.4V

Notes:

1. RST pin is a Schmitt trigger input. RST has internal pull-low resistors of about 30 KΩ.

3. P0, ALE and /PSEN are tested in the external access mode.

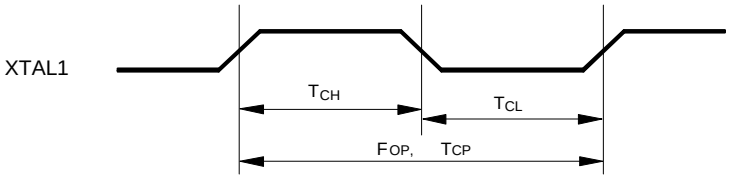
4. XTAL1 is a CMOS input.

5. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} approximates to 2V.

AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.8 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	FOP	0	-	40	MHz	1
Clock Period	TCP	25	-	-	nS	2
Clock High	TCH	10	-	-	nS	3
Clock Low	TCL	10	-	-	nS	3

Notes:
1. The clock may be stopped indefinitely in either state.
2. The TCP specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 TCP -Δ	-	-	nS	4
Address Hold from ALE Low	TAAH	1 TCP -Δ	-	-	nS	1, 4
ALE Low to $\overline{\text{PSEN}}$ Low	TAPL	1 TCP -Δ	-	-	nS	4
$\overline{\text{PSEN}}$ Low to Data Valid	TPDA	-	-	2 TCP	nS	2
Data Hold after $\overline{\text{PSEN}}$ High	TPDH	0	-	1 TCP	nS	3
Data Float after $\overline{\text{PSEN}}$ High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP -Δ	2 TCP	-	nS	4
$\overline{\text{PSEN}}$ Pulse Width	TPSW	3 TCP -Δ	3 TCP	-	nS	4

Notes:
1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.
2. Memory access time is 3 TCP.
3. Data have been latched internally prior to $\overline{\text{PSEN}}$ going high.
4. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Read Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
ALE Low to $\overline{\text{RD}}$ Low	TDAR	3 TCP -Δ	-	3 TCP +Δ	nS	1, 2
$\overline{\text{RD}}$ Low to Data Valid	TDDA	-	-	4 TCP	nS	1
Data Hold from $\overline{\text{RD}}$ High	TDDH	0	-	2 TCP	nS	
Data Float from $\overline{\text{RD}}$ High	TDDZ	0	-	2 TCP	nS	
$\overline{\text{RD}}$ Pulse Width	TDRD	6 TCP -Δ	6 TCP	-	nS	2

Notes:
1. Data memory access time is 8 TCP.
2. "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Data Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
ALE Low to $\overline{WR}$ Low	TDAW	3 TCP -Δ	-	3 TCP +Δ	nS
Data Valid to $\overline{WR}$ Low	TDAD	1 TCP -Δ	-	-	nS
Data Hold from $\overline{WR}$ High	TDWD	1 TCP -Δ	-	-	nS
$\overline{WR}$ Pulse Width	TDWR	6 TCP -Δ	6 TCP	-	nS

Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

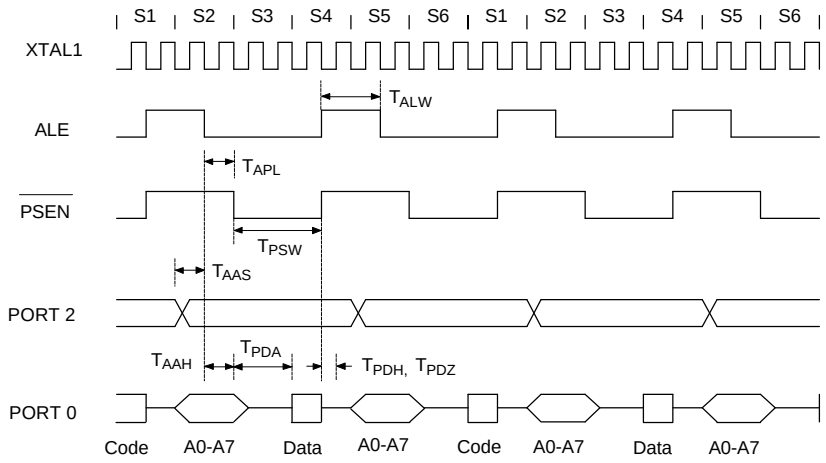
Program Operation

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	TVPS	2.0	-	-	µS
Data Setup Time	TDS	2.0	-	-	µS
Data Hold Time	TDH	2.0	-	-	µS
Address Setup Time	TAS	2.0	-	-	µS
Address Hold Time	TAH	0	-	-	µS
$\overline{CE}$ Program Pulse Width for Program Operation	TPWP	295	300	305	µS
$\overline{CE}$ Program Pulse Width for Program Operation	TOPWP	295	300	305	µS
OECTRL Setup Time	TOCS	2.0	-	-	µS
OECTRL Hold Time	TOCH	2.0	-	-	µS
$\overline{OE}$ Setup Time	TOES	2.0	-	-	µS
$\overline{OE}$ High to Output Float	TDFP	0	-	130	nS
Data Valid from $\overline{OE}$	TOEV	-	-	150	nS

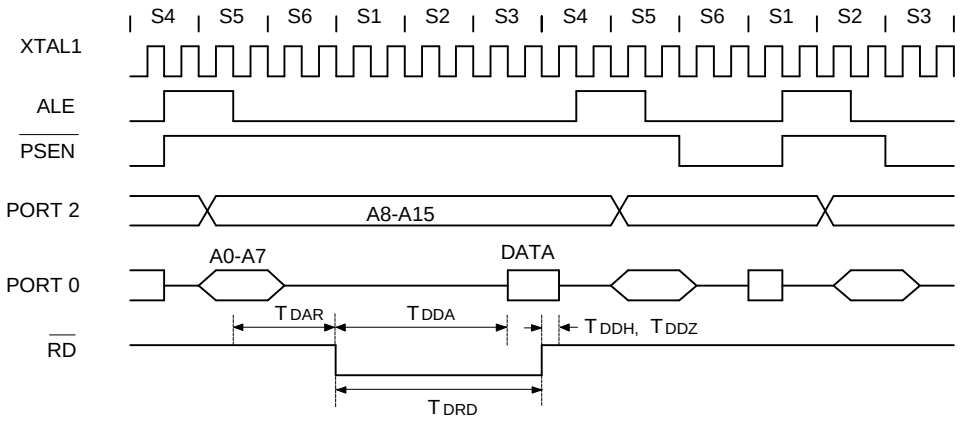
Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the $\overline{PSEN}$ pin must pull in VIH status.

TIMING WAVEFORMS

Program Fetch Cycle

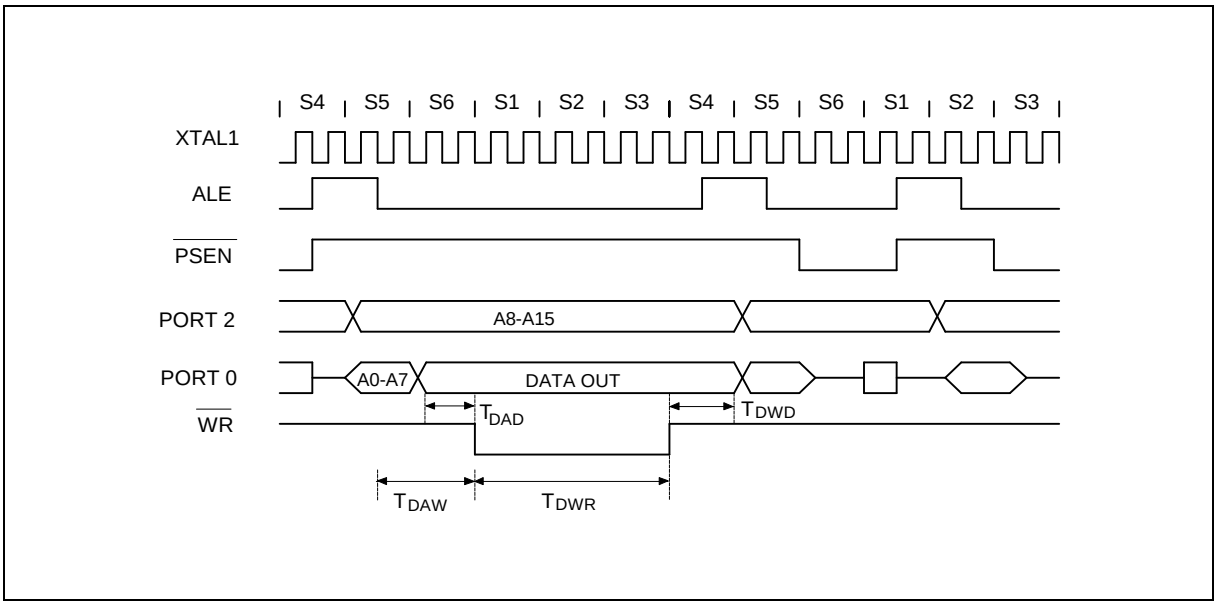


Data Read Cycle

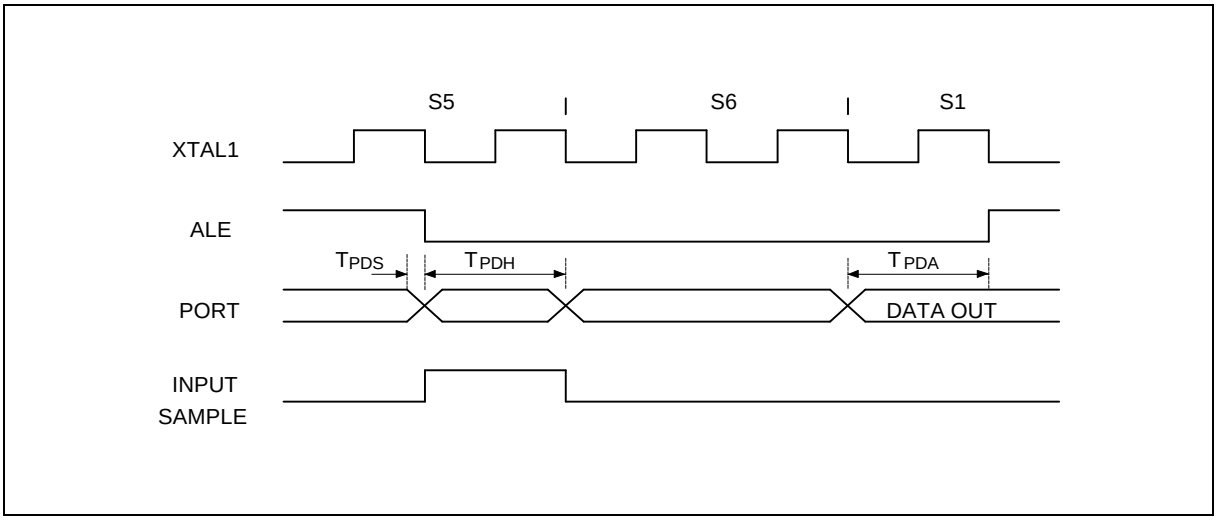


Timing Waveforms, continued

Data Write Cycle

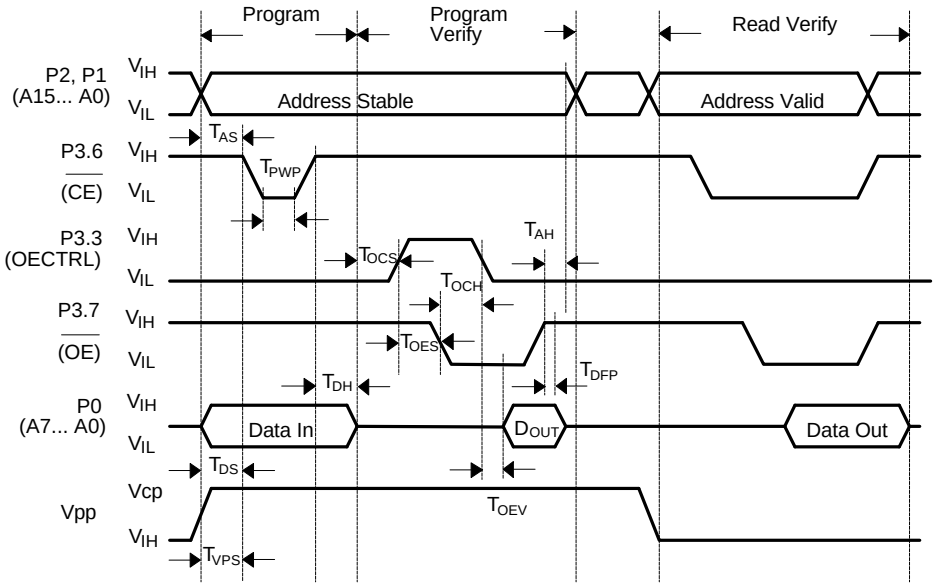


Port Access Cycle



Timing Waveforms, continued

Program Operation



TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

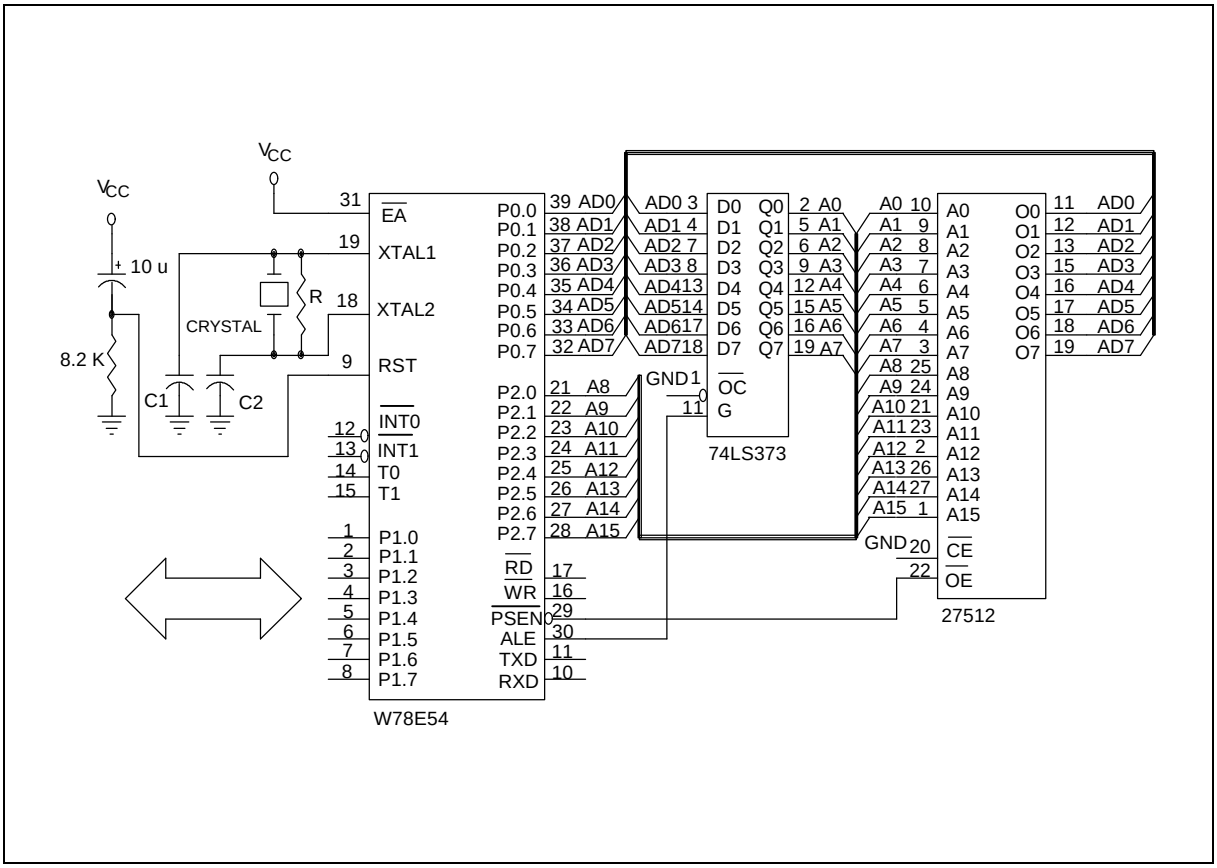


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
24 MHz	15P	15P	-
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	4.7K

Above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

Typical Application Circuits, continued

Expanded External Data Memory and Oscillator

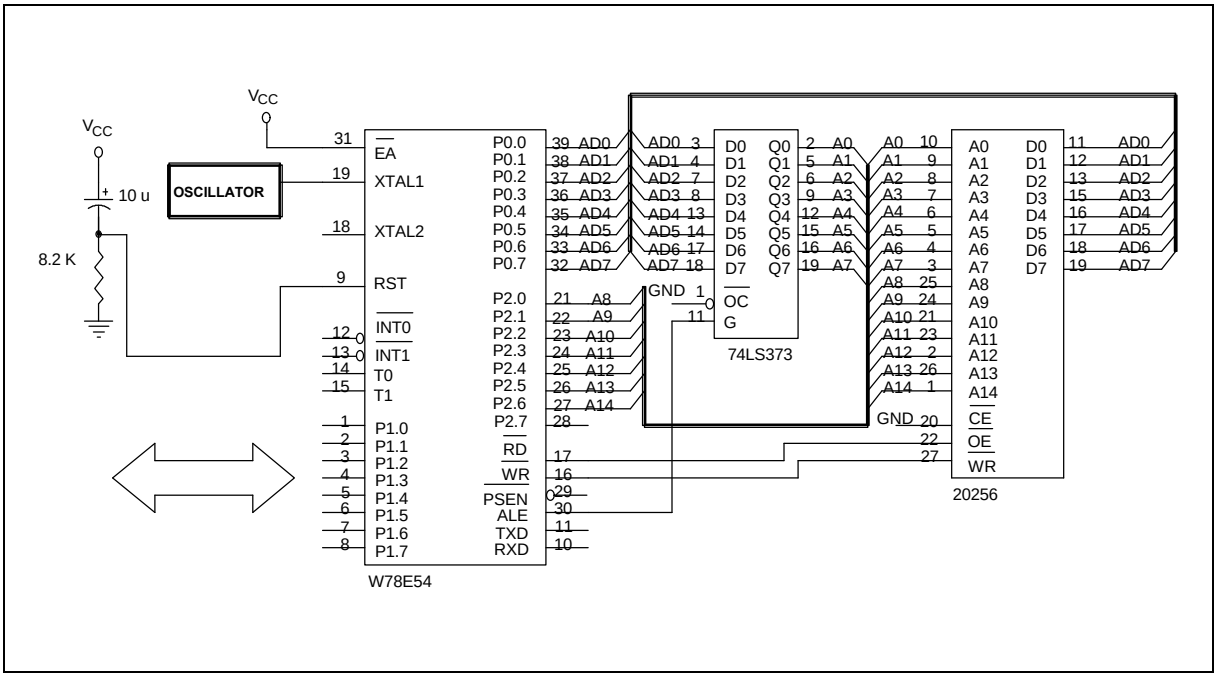
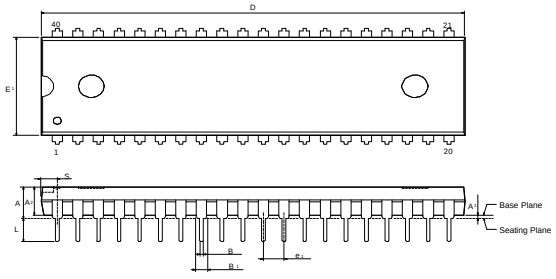


Figure B

PACKAGE DIMENSIONS

40-pin DIP

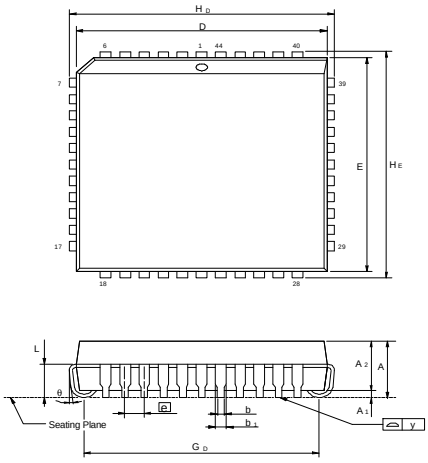


Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.210	—	—	5.334
A1	0.010	—	—	0.254	—	—
A2	0.150	0.155	0.160	3.81	3.937	4.064
B	0.016	0.018	0.022	0.406	0.457	0.559
B1	0.048	0.050	0.054	1.219	1.27	1.372
c	0.008	0.010	0.014	0.203	0.254	0.356
D	—	2.055	2.070	—	52.20	52.58
E	0.590	0.600	0.610	14.986	15.24	15.494
E1	0.540	0.545	0.550	13.72	13.84	13.97
e1	0.090	0.100	0.110	2.286	2.54	2.794
L	0.120	0.130	0.140	3.048	3.302	3.556
a	0	—	15	0	—	15
eA	0.630	0.650	0.670	16.00	16.51	17.01
S	—	—	0.090	—	—	2.286

Notes:
1. Dimension D Max. & S include mold flash or tie bar burrs.
2. Dimension E1 does not include interlead flash.
3. Dimension D & E1 include mold mismatch and are determined at the mold parting line.
4. Dimension B1 does not include dambar protrusion/intrusion.
5. Controlling dimension: Inches.
6. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

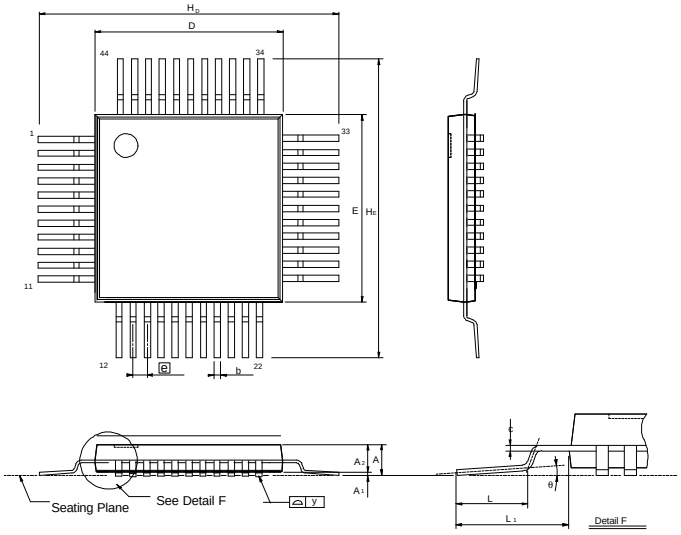
44-pin PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-pin QFP

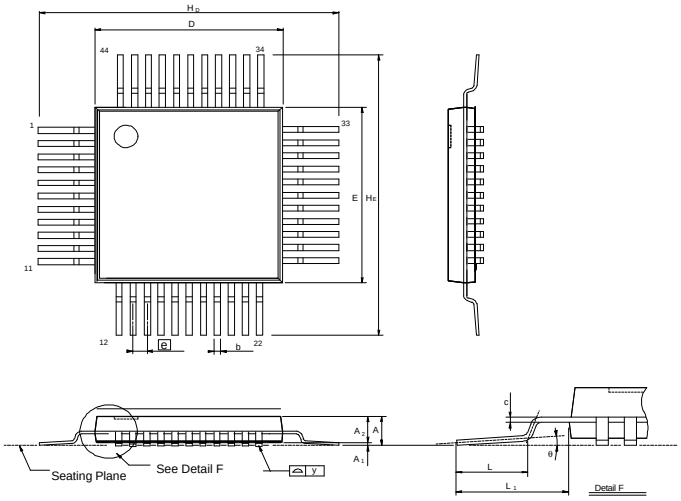


Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

Package Dimensions, continued

44-pin TQFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.047	---	---	1.20
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.0039	0.013	0.015	0.22	0.32	0.38
c	0.004	---	0.008	0.090	---	0.200
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.468	0.472	0.476	11.90	12.00	12.10
H_E	0.468	0.472	0.476	11.90	12.00	12.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	---	0.039	---	---	1.00	---
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:

1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.

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