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**W81E381D/W81E381AD**

**FULL SPEED USB INTEGRATED MICROCONTROLLER**

**W81E381D/W81E381AD**  
**Full Speed USB Integrated**  
**Microcontroller**



# W81E381D/W81E381AD



## W81E381D/AD Data Sheet Revision History

|    | Pages   | Dates   | Version | Version on Web | Main Contents   |
|----|---|---------|---------|----------------|---|
| 1  | n.a.  | 03/2001 | 0.50    | n.a.           | First published   |
| 2  | P.9, P.11, P.14,<br>P.35, P.36, P.47,<br>P.48 | 09/2001 | 0.51    | n.a.           | 1. Modify pin function of SCIO & SCCLK<br>2. Revise register description of SCCR (AC) and SCECR (AD)<br>3. Revise the USB register descriptions |
| 3  | P.14, P.53, P.54                              | 01/2002 | 0.52    | n.a.           | 1. Revise register description of CHPCON (CF)<br>2. Modify the description of SFRCN & CHPCON  |
| 4  |   |         |         |                |   |
| 5  |   |         |         |                |   |
| 6  |   |         |         |                |   |
| 7  |   |         |         |                |   |
| 8  |   |         |         |                |   |
| 9  |   |         |         |                |   |
| 10 |   |         |         |                |   |

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## TABLE OF CONTENTS

|   |           |
|---|-----------|
| <b>1. General Descriptions:</b> .....                               | <b>5</b>  |
| <b>2. FEATURES:</b> .....   | <b>6</b>  |
| <b>3. Pin configuration</b> .....                                   | <b>7</b>  |
| <b>3.1 W81E381D 48-pin LQFP PINOUT</b> .....                        | <b>7</b>  |
| <b>3.2 W81E381AD 100-pin LQFP PINOUT</b> .....                      | <b>10</b> |
| <b>4. Programming interface</b> .....                               | <b>13</b> |
| <b>4.1 Register map</b> .....                                       | <b>13</b> |
| <b>4.2 FLASH Category – Descriptions Summary</b> .....              | <b>14</b> |
| <b>4.3 SC Category - Descriptions Summary</b> .....                 | <b>14</b> |
| <b>4.4 USB Category - Descriptions Summary</b> .....                | <b>15</b> |
| <b>4.5 Individual register description</b> .....                    | <b>16</b> |
| 4.5.1 Register Descriptions - USB Power Control Registers (E7)..... | 16        |
| 4.5.2 Register Descriptions - USB Interrupt System SFRs (A2) .....  | 18        |
| 4.5.3 Register Descriptions - USB Interrupt System SFRs (C0) .....  | 19        |
| 4.5.4 Register Descriptions - USB Interrupt System SFRs (B1) .....  | 20        |
| 4.5.4 Register Descriptions - USB Interrupt System SFRs (B1) .....  | 20        |
| 4.5.5 Register Descriptions - USB Function SFRs (E1) .....          | 21        |
| 4.5.6 Register Descriptions - USB Function SFRs (F1) .....          | 23        |
| 4.5.7 Register Descriptions - USB Function SFRs (8F) .....          | 24        |
| 4.5.8 Register Descriptions - USB Function SFRs (E6) .....          | 26        |
| 4.5.9 Register Descriptions - USB Function SFRs (E4) .....          | 27        |
| 4.5.10 Register Descriptions - USB Function SFRs (E3) .....         | 28        |
| 4.5.11 Register Descriptions - USB Function SFRs (E5) .....         | 30        |
| 4.5.12 Register Descriptions - USB Function SFRs (E2) .....         | 32        |
| 4.5.13 Register Descriptions - USB Function SFRs (F6) .....         | 34        |
| 4.5.14 Register Descriptions - USB Function SFRs (F4) .....         | 35        |
| 4.5.15 Register Descriptions - USB Function SFRs (F3) .....         | 36        |
| 4.5.16 Register Descriptions - USB Function SFRs (F5) .....         | 38        |
| 4.5.17 Register Descriptions - USB Function SFRs (F2) .....         | 40        |
| 4.5.18 Register Descriptions - USB Device SFRs (B7).....            | 42        |
| 4.5.19 Register Descriptions - USB Device SFRs (BF).....            | 43        |
| 4.5.20 Register Descriptions - SC Interrupt SFRs (AA).....          | 44        |
| 4.5.21 Register Descriptions - SC Interrupt SFRs (AB) .....         | 45        |
| 4.5.22 Register Descriptions - SC Control SFRs (A3).....            | 46        |
| 4.5.24 Register Descriptions - SC Control SFRs (AC).....            | 47        |
| 4.5.25 Register Descriptions - SC Control SFRs (AD).....            | 48        |
| 4.5.26 Register Descriptions - SC Control SFRs (AE, A4) .....       | 49        |
| 4.5.27 Register Descriptions - SC Control SFRs (A5).....            | 50        |
| 4.5.28 Register Descriptions - SC Data SFRs (A6, A7) .....          | 51        |
| 4.5.29 Register Descriptions – ISP Registers (C4, C5).....          | 52        |
| 4.5.30 Register Descriptions – ISP Registers (C6, C7).....          | 53        |

# W81E381D/W81E381AD



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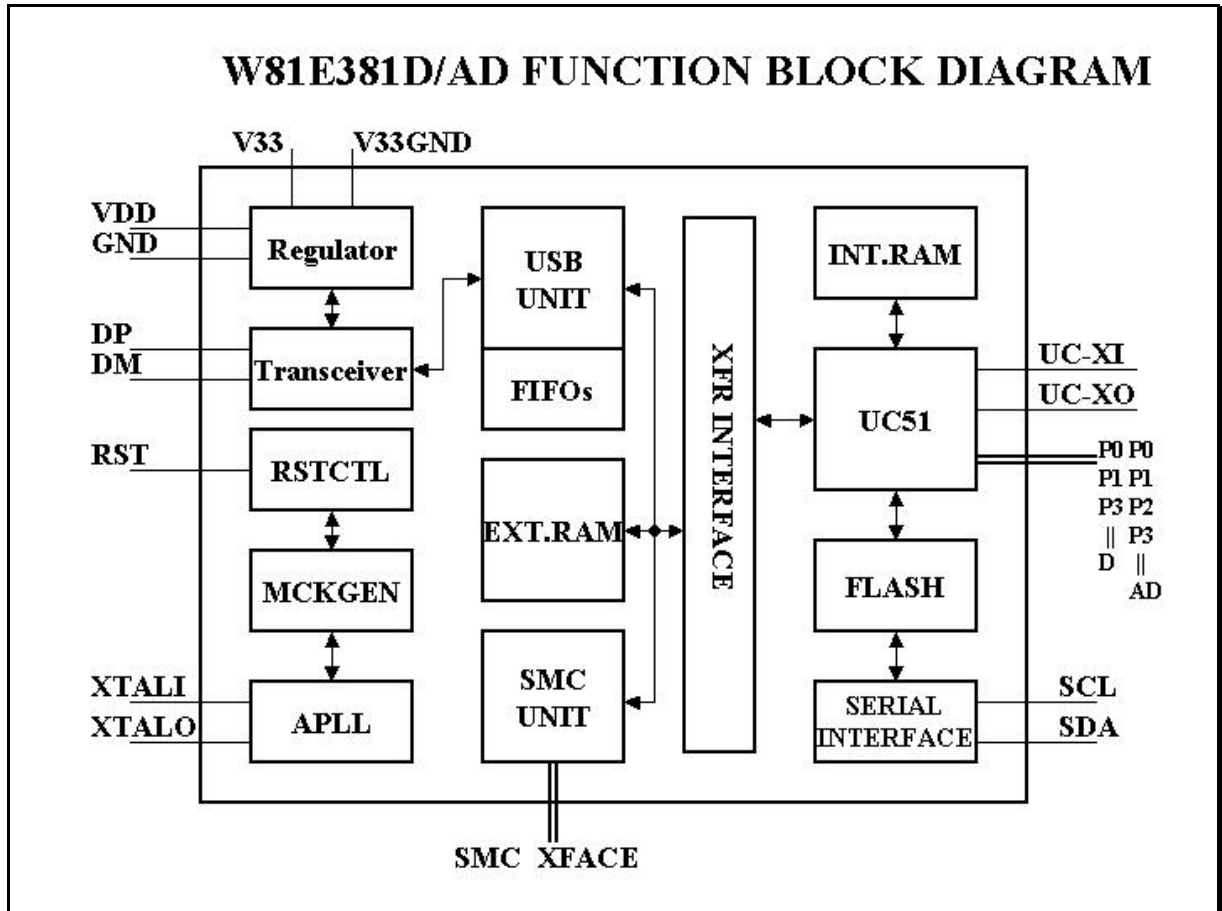
|            |   |           |
|------------|---|-----------|
| 4.5.31     | Register Descriptions – uC Control Registers (CF).....                | 54        |
| 4.5.32     | Register Descriptions – uC Control Registers (D4, D5).....            | 55        |
| <b>4.6</b> | <b>MTP-ROM PROGRAMMING .....</b>                                      | <b>56</b> |
| <b>5.</b>  | <b>Security.....</b>  | <b>57</b> |
| <b>6.</b>  | <b>Electrical Characteristics .....</b>                               | <b>58</b> |
| <b>7.</b>  | <b>Mechanical information .....</b>                                   | <b>59</b> |
| <b>7.1</b> | <b>W81E381D 48 LQFP (7x7x1.4mm footprint 2.0mm) PACKAGE .....</b>     | <b>59</b> |
| <b>7.2</b> | <b>W81E381AD 100 LQFP (14x14x1.4 mm footprint 2.0mm) PACKAGE.....</b> | <b>60</b> |
| <b>8.</b>  | <b>TYPICAL APPLICATION.....</b>                                       | <b>61</b> |
| <b>8.1</b> | <b>W81E381D reference schematic .....</b>                             | <b>61</b> |
| <b>8.2</b> | <b>W81E381AD reference schematic .....</b>                            | <b>62</b> |

# W81E381D/W81E381AD



## 1. GENERAL DESCRIPTIONS:

The W81E381 is 8052-based USB device with 20 Kbytes flash memory. By integrating the USB1.1 transceiver, SIE, enhanced 8032 code, 20K Flash memory, extra 256 Byte RAM, power regulator, and general purpose I/O in single chip, W81E381D/W81E381AD creates a very low cost-effective solution that provides superior time-to-market advantages. The GPIO provides an easy interface to popular interface, such as ATAPI, EPP, RS232, MCU and DSP interface.



## 2. FEATURES:

- Fully compliant with the Universal Serial Bus Specification version 1.1.
- Support USB Suspend and Resume operation for power-down standby.
- Support USB remote wake up function.
- Embedded microprocessor--8052 with extra 256Bytes RAM for data processing/storage, 20 Kbytes of In-System Programmable Flash memory.
- Internal generated 12MHz clock for 8052 use (the same as standard 8052 uses 24 MHz clock outside)
- External and separated 8052 clock input supported
- 6 clock per instruction 8052 core
- Flash support 512Byte erase block
- Software setting, 2KByte block programmable write protection for Flash memory
- 6-Mhz crystal/oscillator input for both Full speed application with limited EMI affection
- Support smart card interface, including serial interface memory card, and SCIO & SCCLK pins could be programmed as GPIO pins by registers setting
- Built-in 3.3V power regulator for single 5V power operation
- Internal PLL for USB and SC requirements
- Support one Control endpoint for command (8 bytes), and four endpoints 1, 2, 3, 4 (Bulk In, Bulk Out Interrupt In, and Interrupt Out) for data.
  - BulkIn, BulkOut with 16 bytes FIFO
  - InterruptIn, InterruptOut with 8 bytes FIFO
- W81E381D: 48LQFP package
- W81E381AD: 100LQFP package

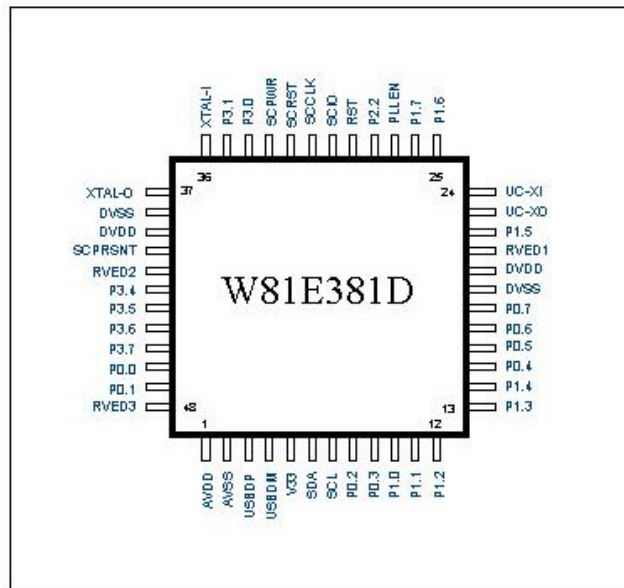
### Ordering Information

| Part Number | Package Type | Production Flow          |
|-------------|--------------|--------------------------|
| W81E381D    | 48-PIN LQFP  | Commercial, 0°C to +70°C |
| W81E381AD   | 100-PIN LQFP | Commercial, 0°C to +70°C |

# W81E381D/W81E381AD

## 3. PIN CONFIGURATION

### 3.1 W81E381D 48-pin LQFP PINOUT



# W81E381D/W81E381AD



## 3.1.1 48- pin LQFP package description

| SYMBOL            | TYPE  | PIN NO                            | DESCRIPTIONS  |
|-------------------|-------|-----------------------------------|---|
| <b>USB Pins</b>   |       |                                   |   |
| AVDD              | PWR   | 1                                 | Analog 5V power supply  |
| AVSS              | PWR   | 2                                 | Analog 5V power ground  |
| V33               | PWR   | 5                                 | USB DC power 3.3V output.   |
| D+                | I/O   | 3                                 | USB signal (+)  |
| D-                | I/O   | 4                                 | USB signal (-)  |
| XTALI             | I     | 36                                | Crystal input. Use 6M Hz crystal. A 6 MHz clock source may also be used.  |
| XTALO             | O     | 37                                | Crystal output.   |
| <b>Extra Pins</b> |       |                                   |   |
| PLEN              | I     | 27                                | PLL enable pin; Schmitt-trigger pull up input   |
| <b>uC Pins</b>    |       |                                   |   |
| RVED1-3           | X     | 21,41,<br>48                      | Reserved pins. Leave these pins floating.   |
| RST               | I L   | 29                                | RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.   |
| P0.0–P0.7         | I/O D | 46,47,<br>8,9,<br>15,16,<br>17,18 | PORT 0: Function is the same as that of the standard 8052.  |
| P1.0              | I/O   | 10                                | It is a high drive I/O pad. Used as a GPIO pin for memory-type SC   |
| P1.1              | I/O   | 11                                | It is a high drive I/O pad. Used as a GPIO pin for memory-type SC   |
| P1.2              | I/O   | 12                                | Used as a GPIO pin for memory-type SC   |
| P1.3              | I/O   | 13                                | Used as a GPIO pin for memory-type SC   |
| P1.4              | I/O   | 14                                | Used as a GPIO pin for memory-type SC   |
| P1.5              | I/O   | 22                                | Used as a GPIO pin for memory-type SC   |
| P1.6              | I/O   | 25                                | GPIO & remote wakeup pin  |
| P1.7              | I/O   | 26                                | GPIO & external interrupt pin   |
| P2.2              | I/O H | 28                                | It's a bi-directional I/O port with internal pull-ups. It can be programmed to be an output-latched port like an on-chip 74373, or a buffer input port like an on-chip 74244. |



# W81E381D/W81E381AD



## 3.1.1 48-PIN LQFP package DESCRIPTION, continued

| SYMBOL                        | TYPE    | PIN NO          | DESCRIPTIONS   |
|-------------------------------|---------|-----------------|--|
| P3.0–P3.1                     | I/O H   | 34,35           | PORT 3: Function is the same as that of the standard 8052. |
| P3.4–P3.7                     | I/O H   | 42,43,<br>44,45 | PORT 3: Function is the same as that of the standard 8052. |
| UC-XI                         | I       | 24              | uC Crystal input.  |
| UC-XO                         | O       | 23              | uC Crystal output.   |
| <b>Power Pins</b>             |         |                 |  |
| VSS                           | PWR     | 19,38           | GROUND: ground potential.                                  |
| VDD                           | PWR     | 20,39           | POWER SUPPLY: Supply voltage for operation.                |
| <b>Serial Interface</b>       |         |                 |  |
| SDA                           | I/O     | 6               | Data input/output of serial interface                      |
| SCL                           | I       | 7               | Clock input of serial interface                            |
| <b>Smart Card Reader Pins</b> |         |                 |  |
| SCPWR                         | O       | 33              | Smart card power supplier enable pin                       |
| SCIO                          | I/O     | 30              | Smart card serial data input/output pin or GPIO pin        |
| SCCLK                         | O (I/O) | 31              | Smart card clock output (default 3M Hz) or GPIO pin        |
| SCRST                         | O       | 32              | Smart card reset signal                                    |
| SCPRSNT                       | I       | 40              | Smart card existed indicator. Schmitt-trigger input        |

\*Note: TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain, PWR: Power pins, X: Floating



# W81E381D/W81E381AD



## 3.2.1 100-pin LQFP package description

| SYMBOL                        | TYPE    | PIN NO | DESCRIPTIONS   |
|-------------------------------|---------|--------|--|
| <b>USB Pins</b>               |         |        |  |
| AVDD                          | PWR     | 1      | Analog 5V power supply   |
| AVSS                          | PWR     | 2, 3   | Analog 5V power ground   |
| V33                           | PWR     | 6      | USB DC power 3.3V output.  |
| D+                            | I/O     | 4      | USB signal (+)   |
| D-                            | I/O     | 5      | USB signal (-)   |
| XTALI                         | I       | 79     | Crystal input. Use 6MHz crystal. A 6MHz clock source may also be used. |
| XTALO                         | O       | 80     | Crystal output.  |
| <b>Smart Card Reader Pins</b> |         |        |  |
| SCPWR                         | O       | 66     | Smart card power supplier enable pin                                   |
| SCIO                          | I/O     | 63     | Smart card serial data input/output pin or GPIO pin                    |
| SCCLK                         | O (I/O) | 64     | Smart card clock output (default 3MHz) or GPIO pin                     |
| SCRST                         | O       | 65     | Smart card reset signal  |
| SCPRSNT                       | I       | 83     | Smart card existed indicator. Schmitt-trigger input                    |
| <b>Extra Pins</b>             |         |        |  |
| PLEN                          | I       | 53     | PLL enable pin; Schmitt-trigger pull up input                          |
| XCVREN                        | I       | 95     | XCVR enable pin; Schmitt-trigger pull up input                         |
| SOFTCNEN                      | I       | 11     | Software connection enable pin; Schmitt-trigger pull up input          |
| TESTENB                       | I       | 12     | Test enable pin; Schmitt-trigger pull up input                         |
| <b>Power Pins</b>             |         |        |  |
| VSS                           | PWR     | 37,81  | GROUND: ground potential.  |
| VDD                           | PWR     | 38,82  | POWER SUPPLY: Supply voltage for operation.                            |
| <b>Serial Interface</b>       |         |        |  |
| SDA                           | I/O     | 8      | Data input/output of serial interface                                  |
| SCL                           | I       | 9      | Clock input of serial interface  |

# W81E381D/W81E381AD



## 3.2.1 100-pin LQFP package description, continued

| SYMBOL         | TYPE  | PIN NO                     | DESCRIPTIONS   |
|----------------|-------|----------------------------|--|
| <b>uC Pins</b> |       |                            |  |
| EA             | I     | 96                         | EXTERNAL ACCESS ENABLE: This pin forces the processor to execute the external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the 64 KB area. Otherwise they will be present on the bus. |
| UC51EN         | I     | 97                         | EXTERNAL uC51 ENABLE: to enable external processor   |
| PSEN           | O H   | 39                         | PROGRAM STORE ENABLE: $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus.<br>When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.  |
| ALE            | O H   | 86                         | ADDRESS LATCH ENABLE: ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.   |
| RST            | I L   | 61                         | RESET: A high on this pin for two machine cycles while the oscillator is running resets the device.  |
| UC-XO          | O     | 45                         | uC Crystal output.   |
| UC-XI          | I     | 46                         | uC Crystal input.  |
| P0.0 - 7       | I/O D | 93,94,14,15<br>29,31,32,33 | PORT 0: Function is the same as that of the standard 8052.   |
| P1.0           | I/O   | 16                         | It is a high drive I/O pad. Used as a GPIO pin for memory-type SC  |
| P1.1           | I/O   | 18                         | It is a high drive I/O pad. Used as a GPIO pin for memory-type SC  |
| P1.2           | I/O   | 19                         | Used as a GPIO pin for memory-type SC  |
| P1.3           | I/O   | 26                         | Used as a GPIO pin for memory-type SC  |
| P1.4           | I/O   | 27                         | Used as a GPIO pin for memory-type SC  |
| P1.5           | I/O   | 43                         | Used as a GPIO pin for memory-type SC  |
| P1.6           | I/O   | 51                         | GPIO & remote wakeup pin   |
| P1.7           | I/O   | 52                         | GPIO & external interrupt pin  |
| P2.0 - 7       | I/O H | 41,42,55,56<br>57,59,60,84 | PORT 2: Bi-directional I/O port with internal pull-ups. Also provides the upper address bits for external memory. Can be programmed as output-latched port as on-chip 74373, or a buffer input port as an on-chip 74244.   |
| P3.0 - 7       | I/O H | 68,69,35,36<br>88,89,90,91 | PORT 3: Function is the same as that of the standard 8052.   |

\*Note: **TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain, PWR: Power pins

# W81E381D/W81E381AD



## 4. PROGRAMMING INTERFACE

### 4.1 Register map

|    | 0/8                | 1/9                             | 2/A                 | 3/B                             | 4/C                | 5/D                | 6/E                 | 7/F                             |    |
|----|--------------------|---------------------------------|---------------------|---------------------------------|--------------------|--------------------|---------------------|---------------------------------|----|
| F8 |                    |                                 |                     |                                 |                    |                    |                     |                                 | FF |
| F0 | B<br>0000 0000     | EPINDEX<br>xxxx xxx0            | TXSTAT<br>0xx0 0000 | TXDAT<br>xxxx xxxx<br>xxx0 0000 | TXCON<br>0xxx 0xxx | TXFLG<br>x0xx 1000 | TXCNT<br>xxxx 0000  | USBIDR                          | F7 |
| E8 |                    |                                 |                     |                                 |                    |                    |                     |                                 | EF |
| E0 | ACC<br>0000 0000   | EPCON<br>001x 0101<br>000x 0000 | RXSTAT<br>0000 0000 | RXDAT<br>0000 0000              | RXCON<br>0xx0 0xxx | RXFLG<br>x0xx 1000 | RXCNT<br>xxxx 0000  | FPCON<br>0000 0000<br>000- 1000 | E7 |
| D8 |                    |                                 |                     |                                 |                    |                    |                     |                                 | DF |
| D0 | PSW<br>0000 00x0   |                                 |                     | AUX<br>0000 0110                | PMPR1<br>xxxx xx00 | PMPR2<br>0000 0000 | CHPENR<br>0000 0000 |                                 | D7 |
| C8 |                    |                                 |                     |                                 |                    |                    |                     | CHPCON<br>0xx0 0000             | CF |
| C0 | FIFLG<br>xxx0 x000 |                                 |                     |                                 | SFRAL<br>0000 0000 | SFRAH<br>0000 0000 | SFRFD<br>0000 0000  | SFRCN<br>0000 0000              | C7 |
| B8 | IP<br>xxx0 0000    |                                 |                     |                                 |                    |                    |                     | SCON                            | BF |
| B0 | P3<br>1111 1111    | IEN1<br>0xxx 0x0x<br>-xxx ____  |                     |                                 |                    |                    |                     | DCON                            | B7 |
| A8 | IE<br>0xx0 0000    |                                 | SCIER<br>0000 0000  | SCISR<br>0000 0000              | SCCR<br>0001 0110  | SCECR<br>0000 0000 | SCGTR<br>0000 0000  |                                 | AF |
| A0 | P2<br>1111 1111    |                                 | FIE<br>xxx0 x000    | SCSR<br>0000 0000               | SCBDR<br>0000 0001 | SCCBR<br>0000 0001 | SCRDR<br>0000 0000  | SCTDR<br>0000 0000              | A7 |
| 98 | SCON<br>0000 0000  | SBUF<br>xxxx xxxx               |                     |                                 |                    |                    |                     |                                 | 9F |
| 90 | P1<br>1111 1111    |                                 |                     |                                 |                    |                    |                     |                                 | 97 |
| 88 | TCON<br>0000 0000  | TMOD<br>0000 0000               | TL0<br>0000 0000    | TL1<br>0000 0000                | TH0<br>0000 0000   | TH1<br>0000 0000   |                     | FADDR<br>0000 0000              | 8F |
| 80 | P0<br>1111 1111    | SP<br>0000 0011                 | DPL<br>0000 0000    | DPH<br>0000 0000                |                    |                    |                     | PCON<br>00xx 0000               | 87 |
|    | 0/8                | 1/9                             | 2/A                 | 3/B                             | 4/C                | 5/D                | 6/E                 | 7/F                             |    |

|                                  |
|----------------------------------|
| 8052 uC SFRs                     |
| USB SFRs                         |
| Flash SFRs                       |
| Smart Card SFRs                  |
| Endpoint-Indexed SFRs by EPINDEX |

# W81E381D/W81E381AD



## 4.2 FLASH Category – Descriptions Summary

| Mnemonic | ISP Registers                                     | Address | Description |      |      |      |       |       |       |         |
|----------|---|---------|-------------|------|------|------|-------|-------|-------|---------|
| SFR CN   | The Control Register of uC ISP Function           | S:C7H   | –           | –    | OEN  | CEN  | CTRL3 | CTRL2 | CTRL1 | CTRL0   |
| SFR FD   | The Programming Data Register for Flash Memory    | S:C6H   | FD7         | FD6  | FD5  | FD4  | FD3   | FD2   | FD1   | FD0     |
| SFR AH   | The High Byte of the Programming Address          | S:C5H   | HA7         | HA6  | HA5  | HA4  | HA3   | HA2   | HA1   | HA0     |
| SFR AL   | The Low Byte of the Programming Address           | S:C4H   | LA6         | LA6  | LA5  | LA4  | LA3   | LA2   | LA1   | LA0     |
| Mnemonic | uC Control Registers                              | Address | Description |      |      |      |       |       |       |         |
| CHPCON   | On-chip Programming Control Register              | S:CFH   | –           | –    | –    | –    | –     | –     | –     | FPROGEN |
| PMPR2    | Flash Memory Protective Blocks Configure Register | S:D5H   | LBP7        | LBP6 | LBP5 | LBP4 | LBP3  | LBP2  | LBP1  | LBP0    |
| PMPR1    | Flash Memory Protective Blocks Configure Register | S:D4H   | –           | –    | –    | –    | –     | –     | HBP1  | HBP0    |

## 4.3 SC Category - Descriptions Summary

| Mnemonic | SC Interrupt SFRs              | Address | Description |        |        |         |         |        |      |        |
|----------|--------------------------------|---------|-------------|--------|--------|---------|---------|--------|------|--------|
| SCIER    | SC Interrupt Enable Register   | S:AAH   | –           | ESCPTI | WCE    | –       | RDRE    | PBE    | EXIE | –      |
| SCISR    | SC Interrupt Status Register   | S:ABH   | –           | SCPTI  | WCI    | TDI     | RDRI    | PBRI   | EXI  | EXI_16 |
| Mnemonic | SC Control SFRs                | Address | Description |        |        |         |         |        |      |        |
| SCSR     | SC Status Register             | S:A3H   | –           | –      | –      | –       | SCPRSNT | –      | –    | CA     |
| SCCR     | SC Control Register            | S:ACH   | –           | –      | –      | CLKSTPL | S_CK1   | S_CK0  | EPE  | EXINTH |
| SCECR    | SC Extended Control Register   | S:ADH   | CRDRST      | PWRENP | VCC_EN | –       | –       | CLKSTP | SCIO | SCRRST |
| SCGTR    | SC Guard Time Control Register | S:AEH   | BIT7        | BIT6   | BIT5   | BIT4    | BIT3    | BIT2   | BIT1 | BIT0   |
| SCBDR    | SC Baud Rate Divider Register  | S:A4H   | BIT7        | BIT6   | BIT5   | BIT4    | BIT3    | BIT2   | BIT1 | BIT0   |
| SCC BR   | SC Clock Base Register         | S:A5H   | BIT7        | BIT6   | BIT5   | BIT4    | BIT3    | BIT2   | BIT1 | BIT0   |
| Mnemonic | SC Data SFRs                   | Address | Description |        |        |         |         |        |      |        |
| SCRDR    | SC RX Data Register            | S:A6H   | RD7         | RD6    | RD5    | RD4     | RD3     | RD2    | RD1  | RD0    |
| SCTDR    | SC TX Data Register            | S:A7H   | TD7         | TD6    | TD5    | TD4     | TD3     | TD2    | TD1  | TD0    |

# W81E381D/W81E381AD



## 4.4 USB Category - Descriptions Summary

| Mnemonic | USB Power Control SFRs                 | Address | Description |          |         |         |          |          |          |          |  |
|----------|--|---------|-------------|----------|---------|---------|----------|----------|----------|----------|--|
| FPCON    | Function Power Control Register        | S:E7H   | FPD         | FRWUPE   | FWKP    | URDIS   | URST     | FRWU     | FRSM     | FSUS     |  |
| Mnemonic | USB Interrupt System SFRs              | Address | Description |          |         |         |          |          |          |          |  |
| FIE      | USB Function Interrupt Enable Register | S:A2H   | –           | –        | FRXIE4  | FTXIE3  | FRXIE2   | FTXIE1   | FRXIE0   | FTXIE0   |  |
| FIFLG    | USB Function Interrupt Flag Register   | S:C0H   | –           | –        | FRXD4   | FTXD3   | FRXD2    | FTXD1    | FRXD0    | FTXD0    |  |
| IEN1     | USB Interrupt Enable Register          | S:B1H   | EA          | –        | –       | –       | EFSR     | –        | EF       | –        |  |
| Mnemonic | USB Function SFRs                      | Address | Description |          |         |         |          |          |          |          |  |
| EPCON*   | Endpoint Control Register              | S:E1H   | RXSTL       | TXSTL    | CTLEP   | –       | RXIE     | RXEPEN   | TXOE     | TXEPEN   |  |
| EPINDEX  | Endpoint Index Register                | S:F1H   | –           | –        | –       | –       | –        | EPINX2   | EPINX1   | EPINX0   |  |
| FADDR    | Function Address Register              | S:8FH   | –           | A6       | A5      | A4      | A3       | A2       | A1       | A0       |  |
| RXCNT*   | Receive FIFO Byte-Count Register       | S:E6H   | –           | –        | –       | BC4     | BC3      | BC2      | BC1      | BC0      |  |
| RXCON*   | Receive FIFO Control Register          | S:E4H   | RXCLR       | –        | –       | RXFFRC  | RXISO    | –        | –        | –        |  |
| RXDAT*   | Receive FIFO Data Register             | S:E3H   | RD7         | RD6      | RD5     | RD4     | RD3      | RD2      | RD1      | RD0      |  |
| RXFLG*   | Receive FIFO Flag Register             | S:E5H   | –           | RXFIFO   | –       | –       | RXEMP    | RXFULL   | RXURF    | RXOVF    |  |
| RXSTAT*  | Endpoint Receive Status Register       | S:E2H   | RXSEQ       | RXSETUP  | STOVW   | EDOVW   | RXSOVW   | RXVOID   | RXERR    | RXACK    |  |
| TXCNT*   | Transmit FIFO Byte-Count Register      | S:F6H   | –           | –        | –       | BC4     | BC3      | BC2      | BC1      | BC0      |  |
| TXCON*   | Transmit FIFO Control Register         | S:F4H   | TXCLR       | –        | –       | –       | –        | –        | –        | –        |  |
| TXDAT*   | Transmit FIFO Data Register            | S:F3H   | TD7         | TD6      | TD5     | TD4     | TD3      | TD2      | TD1      | TD0      |  |
| TXFLG*   | Transmit FIFO Flag Register            | S:F5H   | –           | TXFIFO   | –       | –       | TXEMP    | TXFULL   | TXURF    | TXOVF    |  |
| TXSTAT*  | Endpoint Transmit Status Register      | S:F2H   | TXSEQ       | –        | –       | TXFLUSH | TXSOVW   | TXVOID   | TXERR    | TXACK    |  |
| Mnemonic | USB Device SFRs                        | Address | Description |          |         |         |          |          |          |          |  |
| DCON     | Device Control Register 1              | S:B7H   | TEST_MODE   | SCGPIOSL | SCIOGPE | SCIOGPD | SCCLKGPE | SCCLKGPD | PTRWJEN  | CONPUEN  |  |
| SCON     | SIE Control Register                   | S:BFH   | SIERXDE     | SIELSE   | SECKPAT | STODPAT | SEOSMOD1 | SEOSMOD0 | SEOPMOD1 | SEOPMOD0 |  |

## 4.5 Individual register description

### 4.5.1 Register Descriptions - USB Power Control Registers (E7)

**FPCON**

Address: S:E7H  
 System Reset State: 0000 0000H  
 USB Reset State: 000–1000H

*Function Power Control Register. Facilitates the control and status relating to power-down mode, remote-wakeup enable, function wakeup, USB reset separation, remote wake-up control and function resume/suspend.*

|            |               |             |             |             |             |             |             |
|------------|---------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 7          | 6             | 5           | 4           | 3           | 2           | 1           | 0           |
| <b>FPD</b> | <b>FRWUPE</b> | <b>FWKP</b> | <b>FRIE</b> | <b>FRST</b> | <b>FRWU</b> | <b>FRSM</b> | <b>FSUS</b> |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | FPD          | Function Power-down Mode Bit:<br>When set, activates USB power-down mode. This bit should only be set if the FSUS bit is also set. Cleared by hardware when an interrupt or reset occurs. Recommends to set with PCON.0 & PCON.1 together.  |
| 6          | FRWUPE       | Function Remote Wake-up Enable Bit:<br>Set if the function is currently enabled to request remote wake-up. This bit is modified through the Set/ClearFeature (DEVICE_REMOTE_WAKEUP). When '0', the function can't initiate remote resume via either FW setting FRWU or triggered by external signal. Note that don't set this bit until after the Function is enumerated and the host issued a SetFeature(DEVICE_REMOTE_WAKEUP).  |
| 5          | FWKP         | Function Wake-up Bit:<br>1=wake-up. Set by hardware when wake-up events occur, asserts signal FWKP to high. This bit is "Or"ed with FSUS and FRSM to generate the interrupt. Cleared by firmware when servicing the function. Firmware should prioritize FRSM over FWKP if both bits are set simultaneously.<br>Note: This bit is not set if FRWUPE=0 or FRSM=1 or FRWU=1.  |
| 4          | URDIS        | USB Reset Disable:<br>When cleared by firmware, a chip reset occurs upon receiving of a USB reset signal. This resets all USB blocks, microcontroller, and all peripherals. When set by firmware, a USB reset signal just only reset all USB blocks, but not reset microcontroller and all peripherals. Microcontroller can be interrupted via the interrupt source URST that is set by the completion of a received USB reset. Note that IEN1. EA/EFSR/EF doesn't be reset furring USB reset signaling if this bit is set. |



# W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 3          | URST         | <b>USB Reset Flag:</b><br>This flag will be set by hardware when a USB reset occurs and completes, regardless of when the EFSR bit in the IEN1 register is enabled or disabled. The URST also serves as the interrupt bit, "Or"ed with FRSM and FSUS bits to generate an interrupt. Should be cleared by firmware when serving the USB reset interrupt.   |
| 2          | FRWU         | <b>Function Remote Wake-up Bit:</b><br>This bit is used by the function to issue a wake-up signal (K) to host when uC is interrupt by the FWKP=1. Set by firmware to make driving resume signal. It will be cleared by hardware when remote-wakeup is completed. FW can poll and wait FRWU=0 to know the completion of remote-wakeup.<br>Note: Don't set this bit unless the function is suspended (FSUS=1 and FRSM=0). |
| 1          | FRSM         | <b>Function Resume Bit:</b><br>1= resume. Set by hardware when "start" or "end" of up stream port resume is occurred. This bit is "Or"ed with FSUS to generate the interrupt. Cleared by firmware when servicing the function suspend/resume interrupt.<br>Note: This bit is not set if remote wakeup is active (FRWU=1). Firmware should prioritize FRSM over FSUS if both bits are set simultaneously.                |
| 0          | FSUS         | <b>Function Suspend Bit:</b><br>1= suspend. Set by hardware when the device is set to suspend. This bit is "Or"ed with FRSM to generate the interrupt. During the function suspend ISR, firmware should set the FPD bit to enter the suspend mode. Cleared by hardware when a function resume occurs.   |

# W81E381D/W81E381AD



## 4.5.2 Register Descriptions - USB Interrupt System SFRs (A2)

**FIE**

Address: S:A2H  
Reset State: XX00 0000H

*Function Interrupt Enable Register: Enables and disables the received and transmit done interrupts for the function endpoints.*

|   |   |        |        |        |        |        |        |
|---|---|--------|--------|--------|--------|--------|--------|
| 7 | 6 | 5      | 4      | 3      | 2      | 1      | 0      |
| - | - | FRXIE4 | FTXIE3 | FRXIE2 | FTXIE1 | FRXIE0 | FTXIE0 |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.                           |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.                           |
| 5          | FRXIE4       | Function Receive Interrupt Enable 4:<br>Enables the receive done interrupt for function endpoint 4 (FRXD4).   |
| 4          | FTXIE3       | Function Transmit Interrupt Enable 3:<br>Enables the transmit done interrupt for function endpoint 3 (FTXD3). |
| 3          | FRXIE2       | Function Receive Interrupt Enable 2:<br>Enables the receive done interrupt for function endpoint 2 (FRXD2).   |
| 2          | FTXIE1       | Function Transmit Interrupt Enable 1:<br>Enables the receive done interrupt for function endpoint 1 (FTXD1).  |
| 1          | FRXIE0       | Function Receive Interrupt Enable 0:<br>Enables the receive done interrupt for function endpoint 0 (FRXD0).   |
| 0          | FTXIE0       | Function Transmit Interrupt Enable 0:<br>Enables the transmit done interrupt for function endpoint 0 (FTXD0). |

# W81E381D/W81E381AD



## 4.5.3 Register Descriptions - USB Interrupt System SFRs (C0)

**FIFLG**

Address: S:C0H  
Reset State: XX00 0000H

*Function Interrupt Flag Register: Contains the USB function's transmit and receive done interrupt flags for non-isochronous endpoints.*

|   |   |       |       |       |       |       |       |
|---|---|-------|-------|-------|-------|-------|-------|
| 7 | 6 | 5     | 4     | 3     | 2     | 1     | 0     |
| - | - | FRXD4 | FTXD3 | FRXD2 | FTXD1 | FRXD0 | FTXD0 |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.                                       |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.                                       |
| 5          | FRXD4        | Function Receive Done Flag 4: (read, write clear)<br>For endpoint 4. This bit is cleared when firmware writes '1' to it.  |
| 4          | FTXD3        | Function Transmit Done Flag 3: (read, write clear)<br>For endpoint 3. This bit is cleared when firmware writes '1' to it. |
| 3          | FRXD2        | Function Receive Done Flag 2: (read, write clear)<br>For endpoint 2. This bit is cleared when firmware writes '1' to it.  |
| 2          | FTXD1        | Function Transmit Done Flag 1: (read, write clear)<br>For endpoint 1. This bit is cleared when firmware writes '1' to it. |
| 1          | FRXD0        | Function Receive Done Flag 0: (read, write clear)<br>For endpoint 0. This bit is cleared when firmware writes '1' to it.  |
| 0          | FTXD0        | Function Transmit Done Flag 0: (read, write clear)<br>For endpoint 0. This bit is cleared when firmware writes '1' to it. |

# W81E381D/W81E381AD



## 4.5.4 Register Descriptions - USB Interrupt System SFRs (B1)

IEN1

Address: S:B1H

System Reset State: 0XXX 0X0XH

USB Reset with PCON1.URDIS=1: -XXX -X--XH

*USB Interrupt Enable Register: Contains the enable bits for the USB interrupts.*

|    |   |   |   |      |   |    |   |
|----|---|---|---|------|---|----|---|
| 7  | 6 | 5 | 4 | 3    | 2 | 1  | 0 |
| EA | - | - | - | EFSR | - | EF | - |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | EA           | Global Interrupt Enable:<br>Setting this bit enables the interrupts that are individually enabled by bit3 & bit1 of this register. Clearing this bit disables all interrupts.<br>Note: This bit doesn't be reset when a USB reset occurs if FPCON.URDIS=1. |
| 6          | -            | Reserved:  |
| 5          | -            | Reserved:  |
| 4          | -            | Reserved:  |
| 3          | EFSR         | Enable Function Suspend/Resume:<br>Function suspend/resume interrupt enable bit.<br>Note This bit doesn't be reset when a USB reset occurs if FPCON.URDIS=1.   |
| 2          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |
| 1          | EF           | Enable Function:<br>Transmit/receive done interrupt enable bit for non-isochronous USB function endpoints.<br>Note: This bit doesn't be reset when a USB reset occurs if FPCON.URDIS=1.  |
| 0          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |

# W81E381D/W81E381AD



## 4.5.5 Register Descriptions - USB Function SFRs (E1)

**EPCON**

Address: S:E1H

Reset State(Endpoint 0): 001X 0101H

Reset State(Endpoint X): 000X 0000H

*Endpoint Control Register (Endpoint-Indexed). This SFR configures the operation of the endpoint specified by EPINDEX.*

|              |              |              |          |             |               |             |               |
|--------------|--------------|--------------|----------|-------------|---------------|-------------|---------------|
| 7            | 6            | 5            | 4        | 3           | 2             | 1           | 0             |
| <b>RXSTL</b> | <b>TXSTL</b> | <b>CTLEP</b> | <b>-</b> | <b>RXIE</b> | <b>RXEPEN</b> | <b>TXOE</b> | <b>TXEPEN</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | RXSTL        | <p><b>Stall Receive Endpoint:</b><br/>Set this bit to stall the receive endpoint. Clear this bit only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond with a STALL handshake to a valid OUT token. When this bit is set and RXSETUP is set, the receive endpoint will NAK. This bit does not affect the reception of SETUP tokens by a control endpoint.</p>              |
| 6          | TXSTL        | <p><b>Stall Transmit Endpoint:</b><br/>Set this bit to stall the transmit endpoint. Clear this bit only when the host has intervened through commands sent down endpoint 0. When this bit is set and RXSETUP is clear, the receive endpoint will respond will respond with a STALL handshake to a valid IN token. When this bit is set and RXSETUP is set, the receive endpoint will NAK.</p>  |
| 5          | CTLEP        | <p><b>Control Endpoint:</b><br/>Set this bit to configure the endpoint as a control endpoint. Only control endpoints are capable of receiving SETUP tokens. For W81E381, the endpoint 0 (EPINDEX=0000 0000) is hard-wired to "1", since endpoint 0 is always a control endpoint.</p>   |
| 4          | -            | <p><b>Reserved:</b><br/>The value read from this bit is indeterminate. Write zero to this bit.</p>   |
| 3          | RXIE         | <p><b>Receive Input Enable:</b><br/>Set this bit to enable data from the USB to be written into the receive FIFO. If cleared, the endpoint will not write the received data into the receive FIFO at the end of reception, but will return a NAK handshake on a valid OUT token if the RXSTL bit is not set. This bit does not affect a valid SETUP token. A valid SETUP token and packet overrides this bit if it is cleared, and place the receive data in the FIFO.</p> |

## W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 2          | RXEPEN       | Receive Endpoint Enable:<br>Set this bit to enable the receive endpoint. When disabled, the endpoint does not respond to a valid OUT or SETUP token. This bit is hardware read-only and has the highest priority between RXIE and RXSTL.<br>Note: The endpoint 0 is enabled for reception upon reset. |
| 1          | TXOE         | Transmit Output Enable:<br>This bit used to enable the data in TXDAT to be transmitted. If cleared, the endpoint returns a NAK handshake to a valid IN token if the TXSTL bit is not set.   |
| 0          | TXEPEN       | Transmit Endpoint Enable:<br>This bit is used to enable the transmit endpoint. When disabled, the endpoint does not respond to a valid IN token. This bit is hardware read-only.<br>Note: The endpoint 0 is enabled for transmission upon reset.  |

# W81E381D/W81E381AD



## 4.5.6 Register Descriptions - USB Function SFRs (F1)

**EPINDEX**

Address: S:F1H  
Reset State: XXXX X000H

*Endpoint Index Register. This register identifies the endpoint pair. It contains select the transmit and receive FIFO pair and serve as an index to endpoint-specific SFRs.*

|   |   |   |   |   |        |        |        |
|---|---|---|---|---|--------|--------|--------|
| 7 | 6 | 5 | 4 | 3 | 2      | 1      | 0      |
| - | - | - | - | - | EPINX2 | EPINX1 | EPINX0 |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 4          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 3          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 2:0        | EPINX2:0     | Endpoint Index Bit 2:0:<br>EPINDEX 7:0<br>= XXXX X000 Function Endpoint 0 -> Control Read/write<br>= XXXX X001 Function Endpoint 1 -> Bulk In<br>= XXXX X010 Function Endpoint 2 -> Bulk Out<br>= XXXX X011 Function Endpoint 3 -> Interrupt In<br>= XXXX X100 Function Endpoint 4 -> Interrupt Out |

# W81E381D/W81E381AD



## 4.5.7 Register Descriptions - USB Function SFRs (8F)

**FADDR**

Address: S:8FH  
Reset State: 0000 0000H

*Function Address Register. This SFR holds the address for the USB function. During bus enumeration, it is written with a unique value assigned by the host.*

|   |    |    |    |    |    |    |    |
|---|----|----|----|----|----|----|----|
| 7 | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| - | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |
| 6          | A6           | Programmable Function Address Bit 6:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |
| 5          | A5           | Programmable Function Address Bit 5:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |
| 4          | A4           | Programmable Function Address Bit 4:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |
| 3          | A3           | Programmable Function Address Bit 3:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |



# W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 2          | A2           | Programmable Function Address Bit 2:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |
| 1          | A1           | Programmable Function Address Bit 1:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |
| 0          | A0           | Programmable Function Address Bit 0:<br>This register is programmed through the commands received via endpoint 0 on configuration, which should be the only time the firmware should change the value of this register. This register is hardware read-only. |

# W81E381D/W81E381AD



## 4.5.8 Register Descriptions - USB Function SFRs (E6)

**RXCNT**

Address: S:E6H  
Reset State: XXX0 0000H

*Receive FIFO Byte-Count Register (Endpoint-Indexed). Store the byte count for the data packet received in the receive FIFO specified by EPINDEX.*

|   |   |   |     |     |     |     |     |
|---|---|---|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4   | 3   | 2   | 1   | 0   |
| - | - | - | BC4 | BC3 | BC2 | BC1 | BC0 |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit. |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit. |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit. |
| 4          | BC4          | Receive Byte Count Bit 4:<br>Store received byte count. Maximum is sixteen bytes.   |
| 3          | BC3          | Receive Byte Count Bit 3:<br>Store received byte count. Maximum is sixteen bytes.   |
| 2          | BC2          | Receive Byte Count Bit 2:<br>Store received byte count. Maximum is sixteen bytes.   |
| 1          | BC1          | Receive Byte Count Bit 1:<br>Store received byte count. Maximum is sixteen bytes.   |
| 0          | BC0          | Receive Byte Count Bit 0:<br>Store received byte count. Maximum is sixteen bytes.   |

# W81E381D/W81E381AD



## 4.5.9 Register Descriptions - USB Function SFRs (E4)

**RXCON**

Address: S:E4H  
Reset State: 0XX0 0XXXH

Receive FIFO Control Register(Endpoint-Indexed). Controls the receive FIFO specified by EPINDEX.

|              |   |   |               |              |   |   |   |
|--------------|---|---|---------------|--------------|---|---|---|
| 7            | 6 | 5 | 4             | 3            | 2 | 1 | 0 |
| <b>RXCLR</b> | - | - | <b>RXFFRC</b> | <b>RXISO</b> | - | - | - |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | RXCLR        | Receive FIFO Clear:<br>Set this bit to flush the entire receive FIFO. All flags in RXFLG revert to their reset states (RXEMP is set; the other flags cleared) and all the read/write pointers and markers are read. The RXISO bit in this register and the RXSEQ bit in the RXSTAT register are not affected by this operation. Hardware clears this bit when the flush operation is completed. |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 4          | RXFFRC       | FIFO Read Complete:<br>Set this bit to release the receive FIFO when data set read is complete. Setting this bit "clears" the RXFIF "bit" in the RXFLG register corresponding to the data set that was just read. Hardware clears this bit after the RXFIF bit is cleared. All data from this data set must have been read.<br>Note: that RXFFRC only works if STOVW and EDOVW are cleared.     |
| 3          | RXISO        | Receive Isochronous Data:<br>Set this bit to indicate that the receive FIFO is programmed to receive isochronous data and to set up the USB interface to handle an isochronous data transfer. This bit is not reset when the RXCLR bit is set; it must be cleared by firmware.  |
| 2          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 1          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 0          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |

# W81E381D/W81E381AD



## 4.5.10 Register Descriptions - USB Function SFRs (E3)

**RXDAT**

Address: S:E3H  
Reset State: XXXX XXXXH

*Receive FIFO Data Register (Endpoint-Indexed). Receive FIFO data specified by EPINDEX is stored and read from this register.*

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| <b>RD7</b> | <b>RD6</b> | <b>RD5</b> | <b>RD4</b> | <b>RD3</b> | <b>RD2</b> | <b>RD1</b> | <b>RD0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | RD7          | Receive Data Bit 7:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |
| 6          | RD6          | Receive Data Bit 6:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |
| 5          | RD5          | Receive Data Bit 5:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |
| 4          | RD4          | Receive Data Bit 4:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |
| 3          | RD3          | Receive Data Bit 3:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |

## W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 2          | RD2          | Receive Data Bit 2:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |
| 1          | RD1          | Receive Data Bit 1:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |
| 0          | RD0          | Receive Data Bit 0:<br>To write data to the receive FIFO, the FIU/HIU writes to this register. To read data from the receive FIFO, the firmware reads from this register. The write pointer and read pointer are incremented automatically after a write and read, respectively. |

# W81E381D/W81E381AD



## 4.5.11 Register Descriptions - USB Function SFRs (E5)

**RXFLG**

Address: S:E5H  
Reset State: X0XX 1000

Receive FIFO Flag Register (Endpoint-Indexed). These flags indicate the status of data packet in the receive FIFO specified by EPINDEX.

|   |        |   |   |       |        |       |       |
|---|--------|---|---|-------|--------|-------|-------|
| 7 | 6      | 5 | 4 | 3     | 2      | 1     | 0     |
| - | RXFIFO | - | - | RXEMP | RXFULL | RXURF | RXOVF |

| Bit Number | Bit Mnemonic | Function  |             |           |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
|------------|--------------|---|-------------|-----------|------|-------------|-----------|---|---------|---|----------|----------|---|---------|---|---|----------|---|---------|---|---|---------|---|-------------|---|---|---------|---|-------------|---|---|----------|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |             |           |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 6          | RXFIFO       | Receive FIFO Index Flag (read-only):<br>This read-only flag indicate whether a data packet is updated after each write to RXCNT to reflect the addition of a data packet. Likewise, the RXFIF bit is cleared in sequence after each setting of the RXFFRC bit. The next state table for RXFIFO bit is shown below in single packet mode. <table border="1" data-bbox="522 1213 1390 1415"> <thead> <tr> <th>RXFIFO</th> <th>Operation</th> <th>Flag</th> <th>Next RXFIFO</th> <th>Next Flag</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>rev. WP</td> <td>x</td> <td>unchange</td> <td>unchange</td> </tr> <tr> <td>0</td> <td>adv. WM</td> <td>x</td> <td>1</td> <td>unchange</td> </tr> <tr> <td>1</td> <td>adv. WM</td> <td>x</td> <td>1</td> <td>RXOVF=1</td> </tr> <tr> <td>0</td> <td>RXFFRC --&gt;1</td> <td>x</td> <td>0</td> <td>RXURF=1</td> </tr> <tr> <td>1</td> <td>RXFFRC --&gt;1</td> <td>x</td> <td>0</td> <td>unchange</td> </tr> </tbody> </table> | RXFIFO      | Operation | Flag | Next RXFIFO | Next Flag | X | rev. WP | x | unchange | unchange | 0 | adv. WM | x | 1 | unchange | 1 | adv. WM | x | 1 | RXOVF=1 | 0 | RXFFRC -->1 | x | 0 | RXURF=1 | 1 | RXFFRC -->1 | x | 0 | unchange |
| RXFIFO     | Operation    | Flag  | Next RXFIFO | Next Flag |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| X          | rev. WP      | x   | unchange    | unchange  |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 0          | adv. WM      | x   | 1           | unchange  |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 1          | adv. WM      | x   | 1           | RXOVF=1   |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 0          | RXFFRC -->1  | x   | 0           | RXURF=1   |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 1          | RXFFRC -->1  | x   | 0           | unchange  |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |             |           |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 4          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |             |           |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |
| 3          | RXEMP        | Receive FIFO Empty Flag (read-only):<br>Hardware sets this flag when the write pointer is as the same location as the read pointer and the write pointer equals the write maker and neither pointer has resoled over. Hardware clears the bit when the empty condition no longer exists. This is not a sticky bit and always tracks the current status of the receive FIFO, regardless of ISO or non-ISO mode.  |             |           |      |             |           |   |         |   |          |          |   |         |   |   |          |   |         |   |   |         |   |             |   |   |         |   |             |   |   |          |

# W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 2          | RXFULL       | <p>Receive FIFO Full Flag (read-only):</p> <p>Hardware sets this flag when the write pointer has rolled over and equals the read pointer. Hardware clears the bit when the full condition no longer exists. This is not a sticky bit and always tracks the current status of the receive FIFO, regardless of ISO or non-ISO mode.</p>   |
| 1          | RXURF        | <p>Receive FIFO Under-run Flag:</p> <p>Hardware sets this bit when an additional byte is read from an empty receive FIFO or RXCNT. Hardware does not clear this bit, so you must clear it in firmware. When the receive FIFO under-run, the read point will bit advance-it remains locked in the empty position.</p> <p>Note: that you must check the RXURF flag after reads from the receive FIFO before setting the RXFFRC bit in RXCON. When the bit is set, the FIFO is in an unknown state and all transmissions are "NAK"ed. It is recommended that you reset the FIFO in the error management routine using the RXCLR bit in the RXCON register.</p>                                     |
| 0          | RXOVF        | <p>Receive FIFO Overrun Flag:</p> <p>Hardware sets this bit when FIU/HIU writes an additional byte to a full receive FIFO or writes a byte count to RXCNT with RXFIFO=1.This is a sticky bit that must be cleared through firmware, although it can be cleared by hardware if a SETUP packet is received after RXOVF error had already occurred. When the receive FIFO overruns, the write pointer will not advance- it remains locked in the full position.</p> <p>Note: that when the bit is set, the FIFO is in an unknown state and all transmissions are "NAK"ed. It is recommended that you reset the FIFO in the error management routine using the RXCLR bit in the RXCON register.</p> |

# W81E381D/W81E381AD



## 4.5.12 Register Descriptions - USB Function SFRs (E2)

**RXSTAT**

Address: S:E2H  
Reset State: 0000 0000

*Endpoint Receive Status Register (Endpoint-Indexed). Contains the current endpoint status of the receive FIFO specified by EPINDEX.*

|              |                |              |              |               |               |              |              |
|--------------|----------------|--------------|--------------|---------------|---------------|--------------|--------------|
| 7            | 6              | 5            | 4            | 3             | 2             | 1            | 0            |
| <b>RXSEQ</b> | <b>RXSETUP</b> | <b>STOVW</b> | <b>EDOVW</b> | <b>RXSOVW</b> | <b>RXVOID</b> | <b>RXERR</b> | <b>RXACK</b> |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | RXSEQ        | <p>Receive Endpoint Sequence Bit(read, condition write):<br/>The bit will be toggled on completion of an ACK handshake in response to an OUT token. This bit will be set/cleared by hardware after reception of a SETUP token. This bit can be written by firmware if the RXOVW bit is set when written along with the new RXSEQ value.<br/>Note that always verify this bit after writing to ensure that there is no conflict with hardware, which could occurred if a new SETUP token is received.</p>  |
| 6          | RXSETUP      | <p>Received Setup Token:<br/>This bit is set by hardware when a valid SETUP token has been received. When set, this bit causes received IN or OUT tokens to be "NAK"ed until the bit is cleared to allow proper data management for the transmit and receive FIFOs from the previous transaction. IN or OUT tokens are "NAK"ed even if the endpoint is stalled (RXSTL/TXSTL) to allow a control transaction to clear a stalled endpoint. Clear this bit upon detection of a SETUP token or the firmware ready to handle the data/status stage of control transfer.</p>  |
| 5          | STOVW        | <p>Start Overwrite Flag (read-only):<br/>Set by hardware upon receipt of a DETUP token for any control endpoint to indicate that the receive FIFO is being overwritten with new SETUP data. When set, the FIFO state (RXFIFO and read pointer) resets and is locked for this endpoint until EDVW is set. This prevents a proper, ongoing firmware read from corrupting the read pointer as the receive FIFO is being cleared and new data is being written into it. This bit is cleared by hardware at the end of handshake phase transmission of the SETUP stage. This bit is used only for control endpoints.</p> |



# W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 4          | EDOVW        | <p>End Overwrite Flag:</p> <p>This flag is set by hardware during the handshake phase of a SETUP stage. It is set after every SETUP packet is received and must be cleared prior to reading the contents of the FIFO. When set, the FIFO state (RXFIFO and read pointer) remains locked for this endpoint until this bit is cleared. This prevents a prior, ongoing firmware read from corrupting the read pointer after the new data has been written into the receive FIFO. This bit is only used for control endpoints.</p> <p>Note: that make sure the EDOVW bit is cleared prior to reading the contents of the FIFO.</p>   |
| 3          | RXSOWW       | <p>Receive Data Sequence Overwrite Bit:</p> <p>Write '1' to this bit to allow the value of the RXSEQ bit to be overwritten. Writing a '0' to this bit has no effect on RXSEQ. This bit always returns '0' when read. The SIE will handle all sequence bit tracking. This bit should be used only when initializing a new configuration or interface.</p>   |
| 2          | RXVOID       | <p>Receive Void Condition (read-only):</p> <p>This bit is set when no valid data is received in response to a SETUP or OUT token due to one of the following conditions: 1. The receive FIFO is still locked; 2. The EPCON register's RXSTL bit is set. This bit does not affect the F/HRXDx, RXERR or RXACK. This bit is set and cleared by hardware. For non-isochronous transactions, this bit is updated by hardware at the end of the transaction in response to valid OUT token. For isochronous transactions, it is not updated until the next SOF.</p>   |
| 1          | RXERR        | <p>Receive Error Condition (read-only):</p> <p>Set when an error condition has occurred with the reception. Complete or partial data has been written into the receive FIFO. No handshake is returned. The error can be one of the following conditions: 1. Data failed CRC check or bit stuffing error; 2. A receive FIFO goes into overrun of under-run condition while receiving. The bit is updated by hardware at the end of a valid SETUP or OUT token transaction (non-isochronous) or at the next SOF on each valid OUT token transaction (isochronous). The corresponding F/HRXDx bit of F/HIFLG is set when active. This bit updated with RXACK bit at the end of data reception and is mutually exclusive with RXACK.</p> |
| 0          | RXACK        | <p>Receive Acknowledged Condition (read-only):</p> <p>This bit is set when data is received completely into a receive FIFO and an ACK handshake is sent. The bit is updated by hardware at the end of a valid SETUP or OUT token transaction (non-isochronous) or at the next SOF on each valid OUT token transaction (isochronous). The corresponding F/HRXDx bit of F/HIFLG is set when active. This bit updated with RXERR bit at the end of data reception and is mutually exclusive with RXERR.</p>   |

# W81E381D/W81E381AD



## 4.5.13 Register Descriptions - USB Function SFRs (F6)

**TXCNT**

Address: S:F6H  
Reset State: XXX0 0000H

*Transmit FIFO Byte-Count Register (Endpoint-indexed). Stored the byte count for the data packet in the transmit FIFO specified by EPINDEX.*

|   |   |   |     |     |     |     |     |
|---|---|---|-----|-----|-----|-----|-----|
| 7 | 6 | 5 | 4   | 3   | 2   | 1   | 0   |
| - | - | - | BC4 | BC3 | BC2 | BC1 | BC0 |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 4          | BC4          | Transmit Byte Count Bit 4:<br>Store transmitted byte count. Maximum is sixteen bytes. |
| 3          | BC3          | Transmit Byte Count Bit 3:<br>Store transmitted byte count. Maximum is sixteen bytes. |
| 2          | BC2          | Transmit Byte Count Bit 2:<br>Store transmitted byte count. Maximum is sixteen bytes. |
| 1          | BC1          | Transmit Byte Count Bit 1:<br>Store transmitted byte count. Maximum is sixteen bytes. |
| 0          | BC0          | Transmit Byte Count Bit 0:<br>Store transmitted byte count. Maximum is sixteen bytes. |

# W81E381D/W81E381AD



## 4.5.14 Register Descriptions - USB Function SFRs (F4)

**TXCON**

Address: S:F4H  
Reset State: 0XXX 0XXXH

*Transmit FIFO Control Register (Endpoint-Indexed). Controls the transmit FIFO specified by EPINDEX.*

|              |   |   |   |   |   |   |   |
|--------------|---|---|---|---|---|---|---|
| 7            | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| <b>TXCLR</b> | - | - | - | - | - | - | - |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | TXCLR        | Transmit FIFO Clear:<br>Set this bit to flush the entire transmit FIFO. All flags in TXFLG revert to their reset states (TXEMP is set; all other flags clear) and all the read/write pointers and makers are reset. The TXISO bit in this register and the TXSEQ bit in the TXSTAL register are not affected by this operation. Hardware clears this bit when the flush operation is completed. |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 4          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 3          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 2          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 1          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |
| 0          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.   |

# W81E381D/W81E381AD



## 4.5.15 Register Descriptions - USB Function SFRs (F3)

**TXDAT**

Address: S:F3H

Reset State (Other Endps): XXXX XXXXH

Reset State (Hub Endp 1): XXX0 0000H

*Transmit FIFO Data Register (Endpoint-Indexed). Data to be transmitted by the FIFO specified by EPINDEX is first written to this register.*

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| <b>TD7</b> | <b>TD6</b> | <b>TD5</b> | <b>TD4</b> | <b>TD3</b> | <b>TD2</b> | <b>TD1</b> | <b>TD0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | TD7          | Transmit Data Bit 7:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively.   |
| 6          | TD6          | Transmit Data Bit 6:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data format the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively. |
| 5          | TD5          | Transmit Data Bit 5:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively.   |
| 4          | TD4          | Transmit Data Bit 4:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively.   |

# W81E381D/W81E381AD



continued

| <b>Bit Number</b> | <b>Bit Mnemonic</b> | <b>Function</b>  |
|-------------------|---------------------|--|
| 3                 | TD3                 | Transmit Data Bit 3:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively. |
| 2                 | TD2                 | Transmit Data Bit 2:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively. |
| 1                 | TD1                 | Transmit Data Bit 1:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively. |
| 0                 | TD0                 | Transmit Data Bit 0:<br>To write data to the transmit FIFO, the firmware writes to this register. To read data from the transmit FIFO, the Function Interface Unit reads from this register. The write pointer and read pointer and read pointer are incremented automatically after a write and read, respectively. |

# W81E381D/W81E381AD



## 4.5.16 Register Descriptions - USB Function SFRs (F5)

**TXFLG**

Address: S:F5H  
Reset State: X0XX 1000H

*Transmit FIFO Flag Register (Endpoint-Indexed). These flags indicate the status of data packet in the transmit FIFO specified by EPINDEX.*

|   |        |   |   |       |        |       |       |
|---|--------|---|---|-------|--------|-------|-------|
| 7 | 6      | 5 | 4 | 3     | 2      | 1     | 0     |
| - | TXFIF0 | - | - | TXEMP | TXFULL | TXURF | TXOVF |

| Bit Number | Bit Mnemonic | Function   |             |           |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
|------------|--------------|--|-------------|-----------|------|-------------|-----------|---|---------|---|-----------|-----------|---|-----------|---|---|-----------|---|-----------|---|---|---------|---|---------|---|---|---------|---|---------|---|---|-----------|
| 7          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |             |           |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 6          | TXFIF0       | Transmit FIFO Index Flag (read-only):<br>This read-only flag indicate whether a data packet is present in the transmit FIFO. The bit is updated after each write to TXCNT to reflect the addition of a data packet. Likewise, the TXFIF bit is cleared in sequence after each advance of the read marker to indicate that the set is effectively discarded. You must check the TXFIF0 flab before and after writes to the transmit FIFO and TXCNT for tractability. The next state table for TXFIF0 bit is shown below in single packet mode. <table border="1" data-bbox="558 1297 1360 1497"> <thead> <tr> <th>TXFIF0</th> <th>Operation</th> <th>Flag</th> <th>Next TXFIF0</th> <th>Next Flag</th> </tr> </thead> <tbody> <tr> <td>X</td> <td>rev. RP</td> <td>X</td> <td>Unchanged</td> <td>Unchanged</td> </tr> <tr> <td>0</td> <td>wr. TXCNT</td> <td>X</td> <td>1</td> <td>Unchanged</td> </tr> <tr> <td>1</td> <td>wr. TXCNT</td> <td>X</td> <td>1</td> <td>TXOVF=1</td> </tr> <tr> <td>0</td> <td>adv. RM</td> <td>X</td> <td>0</td> <td>TXURF=1</td> </tr> <tr> <td>1</td> <td>adv. RM</td> <td>X</td> <td>0</td> <td>Unchanged</td> </tr> </tbody> </table> | TXFIF0      | Operation | Flag | Next TXFIF0 | Next Flag | X | rev. RP | X | Unchanged | Unchanged | 0 | wr. TXCNT | X | 1 | Unchanged | 1 | wr. TXCNT | X | 1 | TXOVF=1 | 0 | adv. RM | X | 0 | TXURF=1 | 1 | adv. RM | X | 0 | Unchanged |
| TXFIF0     | Operation    | Flag   | Next TXFIF0 | Next Flag |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| X          | rev. RP      | X  | Unchanged   | Unchanged |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 0          | wr. TXCNT    | X  | 1           | Unchanged |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 1          | wr. TXCNT    | X  | 1           | TXOVF=1   |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 0          | adv. RM      | X  | 0           | TXURF=1   |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 1          | adv. RM      | X  | 0           | Unchanged |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |             |           |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 4          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |             |           |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |
| 3          | TXEMP        | Transmit FIFO Empty Flag (read-only):<br>Hardware sets this flag when the write pointer is at the same location as the read pointer and the write pointer equals the write marker and neither pointer has rolled over. Hardware clears the bit when the empty condition no longer exists. This is not a sticky bit and always tracks the current status of the transmit FIFO, regardless of ISO or non-ISO mode.   |             |           |      |             |           |   |         |   |           |           |   |           |   |   |           |   |           |   |   |         |   |         |   |   |         |   |         |   |   |           |

# W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 2          | TXFULL       | Transmit FIFO Full Flag (read-only):<br>Hardware sets this flag when the write pointer has rolled over and equals the read pointer. Hardware clears the bit when the full condition no longer exists. This is not a sticky bit and always tracks the current status of the transmit FIFO, regardless of ISO or non-ISO mode.  |
| 1          | TXURF        | Transmit FIFO Under-run Flag:<br>Hardware sets this bit when an additional byte is read from an empty transmit FIFO or TXCNT. If the TXCNT does not agree with the data, hardware sets TXURF. This indicates that the transmitted data was corrupted by a bit-stuffing or CRC error. Hardware does not clear this bit, so you must clear it in firmware. When the transmit FIFO under-runs, the read pointer will not advance-it remains locked in the empty position. When the bit is set, the FIFO is in an unknown state and all transmissions are "NAK"ed. It is recommended that you reset the FIFO in the error management routine using the TXCLR bit in the TXCON register. |
| 0          | TXOVF        | Transmit FIFO Overrun Flag:<br>Hardware sets this bit when firmware writes an additional byte to a full transmit FIFO or writes a byte count to TXCNT with TXFIFO=1. This is a sticky bit that must be cleared through firmware. When the transmit FIFO overruns, the write pointer will not advance-it remains locked in the full position.<br>Note: that when the bit is set, the FIFO is in an unknown state and all transmissions are "NAK"ed. It is recommended that you reset the FIFO in the error management routine using the TXCLR bit in the TXCON register.   |

# W81E381D/W81E381AD



## 4.5.17 Register Descriptions - USB Function SFRs (F2)

**TXSTAT**

Address: S:F2H  
Reset State: 0XX0 0000H

*Endpoint Transmit Status Register (Endpoint-Indexed). Contains the current endpoint status of the transmit FIFO specified by EPINDEX.*

|              |   |   |                |               |               |              |              |
|--------------|---|---|----------------|---------------|---------------|--------------|--------------|
| 7            | 6 | 5 | 4              | 3             | 2             | 1            | 0            |
| <b>TXSEQ</b> | - | - | <b>TXFLUSH</b> | <b>TXSOVW</b> | <b>TXVOID</b> | <b>TXERR</b> | <b>TXACK</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | TXSEQ        | Transmit Endpoint Sequence Bit (read, conditional write):<br>The bit will be transmitted in the next PID and toggled on a valid ACK handshake. This bit is toggled by hardware on a valid SETUP token. This bit can be written by firmware if the TXCOVW bit is set when written along with the new TXSEQ value.   |
| 6          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |
| 5          | -            | Reserved:<br>The value read from this bit is indeterminate. Write zero to this bit.  |
| 4          | TXFLUSH      | Transmit FIFO Packet Flushed (read-only):<br>When set, this bit indicates that hardware flushed a stale ISO data packet from the transmit FIFO due to a TXFIFO=1 at SOF. To guard against a missed IN token in ISO mode, if, with TXFIFO=1, no IN token is received for the current endpoint, hardware automatically flushes the oldest packet and clear TXFIFO=0. |
| 3          | TXSOVW       | Transmit Void Condition (read-only):<br>Write "1" to this bit to allow the value of the TXSEQ bit to be overwritten. Writing "0" to this bit has no effect on TXSEQ. This bit always returns "0" when read. This SIE will handle all sequence bit tracking. This bit should be used only when initializing a new configuration or interface.                       |



# W81E381D/W81E381AD



continued

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 2          | TXVOID       | <p>Transmit Void Condition (read-only):</p> <p>A void condition has occurred in response to a valid IN token. Transmit void is closely associated with the NAK/STALL handshake returned by function after a valid IN token, due to the conditions that cause the transmit FIFO to be un-enabled or not ready to transmit. Use this bit to check any NAK/STALL handshake returned by the function. This bit does not affect the F/HTXDx, TXERR or TXACK. This bit is set and cleared by hardware. For non-isochronous transactions, This bit is updated by hardware at the end of the transaction in response to a valid IN token. For isochronous transactions, it is not updated until the next SOF.</p> |
| 1          | TXERR        | <p>Transmit Error Condition (read-only):</p> <p>An error condition has occurred with the transmission. Complete or partial data has been transmitted. The error can be one of the following conditions: 1. Data transmitted successfully but no handshake received. 2. Transmit FIFO goes into under-run condition while transmitting. The bit is updated by hardware at the end of the data transmission (non-isochronous) or at the next SOF (isochronous). The corresponding F/HTXDx bit of F/HIFLG is set when active. This bit updated with TXACK bit at the end of data transmission and is mutually exclusive with TXACK.</p>  |
| 0          | TXACK        | <p>Transmit Acknowledged Condition (read-only):</p> <p>This bit is set when data is transmitted completely and acknowledged successfully. The bit is updated by hardware at the end of data transmission (non-isochronous) or at the next SOF (isochronous). The corresponding F/HRXDx bit of F/HIFLG is set when active. This bit updated with TXERR bit at the end of data transmission and is mutually exclusive with TXERR.</p>   |

# W81E381D/W81E381AD



## 4.5.18 Register Descriptions - USB Device SFRs (B7)

**DCON**

Address: S:B7H  
Reset State: 0000 0000H

*Device Control Register. This register contains bits for USB Device connection pull-up enable.*

|           |          |         |         |          |          |         |         |
|-----------|----------|---------|---------|----------|----------|---------|---------|
| 7         | 6        | 5       | 4       | 3        | 2        | 1       | 0       |
| TEST_MODE | SCGPIOSL | SCIOGPE | SCIOGPD | SCCLKGPE | SCCLKGPD | PTRWUEN | CONPUEN |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | -            | TEST_MODE enable:<br>Used for test only. In normal operation, this bit should be set to zero.  |
| 6          | SCGPIOSL     | Mode select between normal Smart Card and GPIO pad<br>0: Smart Card<br>1: GPIO pad   |
| 5          | SCIOGPE      | Output enable<br>0: Enable<br>1: Disable   |
| 4          | SCIOGPD      | Smart Card I/O (SCIO) data, when SCIOGPE enable.   |
| 3          | SCCLKGPE     | Output enable<br>0: Enable<br>1: Disable   |
| 2          | SCCLKGPD     | Smart Card Clock (SCCLK) data, when SCCLKGPE enable.   |
| 1          | PTRWUEN      | Path through remote wake-up enable:<br>"1" is enable. If set to zero and remote wake up event occurs in suspend state, device will drive wake up signal to Host after setting the FRWU bit in FPCON register. Otherwise, device will drive wake up signal to Host directly.  |
| 0          | CONPUEN      | Device/USP Connection Pull-Up Enable:<br>This bit is used by FW to control whether device is connected to upper host/hub via enable/disable the on-chip pull-up resistor. Set '1' to enable the D+ pull-up resistor; set '0' to disable the D+ pull-up resistor that is D+/D- is kept disconnected state. Default is cleared to '0' after POR, FW should set '1' to enable connection to upper host/hub. |

# W81E381D/W81E381AD



## 4.5.19 Register Descriptions - USB Device SFRs (BF)

**SCON**

Address: S:BFH  
Reset State: 1011 0000H

*SIE Control Register1: This register contains bits for SIE using RXD enable, SIE LS enable, SIE CRC16-based EOP check patch, SIE time-out detection patch, SIE end-of-sync detection modes, SIE EOP detection modes control.*

|                |               |                |                |                 |                 |                 |                 |
|----------------|---------------|----------------|----------------|-----------------|-----------------|-----------------|-----------------|
| 7              | 6             | 5              | 4              | 3               | 2               | 1               | 0               |
| <b>SIERXDE</b> | <b>SIELSE</b> | <b>SECKPAT</b> | <b>STODPAT</b> | <b>SEOSMOD1</b> | <b>SEOSMOD0</b> | <b>SEOPMOD1</b> | <b>SEOPMOD0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | SIERXDE      | SIE Using RXD Enable: (Reserved for test only)<br>The bit is used to select either the differential receiver output RXD (UBPRXD) or the single-ended receiver output RXDP/RXDM (VPIN/VMIN) as the received serial data for SIE input. Set '1', SIE uses RXD (UBPRXD); set '0', SIE used RXDP/RXDM (VPIN/VMIN). Default is set to '1' (using RXD= UBPRXD) after power-on-reset. |
| 6          | SIELSE       | SIE Low-Speed Enable: (Reserved for test only)<br>The bit is used to select SIE operated either in Low-Speed Mode or in Full-Speed Mode. Set '0' SIE operate in Full-Speed Mode; set '1', SIE operates in Low-Speed Mode. Normally, Hub/SIE is default set to full-speed mode (i.e. cleared to '0') after power-on-reset.  |
| 5          | SECKPAT      | SIE CRC16-Based EOP Check Patch Enable: (Reserved for test only)<br>This bit is used by FW to enable the patch for SIE detecting CRC16-based EOP=K/J001 with K/J=(80+80)ns and 00=3*SE0=(160+80)ns. '1' is patch enabled; '0' is patch disabled. Default is set to '1' after POR.  |
| 4          | STODPAT      | SIE Time-Out Detection Patch Enable: (Reserved for test only)<br>This bit is used by FW to enable the patch for SIE detecting time_out_16 bug during waiting for CRC5-based EOP. '1' is patch enabled; '0' is patch disabled. Default is set to '1' after POR.   |
| 3:2        | SEOSMOD1:0   | SIE EOS Detection Modes: (Reserved for test only)<br>These bits are used to select one of the following SIE EOS (End-Of-Sync) detection modes:<br>00 – SYNC Pattern = “- -JKJJK” (Default)<br>01 – SYNC Pattern = “- -J -JJK”<br>10 – SYNC Pattern = “- - -KJJK”<br>11 – SYNC Pattern = “- - - -JJK”   |
| 1:0        | SEOPMOD1:0   | Repeater EOP Detection Modes: (Reserved for test only)<br>These bits are used to select one of the following repeater EOP detection modes:<br>00 – Normal Mode (Default)<br>01 – Relax Mode 1<br>10 – Relax Mode 2<br>11 – Relax Mode 3  |

# W81E381D/W81E381AD



## 4.5.20 Register Descriptions - SC Interrupt SFRs (AA)

**SCIER**

Address: S:AAH  
Reset State: 0000 0000H

*Interrupt Control Register of Smart Card Reader (SCIEL). Contains all control for interrupt enable from smart card interface.*

|   |        |     |   |     |      |      |   |
|---|--------|-----|---|-----|------|------|---|
| 7 | 6      | 5   | 4 | 3   | 2    | 1    | 0 |
| - | ESCPTI | WCE | - | PBE | RDRE | EXIE | - |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved  |
| 6          | ESCPTI       | 1: Enable SC present toggle interrupt request<br>0: Disable SC present toggle interrupt request |
| 5          | WCE          | 1: Enable wrong card interrupt<br>0: Disable wrong card interrupt                               |
| 4          | -            | Reserved  |
| 3          | RDRE         | To enable RX data ready interrupt   |
| 2          | PBE          | To enable the parity check function   |
| 1          | EXIE         | To enable external interrupt  |
| 0          | -            | Reserved  |

# W81E381D/W81E381AD



## 4.5.21 Register Descriptions - SC Interrupt SFRs (AB)

**SCISR**

Address: S:ABH  
Reset State: 0000 0000H

*Interrupt Status Register of Smart Card Reader (SCISL). Contains all interrupt status of smart card interface.*

|   |       |     |     |      |     |     |        |
|---|-------|-----|-----|------|-----|-----|--------|
| 7 | 6     | 5   | 4   | 3    | 2   | 1   | 0      |
| - | SCPTI | WCI | TDI | PBER | RDR | EXI | EXI_16 |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | -            | Reserved   |
| 6          | SCPTI        | The Toggle Interrupt of SCPRSNT  |
| 5          | WCI          | An interrupt of Wrong Card or abnormal card                              |
| 4          | TDI          | Ending of TX data interrupt (rising at guard time ending)                |
| 3          | RDR          | Received Data buffer Ready Interrupt (rising at parity check bit ending) |
| 2          | PBER         | Parity Bit eRror Interrupt   |
| 1          | EXI          | EXternal Interrupt input from P1.7                                       |
| 0          | EXI_16       | Remote wakeup input from P1.6  |

# W81E381D/W81E381AD



## 4.5.22 Register Descriptions - SC Control SFRs (A3)

**SCSR**

Address: S:A3H  
Reset State: 0000 0000H

*Status Register of Smart Card Reader (SCSR).*

|   |   |   |   |         |   |   |    |
|---|---|---|---|---------|---|---|----|
| 7 | 6 | 5 | 4 | 3       | 2 | 1 | 0  |
| - | - | - | - | SCPRSNT | - | - | CA |

| Bit Number | Bit Mnemonic | Function                          |
|------------|--------------|-----------------------------------|
| 7          | -            | Reserved                          |
| 6          | -            | Reserved                          |
| 5          | -            | Reserved                          |
| 4          | -            | Reserved                          |
| 3          | SCPRSNT      | Smart Card is PReSeNT             |
| 2          | -            | Reserved                          |
| 1          | -            | Reserved                          |
| 0          | CA           | Read/Write Cycle Active indicator |

# W81E381D/W81E381AD



## 4.5.24 Register Descriptions - SC Control SFRs (AC)

**SCCR**

Address: S:ACH  
Reset State: 0001 0110H

*Control Register of Smart Card Reader (SCCR).*

|   |   |   |                |              |              |            |               |
|---|---|---|----------------|--------------|--------------|------------|---------------|
| 7 | 6 | 5 | 4              | 3            | 2            | 1          | 0             |
| - | - | - | <b>CLKSTPL</b> | <b>S_CK1</b> | <b>S_CK0</b> | <b>EPE</b> | <b>EXINTH</b> |

| Bit Number     | Bit Mnemonic | Function   |                |  |    |        |    |      |    |      |    |      |
|----------------|--------------|--|----------------|--|----|--------|----|------|----|------|----|------|
| 7              | -            | Reserved   |                |  |    |        |    |      |    |      |    |      |
| 6              | -            | Reserved   |                |  |    |        |    |      |    |      |    |      |
| 5              | -            | Reserved   |                |  |    |        |    |      |    |      |    |      |
| 4              | CLKSTPL      | SC clock polarity control bit during stopping clock (corporate with CLKSTP of SCECR)<br>1: Indicate the SCCLK pin stays in High as clock stopped<br>0: Indicate the SCCLK pin stays in Low as clock stopped  |                |  |    |        |    |      |    |      |    |      |
| 3              | S_CK1        | Bit 1 of selecting the SC clock frequency  |                |  |    |        |    |      |    |      |    |      |
| 2              | S_CK0        | Bit 0 of selecting the SC clock frequency<br><table border="1" style="margin-left: 20px;"> <tr> <td>{S_CK1, S_CK0}</td> <td></td> </tr> <tr> <td>00</td> <td>1.5MHz</td> </tr> <tr> <td>01</td> <td>3MHz</td> </tr> <tr> <td>10</td> <td>4MHz</td> </tr> <tr> <td>11</td> <td>6MHz</td> </tr> </table> | {S_CK1, S_CK0} |  | 00 | 1.5MHz | 01 | 3MHz | 10 | 4MHz | 11 | 6MHz |
| {S_CK1, S_CK0} |              |  |                |  |    |        |    |      |    |      |    |      |
| 00             | 1.5MHz       |  |                |  |    |        |    |      |    |      |    |      |
| 01             | 3MHz         |  |                |  |    |        |    |      |    |      |    |      |
| 10             | 4MHz         |  |                |  |    |        |    |      |    |      |    |      |
| 11             | 6MHz         |  |                |  |    |        |    |      |    |      |    |      |
| 1              | EPE          | 1: To do even parity check<br>0: To do odd parity check  |                |  |    |        |    |      |    |      |    |      |
| 0              | EXINTH       | The polarity of external interrupt<br>1: Indicate external interrupt input is High active<br>0: Indicate external interrupt input is Low active  |                |  |    |        |    |      |    |      |    |      |

# W81E381D/W81E381AD



## 4.5.25 Register Descriptions - SC Control SFRs (AD)

**SCECR**

Address: S:ADH  
Reset State: 0000 0000H

*Extended Control Register of Smart Card Reader (SCECR).*

|               |               |               |          |          |               |             |               |
|---------------|---------------|---------------|----------|----------|---------------|-------------|---------------|
| 7             | 6             | 5             | 4        | 3        | 2             | 1           | 0             |
| <b>CRDRST</b> | <b>PWRENP</b> | <b>VCC_EN</b> | <b>-</b> | <b>-</b> | <b>CLKSTP</b> | <b>SCIO</b> | <b>SCRRST</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | CRDRST       | To issue a reset signal to SC<br>1: High -> Low<br>0: Low -> High  |
| 6          | PWRENP       | To determine the polarity of the VCC_EN signal<br>If WCE=0 => 1: Positive, 0: Negative<br>If WCE=1 => 0: Positive, 1: Negative |
| 5          | VCC_EN       | 1: Enable SC power supply<br>0: Disable SC power supply  |
| 4          | -            | Reserved   |
| 3          | -            | Reserved   |
| 2          | CLKSTP       | 1: To stop the SC clock<br>0: To start the SC clock  |
| 1          | SCIO         | SCIO direction control signal.<br>1: Transmit data to card<br>0: Receive data from card  |
| 0          | SCRRST       | Resynchronize SC interface (reload default value to SC related registers, include itself)                                      |



# W81E381D/W81E381AD



## 4.5.26 Register Descriptions - SC Control SFRs (AE, A4)

**SCGTR**

Address: S:AEH  
Reset State: 0000 0000H

*Guard Time Register of Smart Card Reader (SCGTR).*

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
| <b>BIT 7</b> | <b>BIT 6</b> | <b>BIT 5</b> | <b>BIT 4</b> | <b>BIT 3</b> | <b>BIT 2</b> | <b>BIT 1</b> | <b>BIT 0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|------------|
| 7          | BIT 7        | Data Bit 7 |
| 6          | BIT 6        | Data Bit 6 |
| 5          | BIT 5        | Data Bit 5 |
| 4          | BIT 4        | Data Bit 4 |
| 3          | BIT 3        | Data Bit 3 |
| 2          | BIT 2        | Data Bit 2 |
| 1          | BIT 1        | Data Bit 1 |
| 0          | BIT 0        | Data Bit 0 |

**SCBDR**

Address: S:A4H  
Reset State: 0000 0001H

*Baud Rate Divider Register of Smart Card Reader (SCBDR).*

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
| <b>BIT 7</b> | <b>BIT 6</b> | <b>BIT 5</b> | <b>BIT 4</b> | <b>BIT 3</b> | <b>BIT 2</b> | <b>BIT 1</b> | <b>BIT 0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|------------|
| 7          | BIT 7        | Data bit 7 |
| 6          | BIT 6        | Data bit 6 |
| 5          | BIT 5        | Data bit 5 |
| 4          | BIT 4        | Data bit 4 |
| 3          | BIT 3        | Data bit 3 |
| 2          | BIT 2        | Data bit 2 |
| 1          | BIT 1        | Data bit 1 |
| 0          | BIT 0        | Data bit 0 |



# W81E381D/W81E381AD

## 4.5.27 Register Descriptions - SC Control SFRs (A5)

**SCCBR**

Address: S:A5H  
Reset State: 0000 0001H

*Clock Base Register of Smart Card Reader (SCCBR).*

|              |              |              |              |              |              |              |              |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| 7            | 6            | 5            | 4            | 3            | 2            | 1            | 0            |
| <b>BIT 7</b> | <b>BIT 6</b> | <b>BIT 5</b> | <b>BIT 4</b> | <b>BIT 3</b> | <b>BIT 2</b> | <b>BIT 1</b> | <b>BIT 0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|------------|
| 7          | BIT 7        | Data bit 7 |
| 6          | BIT 6        | Data bit 6 |
| 5          | BIT 5        | Data bit 5 |
| 4          | BIT 4        | Data bit 4 |
| 3          | BIT 3        | Data bit 3 |
| 2          | BIT 2        | Data bit 2 |
| 1          | BIT 1        | Data bit 1 |
| 0          | BIT 0        | Data bit 0 |

Ps: The value of (SCCBR X SCBDR) is the same as the definition of Q (Q=F/D) in ISO-7816 specification.

# W81E381D/W81E381AD



## 4.5.28 Register Descriptions - SC Data SFRs (A6, A7)

**SCRDR**

Address: S:A6H  
Reset State: 0000 0000H

*Received Data Register of Smart Card Reader (SCRDR).*

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
| <b>RD 7</b> | <b>RD 6</b> | <b>RD 5</b> | <b>RD 4</b> | <b>RD 3</b> | <b>RD 2</b> | <b>RD 1</b> | <b>RD 0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|------------|
| 7          | RD 7         | Data bit 7 |
| 6          | RD 6         | Data bit 6 |
| 5          | RD 5         | Data bit 5 |
| 4          | RD 4         | Data bit 4 |
| 3          | RD 3         | Data bit 3 |
| 2          | RD 2         | Data bit 2 |
| 1          | RD 1         | Data bit 1 |
| 0          | RD 0         | Data bit 0 |

**SCTDR**

Address: S:A7H  
Reset State: 0000 0000H

*Transmitted Data Register of Smart Card Reader (SCTDR).*

|             |             |             |             |             |             |             |             |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 7           | 6           | 5           | 4           | 3           | 2           | 1           | 0           |
| <b>TD 7</b> | <b>TD 6</b> | <b>TD 5</b> | <b>TD 4</b> | <b>TD 3</b> | <b>TD 2</b> | <b>TD 1</b> | <b>TD 0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|------------|
| 7          | TD 7         | Data bit 7 |
| 6          | TD 6         | Data bit 6 |
| 5          | TD 5         | Data bit 5 |
| 4          | TD 4         | Data bit 4 |
| 3          | TD 3         | Data bit 3 |
| 2          | TD 2         | Data bit 2 |
| 1          | TD 1         | Data bit 1 |
| 0          | TD 0         | Data bit 0 |

# W81E381D/W81E381AD



## 4.5.29 Register Descriptions – ISP Registers (C4, C5)

**SFRAL**

Address: S:C4H  
Reset State: 0000 0000H

*Special Function Register Address Low Register (SFRAL). Low-byte of programming address for on-chip flash.*

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| <b>LA7</b> | <b>LA6</b> | <b>LA5</b> | <b>LA4</b> | <b>LA3</b> | <b>LA2</b> | <b>LA1</b> | <b>LA0</b> |

| Bit Number | Bit Mnemonic | Function |
|------------|--------------|----------|
| 7          | LA7          | Bit 7    |
| 6          | LA6          | Bit 6    |
| 5          | LA5          | Bit 5    |
| 4          | LA4          | Bit 4    |
| 3          | LA3          | Bit 3    |
| 2          | LA2          | Bit 2    |
| 1          | LA1          | Bit 1    |
| 0          | LA0          | Bit 0    |

**SFRAH**

Address: S:C5H  
Reset State: 0000 0000H

*Special Function Register Address High Register (SFRAH). High-byte of programming address for on-chip flash.*

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| <b>HA7</b> | <b>HA6</b> | <b>HA5</b> | <b>HA4</b> | <b>HA3</b> | <b>HA2</b> | <b>HA1</b> | <b>HA0</b> |

| Bit Number | Bit Mnemonic | Function |
|------------|--------------|----------|
| 7          | HA7          | Bit 7    |
| 6          | HA6          | Bit 6    |
| 5          | HA5          | Bit 5    |
| 4          | HA4          | Bit 4    |
| 3          | HA3          | Bit 3    |
| 2          | HA2          | Bit 2    |
| 1          | HA1          | Bit 1    |
| 0          | HA0          | Bit 0    |

# W81E381D/W81E381AD



## 4.5.30 Register Descriptions – ISP Registers (C6, C7)

**SFRFD**

Address: S:C6H  
Reset State: 0000 0000H

*Special Function Register Flash Data Register (SFRFD). The programming data register for on-chip flash.*

|            |            |            |            |            |            |            |            |
|------------|------------|------------|------------|------------|------------|------------|------------|
| 7          | 6          | 5          | 4          | 3          | 2          | 1          | 0          |
| <b>FD7</b> | <b>FD6</b> | <b>FD5</b> | <b>FD4</b> | <b>FD3</b> | <b>FD2</b> | <b>FD1</b> | <b>FD0</b> |

| Bit Number | Bit Mnemonic | Function |
|------------|--------------|----------|
| 7          | FD7          | Bit 7    |
| 6          | FD6          | Bit 6    |
| 5          | FD5          | Bit 5    |
| 4          | FD4          | Bit 4    |
| 3          | FD3          | Bit 3    |
| 2          | FD2          | Bit 2    |
| 1          | FD1          | Bit 1    |
| 0          | FD0          | Bit 0    |

**SFRCN**

Address: S:C7H  
Reset State: 0011 0000H

*Special Function Register Flash Control Register (SFRCN). The programming control register for on-chip flash.*

|   |   |            |            |              |              |              |              |
|---|---|------------|------------|--------------|--------------|--------------|--------------|
| 7 | 6 | 5          | 4          | 3            | 2            | 1            | 0            |
| - | - | <b>OEN</b> | <b>CEN</b> | <b>CTRL3</b> | <b>CTRL2</b> | <b>CTRL1</b> | <b>CTRL0</b> |

| Bit Number | Bit Mnemonic | Function   |
|------------|--------------|--|
| 7          | -            | Reserved   |
| 6          | -            | Reserved   |
| 5          | OEN          | Output enable control of flash memory<br>0/1: Enable/Disable |
| 4          | CEN          | Chip enable control of flash memory<br>0/1: Enable/Disable   |
| 3          | CTRL3        | Bit 3 of flash memory control mode                           |
| 2          | CTRL2        | Bit 2 of flash memory control mode                           |
| 1          | CTRL1        | Bit 1 of flash memory control mode                           |
| 0          | CTRL0        | Bit 0 of flash memory control mode                           |

Note: Refer the ISP related SFR usage in Section 4.6

# W81E381D/W81E381AD



## 4.5.31 Register Descriptions – uC Control Registers (CF)

**CHPCON**

Address: S:CFH  
Reset State: 0000 0000H

*On-chip Programming Control Register (CHPCON). Select the delay period of oscillation when waking up from power-down mode.*

|   |   |   |   |   |   |   |         |
|---|---|---|---|---|---|---|---------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0       |
| - | - | - | - | - | - | - | FPROGEN |

| Bit Number | Bit Mnemonic | Function  |
|------------|--------------|---|
| 7          | -            | Reserved  |
| 6          | -            | Reserved  |
| 5          | -            | Reserved  |
| 4          | -            | Reserved  |
| 3          | -            | Reserved  |
| 2          | -            | Reserved  |
| 1          | -            | Reserved  |
| 0          | FPROGEN      | <p>MTP-ROM Programming Enable</p> <p>1: Enable. The micro controller switches to the programming flash mode after entering the idle mode and waken up from interrupt. The microcontroller will execute the loader program while in on-chip programming mode.</p> <p>0: Disable. The on-chip flash memory is read-only. In-system program ability is disabled.</p> |

# W81E381D/W81E381AD



## 4.5.32 Register Descriptions – uC Control Registers (D4, D5)

**PMPR2**

Address: S:D4H  
Reset State: 0000 0000H

*Program Memory Protection Register2 (PMPR2). To configure the blocks of flash memory under protection.*

|   |   |   |   |   |   |      |      |
|---|---|---|---|---|---|------|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1    | 0    |
| - | - | - | - | - | - | HBP1 | HBP0 |

| Bit Number | Bit Mnemonic | Function                       |
|------------|--------------|--------------------------------|
| 7          | -            | Reserved                       |
| 6          | -            | Reserved                       |
| 5          | -            | Reserved                       |
| 4          | -            | Reserved                       |
| 3          | -            | Reserved                       |
| 2          | -            | Reserved                       |
| 1          | HBP1         | To protect 0x4800-0x4fff block |
| 0          | HBP0         | To protect 0x4000-0x47ff block |

**PMPR1**

Address: S:D5H  
Reset State: 0000 0000H

*Program Memory Protection Register1 (PMPR1). To configure the blocks of flash memory under protection.*

|      |      |      |      |      |      |      |      |
|------|------|------|------|------|------|------|------|
| 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
| LBP7 | LBP6 | LBP5 | LBP4 | LBP3 | LBP2 | LBP1 | LBP0 |

| Bit Number | Bit Mnemonic | Function                       |
|------------|--------------|--------------------------------|
| 7          | LBP7         | To protect 0x3800-0x3fff block |
| 6          | LBP6         | To protect 0x3000-0x37ff block |
| 5          | LBP5         | To protect 0x2800-0x2fff block |
| 4          | LBP4         | To protect 0x2000-0x27ff block |
| 3          | LBP3         | To protect 0x1800-0x1fff block |
| 2          | LBP2         | To protect 0x1000-0x17ff block |
| 1          | LBP1         | To protect 0x0800-0x0fff block |
| 0          | LBP0         | To protect 0x0000-0x07ff block |

# W81E381D/W81E381AD



## 4.6 MTP-ROM PROGRAMMING

The context of flash in W81E381 is empty by default. At the first use, you must program the flash by external writer device. For programming the flash by external device, the W81E381 must enter the flash-programming mode by power on reset. The setting conditions and the timing are following. Especially to illustrate, if you only want to erase one block (512 bytes), not to erase all (20k bytes), you have to use the in-system-programming function to do the operation.

| Mode                | SFRAH<6><br>(A<14>) | SFRCN<5><br>(FOEN) | SFRCN<4><br>(FCEN) | SFRCN<3:0><br>(FCTRL<3:0>) | SFRAH, SFRAL<br>(A<13:0>) | SFRFD<br>(D<7:0>) |
|---------------------|---------------------|--------------------|--------------------|----------------------------|---------------------------|-------------------|
| Standby             | X                   | 1                  | 1                  | X                          | X                         | X                 |
| Read 16KB APROM     | 0                   | 0                  | 0                  | 0000                       | Address in                | Data out          |
| Read 4KB LDRROM     | 1                   | 0                  | 0                  | 0000                       | Address in                | Data out          |
| Program 16KB APROM  | 0                   | 1                  | 0                  | 0001                       | Address in                | Data in           |
| Program 4KB LDRROM  | 1                   | 1                  | 0                  | 0001                       | Address in                | Data in           |
| Check board         | X                   | 1                  | 0                  | 1000                       | Address in                | Data in           |
| Erase All           | X                   | 1                  | 0                  | 0110                       | X                         | X                 |
| Erase 16KB APROM    | 0                   | 1                  | 0                  | 0010                       | X                         | X                 |
| Erase 512Byte       | 0                   | 1                  | 0                  | 1111                       | Address in                | X                 |
| Read ROM_MAP        | 0                   | 0                  | 0                  | 0011                       | FFFF H                    | Data out          |
| Program ROM_MAP     | 0                   | 1                  | 0                  | 0100                       | FFFF H                    | Data in           |
| Erase ROM_MAP       | 0                   | 1                  | 0                  | 0101                       | FFFF H                    | X                 |
| Read Company ID     | X                   | 0                  | 0                  | 1011                       | X                         | DA H              |
| Read Device ID      | X                   | 0                  | 0                  | 1100                       | X                         | 62H / 61H         |
| 16KB program verify | 0                   | 0                  | 0                  | 1010                       | Address in                | Data out          |
| 4KB program verify  | 1                   | 0                  | 0                  | 1010                       | Address in                | Data out          |
| 16KB erase verify   | 0                   | 0                  | 0                  | 1001                       | Address in                | Data out          |
| 4KB erase verify    | 1                   | 0                  | 0                  | 1001                       | Address in                | Data out          |
| 16KB VT mode        | 0                   | 0                  | 0                  | 1101                       | Address in                | Current           |
| 4kB VT mode         | 1                   | 0                  | 0                  | 1101                       | Address in                | Current           |
| 16KB Read-Disturb   | 0                   | 0                  | 0                  | 1110                       | Address in                | Data out          |
| 4KB Read-Disturb    | 1                   | 0                  | 0                  | 1110                       | Address in                | Data out          |



# W81E381D/W81E381AD

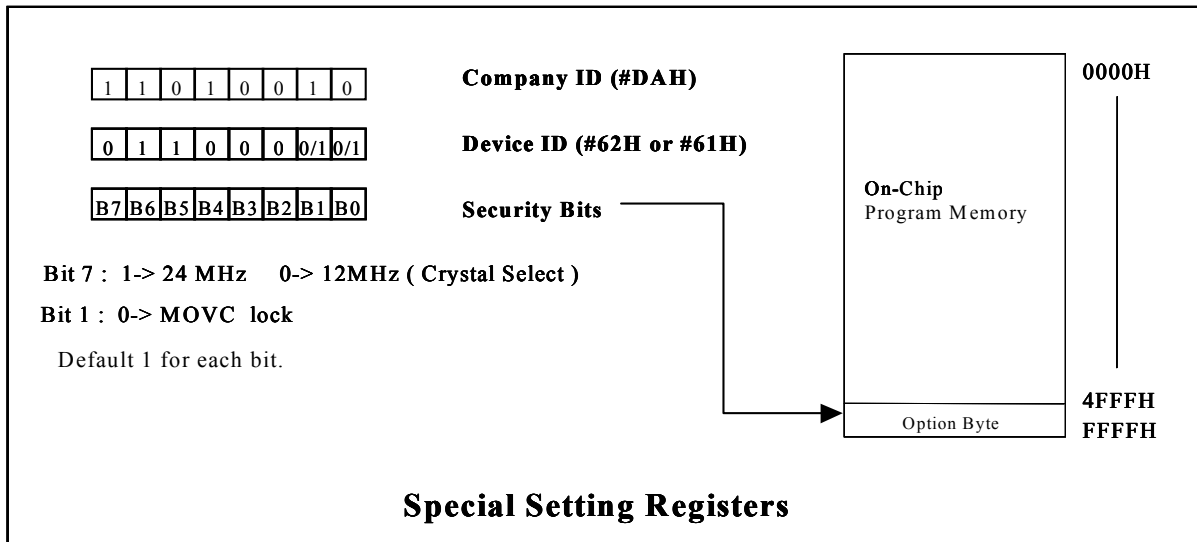


## 5. SECURITY

During the on-chip MTP-ROM programming mode, the MTP-ROM can be programmed and verified repeatedly. Until the code inside the MTP-ROM is confirmed OK, the code can be protected. The protection of MTP-ROM and those operations on it are described below.

W81E381 has some Special Setting Registers, including the Security Register and Company/Device ID Registers, which can't be accessed in programming mode. Those bits of the Security Registers can't be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The contents of the Company ID and Device ID registers have been set in factory.

**The Security Register is located at the FFFFH.**



### MOVC Lock:

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the program to be downloaded using this instruction if the program needs to jump outside to get data. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code in the external memory, but it will not be able to access code in the internal memory. A MOVC instruction in internal program memory space will always be able to access code in both internal and external memory. If this bit is logic 1 (default), there is no restriction on the MOVC instruction.

### Crystal Select

If this bit is set to logic 1, uC uses internal 24Mhz input. If this bit is set to logic 0, W81E381 could use external crystal source.

# W81E381D/W81E381AD



## 6. ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 4.0V to 5.25V, Ta=0° to 70°C

| PARAMETER   | Symbol                                   | Conditions                         | Min         | Max       | Unit     |
|---|--|------------------------------------|-------------|-----------|----------|
| VCC Supply Current  | I <sub>cc</sub>                          |                                    |             | TBD       | mA       |
| VCC Suspend Current   | I <sub>pd</sub>                          |                                    |             | TBD       | uA       |
| Logic Output High   | VOH                                      | IOH=-3mA                           | 2.4         | VCC       | V        |
| Logic Output Low  | VOL                                      | IOL=3mA                            |             | 0.4       | V        |
| Logic Input High  | VIH                                      |                                    | 2.0         |           | V        |
| Logic Input Low   | VIL                                      |                                    |             | 0.8       | V        |
| Logic Input Leakage Current   |  | Ta=70°C                            |             | 10        | uA       |
| <b>USB CHARACTERISTICS</b>  |  | Note 8                             |             |           |          |
| Leakage Current:  |  |                                    |             |           |          |
| Hi-Z State Output Leakage   | ILO                                      | V < V <sub>IN</sub> < 3.3 V        | -10         | +10       | uA       |
| Input Levels:   |  |                                    |             |           |          |
| Differential Input Sensitivity  | VDI                                      | (D+)-(D-)                          | 0.2         |           | V        |
| Single Ended Signal "0"   | VSE0                                     |                                    | 0.8         | 2.0       | V        |
| Differential Common Mode Range  | V <sub>CM</sub>                          | Includes VDI range                 | 0.8         | 2.5       |          |
| Output Levels:  |  |                                    |             |           |          |
| Driver Output Low   | VOLU                                     | RL of 1.5 kΩ to 3.6 V              |             | 0.3       | V        |
| Driver Output High  | VOHU                                     | RL of 15 kΩ to GND                 | 2.8         | 3.6       | V        |
| Output Signal Crossover Voltage   | V <sub>CRS</sub>                         |                                    | 1.3         | 2.0       | V        |
| Capacitance:  |  |                                    |             |           |          |
| Transceiver Capacitance   | CIN                                      | Pin to GND                         |             | 20        | pF       |
| Full Speed Timings:   |  |                                    |             |           |          |
| Output Rise/Fall Times  | t <sub>R</sub> / t <sub>F</sub>          | Note 1, 4 (C <sub>L</sub> = 50 pF) | 4           | 20        | ns       |
| Source Differential Driver Jitter to Next Transition<br>/ to Paired Transition                | t <sub>DJ1</sub><br>/ t <sub>DJ2</sub>   | Note 2, 3                          | -3.5<br>/-4 | 3.5<br>/4 | ns<br>ns |
| Differential to EOP transition Skew   | t <sub>DEOP</sub>                        | Note 3                             | -2          | 5         | ns       |
| Hub Differential Data Delay(without cable)  | t <sub>HDD2</sub>                        | Note 2,3,5                         |             | 44        | ns       |
| Hub Differential Driver Jitter to Next Transition<br>/ to Paired Transition (including cable) | t <sub>HDJ1</sub><br>/ t <sub>HDJ2</sub> | Note 2,3,5                         | -3<br>/-1   | 3<br>/1   | ns<br>ns |
| Data bit width distortion after SOP   | t <sub>SOP</sub>                         | Note 3,5                           | -5          | 5         | ns       |
| Hub SE0 Delay Relative to t <sub>HDD</sub>  | t <sub>EOPD</sub>                        | Note 3,5                           | 0           | 15        | ns       |
| Hub EOP Output Width Skew   | t <sub>HESK</sub>                        | Note 3,5                           | -15         | 15        | ns       |

Note 1: Measured from 10% to 90% of the data signal.

Note 2: Timing difference between the differential signals.

Note 3: Measured at crossover point of differential data signals.

Note 4: The rising and falling edges should be smoothly transition (monotonic).

Note 5: Full Speed timing has a 1.5 kΩ pull-up to 2.8 V on the D+ (DP) data line.

Note 7: The maximum load specification is the maximum effective capacitive load allowed that meets the target hub VBUS droop of 330 mV.

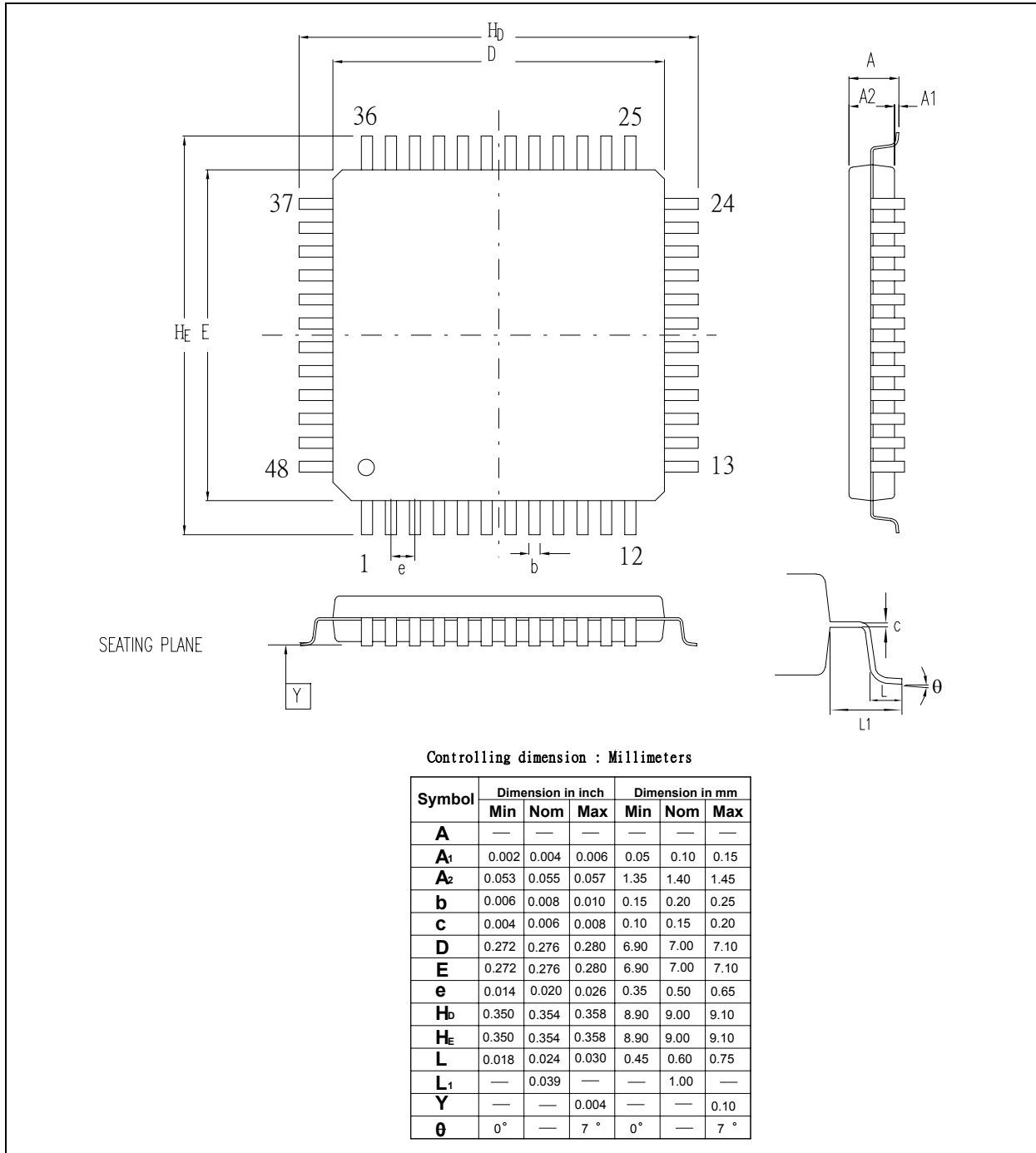
Note 8: Other USB Electrical Characteristics refer to USB spec Rev1.1 Sec7.3.2 and Sec7.3.3.

# W81E381D/W81E381AD



## 7. MECHANICAL INFORMATION

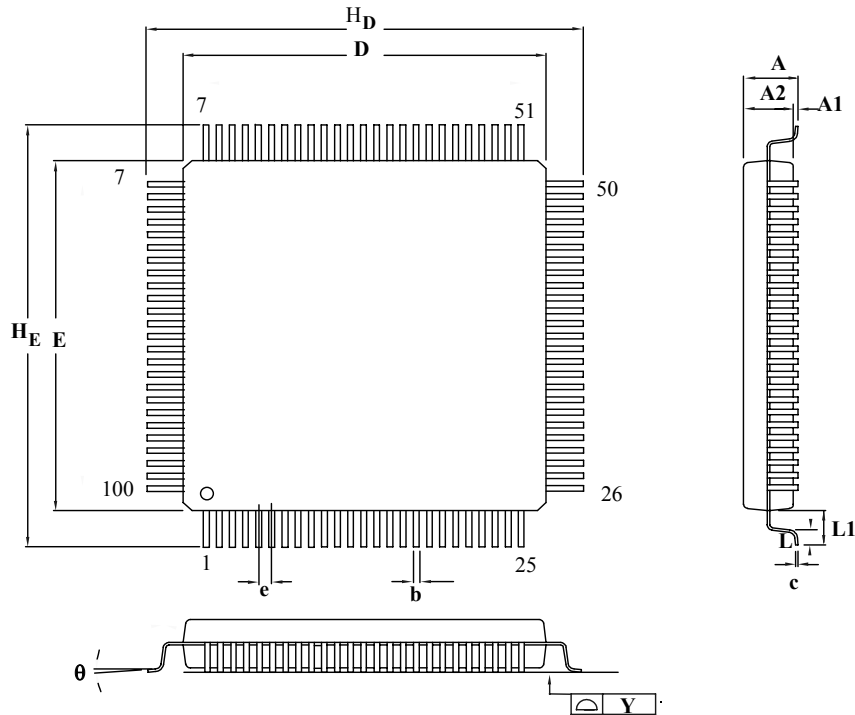
### 7.1 W81E381D 48 LQFP (7x7x1.4mm footprint 2.0mm) PACKAGE



# W81E381D/W81E381AD



## 7.2 W81E381AD 100 LQFP (14x14x1.4 mm footprint 2.0mm) PACKAGE



Controlling Dimension : Millimeters

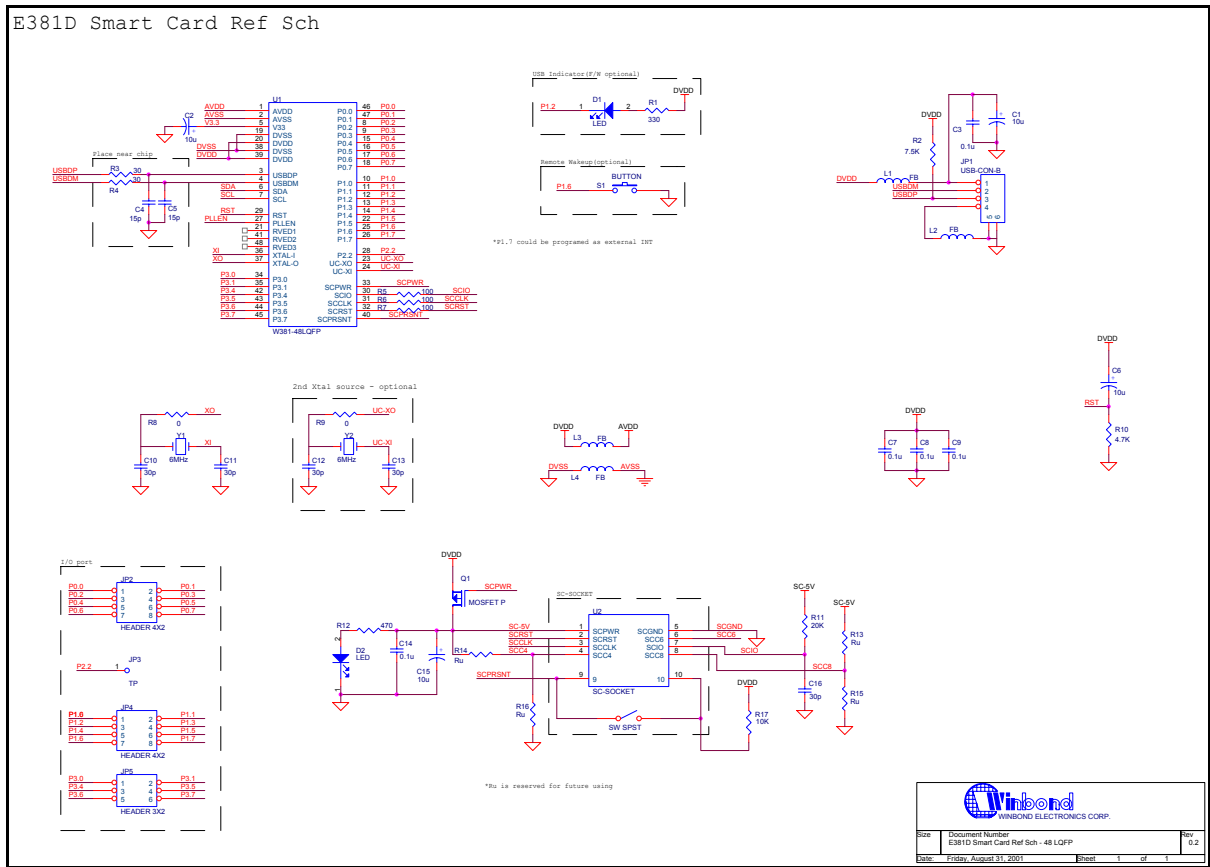
| Symbol         | Dimension in inch |       |       | Dimension in mm |       |       |
|----------------|-------------------|-------|-------|-----------------|-------|-------|
|                | Min               | Nom   | Max   | Min             | Nom   | Max   |
| A              | —                 | —     | 0.063 | —               | —     | 1.60  |
| A1             | 0.002             | —     | —     | 0.05            | —     | —     |
| A              | 0.053             | 0.055 | 0.057 | 1.35            | 1.40  | 1.45  |
| b              | 0.007             | 0.009 | 0.011 | 0.17            | 0.22  | 0.27  |
| c              | 0.004             | 0.006 | 0.008 | 0.10            | 0.15  | 0.20  |
| D              | 0.547             | 0.551 | 0.556 | 13.90           | 14.00 | 14.10 |
| E              | 0.547             | 0.551 | 0.556 | 13.90           | 14.00 | 14.10 |
| e              | —                 | 0.020 | —     | —               | 0.50  | —     |
| H <sub>D</sub> | 0.622             | 0.630 | 0.638 | 15.80           | 16.00 | 16.20 |
| H <sub>E</sub> | 0.622             | 0.630 | 0.638 | 15.80           | 16.00 | 16.20 |
| L              | 0.018             | 0.024 | 0.030 | 0.45            | 0.60  | 0.75  |
| L1             | —                 | 0.039 | —     | —               | 1.00  | —     |
| y              | —                 | —     | 0.004 | —               | —     | 0.10  |
| θ              | 0°                | —     | 7°    | 0°              | —     | 7°    |

# W81E381D/W81E381AD



## 8. TYPICAL APPLICATION

### 8.1 W81E381D reference schematic





# W81E381D/W81E381AD



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