W83697SF

WINBOND I/O

W83697SF Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.	04/16/01	0.50	0.50	First published
2	111	04/27/01	0.51	0.51	Update the Top Marking
3					
4					
5					
6 7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Winbond Electronics Corp.

PRELIMINARY

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Winbond Electronics Corp.

PRELIMINARY

GENERAL DESCRIPTION

The W83697SF is evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (**Low Pin Count**) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83697SF's integration of Game Port and MIDI Port. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

As Smart Card application is gaining more and more attention, W83697SF also implements a smart card reader interface featuring Smart wake-up function. This smart card reader interface fully meets the ISO7816 and PC/SC (Personal Computer/Smart Card Workgroup) standards. W83697SF provides a minimum external components and lowest cost solution for smart card applications.

The disk drive adapter functions of W83697SF include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83697SF greatly reduces the number of components required for interfacing with floppy disk drives. The W83697SF supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data tranSFer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83697SF provides two high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. Both UARTs provide legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems. In addition, the W83697SF provides IR functions: **IrDA 1.0** (**SIR** for 1.152K bps) and TV remote IR (**Consumer IR**, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83697SF supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98 TM, which makes system resource allocation more efficient than ever.

The W83697SF provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured

to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83697SF is made to fully comply with **Microsoft® PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.**

The W83697SF contains a game port and a MIDI port. The game port is designed to support 2 joysticks and can be applied to all standard PC game control devices, They are very important for a entertainment or consumer computer.

The W83697SF provides Flash ROM interface . That can support up to 4M legacy flash ROM.

Moreover, W83697SF support 3 sets PWM Fan Speed Control, which are very important for a high-end computer system to work stably and properly.

FEATURES

General

- Meet LPC Spec. 1.01
- Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)
- Include all the features of Winbond I/O W83877TF
- Integrate Smart Card functions
- Compliant with Microsoft PC98/PC99 Hardware Design Guide
- Support DPM (Device Power Management), ACPI
- Programmable configuration settings
- Single 24 or 48 MHz clock input

FDC

- Compatible with IBM PC AT disk drive systems
- Variable write pre-compensation with track selectable capability
- Support vertical recording format
- DMA enable logic
- 16-byte data FIFOs
- Support floppy disk drives and tape drives
- Detects all overrun and underrun conditions
- Built-in address mark detection circuit to simplify the read electronics
- FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)
- Support up to four 3.5-inch or 5.25-inch floppy disk drives
- Completely compatible with industry standard 82077
- 360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate
- Support **3-mode FDD, and its Win95/98 driver**

UART

- Two high-speed 16550 compatible UARTs with 16-byte send/receive FIFOs
- MIDI compatible
- Fully programmable serial-interface characteristics:
  --- 5, 6, 7 or 8-bit characters
  --- Even, odd or no parity bit generation/detection
  --- 1, 1.5 or 2 stop bits generation

- Internal diagnostic capabilities:
  --- Loop-back controls for communications link fault isolation
  --- Break, parity, overrun, framing error simulation
- Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)
- Maximum baud rate up to **921k bps** for 14.769 MHz and 1.5M bps for 24 MHz

Infrared

- Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps
- Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps
- Support Consumer IR with Wake-Up function.

Parallel Port

- Compatible with IBM parallel port
- Support PS/2 compatible bi-directional parallel port
- Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification
- Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification
- Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port
- Enhanced printer port back-drive current protection

Game Port

- Support two separate Joysticks
- Support every Joystick two axes (X,Y) and two buttons (S1,S2) controllers

MIDI Port

- The baud rate is 31.25 Kbaud
- 16-byte input FIFO
- 16-byte output FIFO

Flash ROM Interface

- Support up to 4M flash ROM

General Purpose I/O Ports

- 60 programmable general purpose I/O ports
- General purpose I/O ports can serve as simple I/O ports, watch dog timer output, power LED output, infrared I/O pins, suspend LED output, Beep output
- Functional in power down mode

Smart Card Reader Interface

- ISO7816 protocol compliant
- PC/SC T=0, T=1 compliant

Fan Speed Control

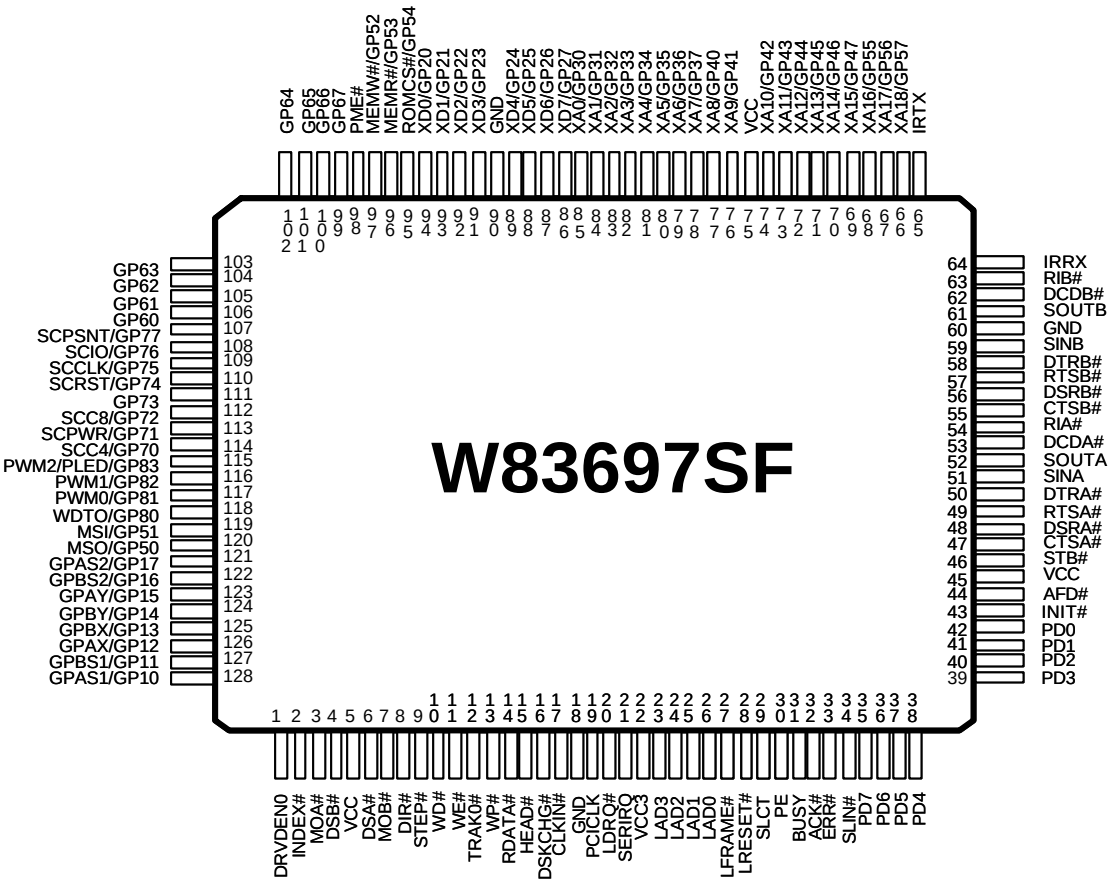
- 3 Sets PWM Fan Speed Control

Package

- 128-pin PQFP

PRELIMINARY

PIN CONFIGURATION FOR 697SF



1.0 PIN DESCRIPTION

Note: Please refer to Section 13.2 DC CHARACTERISTICS for details.

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{16t} - TTL level bi-directional pin with 16 mA source-sink capability

$I/O12_{ts}$ - TTL level output pin with 12 mA source-sink capability and Schmitt-trigger input pin

I/O_{16ts} - TTL level output pin with 16 mA source-sink capability and Schmitt-trigger input pin

I/O_{24cs} - TTL level output pin with 24 mA source-sink capability and CMOS level Schmitt-trigger input pin

I/OD_{16t} - TTL level open-drain output pin with 16 mA source-sink capability and input pin

I/OD_{24cs} - TTL level open-drain output pin with 24 mA source-sink capability and CMOS level Schmitt-trigger input pin

I/O_{24tp3} - 3.3V TTL level bi-directional pin with 24 mA source-sink capability

O_{16} - Output pin with 16 mA source-sink capability

O_{24} - Output pin with 24 mA source-sink capability

OD_8 - Open-drain output pin with 8 mA sink capability

OD_{16} - Open-drain output pin with 16 mA sink capability

OD_{20} - Open-drain output pin with 20 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

O_{24p3} - 3.3V output pin with 24 mA source-sink capability

IN_t - TTL level input pin

IN_{ts} - TTL level Schmitt-trigger input pin

IN_{cs} - CMOS level Schmitt-trigger input pin

IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin

1.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	17	IN_t	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	98	OD_{16}	Generated PME event.
PCICLK	19	IN_{tsp3}	PCI clock input.
LDRQ#	20	O_{24p3}	Encoded DMA Request signal.
SERIRQ	21	I/O_{24tp3}	Serial IRQ input/Output.
LAD[3:0]	23-26	I/O_{24tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	27	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.

LRESET#	28	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.

1.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	1	OD_{24}	Drive Density Select bit 0.
INDEX#	2	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	3	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DSB#	4	OD_{24}	Drive Select B. When set to 0, this pin enables disk drive B. This is an open drain output.
DSA#	6	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
MOB#	7	OD_{24}	Motor B On. When set to 0, this pin enables disk drive 1. This is an open drain output.
DIR#	8	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	9	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	10	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	11	OD_{24}	Write enable. An open drain output.
TRAK0#	12	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	13	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	14	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

1.2 FDC Interface, continued

SYMBOL	PIN	I/O	FUNCTION
HEAD#	15	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1
DSKCHG#	16	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).

1.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
SLCT	29	IN_t	PRINTER MODE: An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	30	IN_t	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
BUSY	31	IN_t	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.
ACK#	32	IN_t	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
ERR#	33	IN_t	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD#pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
SLIN#	34	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	43	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
AFD#	44	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
STB#	46	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD0	42	I/O_{12t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
PD1	41	I/O_{12t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	40	I/O_{12t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.

1.3 Multi-Mode Parallel Port, continued

SYMBOL	PIN	I/O	FUNCTION
PD3	39	I/O_{12t}	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
PD4	38	I/O_{12t}	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		IN_t	EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD5	37	I/O_{12t}	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6	36	I/OD_{12t}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{12}	EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD7	35	I/OD_{12t}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		OD_{12}	EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

1.4 Serial Port Interface

SYMBOL	PIN	I/O	FUNCTION
CTSA# CTSB#	47 55	IN_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA# DSRB#	48 56	IN_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# HEFRAS	49	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS, which provides the power-on value for CR26 bit 6 (HEFRAS). A 4.7 kΩ is recommended if intends to pull up. (select 4EH as configuration I/O port's address)
RTSB#	57	I/O_{8t}	UART B Request To Send. An active low signal informs the modem or data set that the controller is ready to send data.
DTRA# PNPCSV#	50	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
DTRB#	58	I/O_{8t}	UART B Data Terminal Ready. An active low signal informs the modem or data set that controller is ready to communicate.
SINA SINB	51 59	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA PENROM#	52	I/O_{8t}	UART A Serial Output. It is used to transmit serial data out to the communication link. During power on reset , this pin is pulled down internally and is defined as PENROM#, which provides the power on value for CR24 bit 1. A 4.7kΩ is recommended if intends to pull up .
SOUTB PEN48 DCDA# DCDB#	61 53 62	I/O_{8t} IN_t	UART B Serial Output. During power-on reset, this pin is pulled down internally and is defined as PEN48, which provides the power-on value for CR24 bit 6 (EN48). A 4.7 kΩ resistor is recommended if intends to pull up. Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA# RIB#	54 63	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.

1.5 Infrared Port

SYMBOL	PIN	I/O	FUNCTION
IRRX	64	IN_{ts}	Alternate Function Input: Infrared Receiver input. General purpose I/O port 3 bit 6.
IRTX	65	OUT_{12t}	Alternate Function Output: Infrared Transmitter Output. General purpose I/O port 3 bit 7.

1.6 Fresh ROM Interface

SYMBOL	PIN	I/O	FUNCTION
XA18-XA16 GP57-GP55	66-68	O I/OD_{12t}	Flash ROM interface Address[18:16] General purpose I/O port 5 bit7-5
XA15-XA10 GP47-GP42	69-74	O I/OD_{12t}	Flash ROM interface Address[15:10] General purpose I/O port 4 bit7-2
XA9-XA8 GP41-GP40	76-77	O I/OD_{12t}	Flash ROM interface Address[9:8] General purpose I/O port 4 bit1-0
XA7-XA0 GP37-GP30	78-85	O I/OD_{12t}	Flash ROM interface Address[7:0] General purpose I/O port 3 bit7-0
XD7-XD4 GP27-GP24	86-89	O I/OD_{12t}	Flash ROM interface Data Bus[7:4] General purpose I/O port 2 bit7-4
XD3-XD0 GP23-GP20	91-94	O I/OD_{12t}	Flash ROM interface Data Bus [3:0] General purpose I/O port 2 bit3-0
ROMCS# GP54	95	O I/OD_{12t}	Flash ROM interface Chip Select General purpose I/O port 5 bit4
MEMR# GP53	96	O I/OD_{12t}	Flash ROM interface Memory Read Enable General purpose I/O port 5 bit3
MEMW# GP52	97	O I/OD_{12t}	Flash ROM interface Memory Write Enable General purpose I/O port 5 bit2

1.7 General Purpose I/O Port

SYMBOL	PIN	I/O	FUNCTION
GP73	111	I/OD_{12t}	General purpose I/O port 7 bit3
GP80 WDTO	118	I/OD_{12t} OD_{12}	General purpose I/O port 8 bit0 Watch dog timer output.
GP67	99	I/OD_{12t}	General purpose I/O port 6 bit7.
GP66	100	I/OD_{12t}	General purpose I/O port 6 bit6.
GP65	101	I/OD_{12t}	General purpose I/O port 6 bit5.
GP64	102	I/OD_{12t}	General purpose I/O port 6 bit4.
GP63	103	I/OD_{12t}	General purpose I/O port 6 bit3.
GP62	104	I/OD_{12t}	General purpose I/O port 6 bit2.
GP61	105	I/OD_{12t}	General purpose I/O port 6 bit1.
GP60	106	I/OD_{12t}	General purpose I/O port 6 bit0.

1.8 Smart Card Interface

SYMBOL	PIN	I/O	FUNCTION
SCPSNT GP77	107	IN_{ts} I/OD_{12t}	Smart card present detection Schmitt-trigger input. General purpose I/O port 7 bit7.
SCIO GP76	108	I/O_{12t} I/OD_{12t}	Smart card data I/O channel. General purpose I/O port 7 bit6.
SCCLK GP75	109	OUT_{12} I/OD_{12t}	Smart card clock output. General purpose I/O port 7 bit5.
SCRST GP74	110	OUT_{12} I/OD_{12t}	Smart card reset output. General purpose I/O port 7 bit4.
SCC8 GP72	112	I/O_{12t} I/OD_{12t}	Smart card General Purpose I/O channel. General purpose I/O port 7 bit2.
SCPWR GP71	113	OUT_{12} I/OD_{12t}	Smart card power control. General purpose I/O port 7 bit1.
SCC4 GP70	114	I/O_{12t} I/OD_{12t}	Smart card General Purpose I/O channel. General purpose I/O port 7 bit0.

1.9 PWM & General Purpose I/O Port 8

SYMBOL	PIN	I/O	FUNCTION
PWM2	115	OUT16t	Fan speed control . Use the Pulse Width Modulation (**PWM**)
PLED		OD_{12}	Power LED output, this signal is low after system reset.
GP83		I/OD_{12t}	General purpose I/O port 8 bit2-1
PWM1-0	116-117	OUT_{16t}	Fan speed control . Use the Pulse Width Modulation (**PWM**) Technic knowledge to control the Fan' s RPM.
GP82-81		I/OD_{12t}	General purpose I/O port 8 bit2-1

1.10 Game Port & MIDI Port

SYMBOL	PIN	I/O	FUNCTION
MSI	119	INt	MIDI serial data input .
GP51		I/OD_{12}	General purpose I/O port 5 bit 1.
MSO	120	OUT12t	MIDI serial data output.
GP50		I/OD_{12}	General purpose I/O port 5 bit 0.
GPAS2	121	INcs	Active-low, Joystick I switch input 2. This pin has an internal pull-up resistor. (Default)
GP17		I/OD_{12}	General purpose I/O port 1 bit 7.
GPBS2	122	INcs	Active-low, Joystick II switch input 2. This pin has an internal pull-up resistor. (Default)
GP16		I/OD_{12}	General purpose I/O port 1 bit 6.
GPAY	123	I/OD_{12}	Joystick I timer pin. this pin connect to Y positioning variable resistors for the Josystick. (Default)
GP15		I/OD12	General purpose I/O port 1 bit 5.
GPBY	124	I/OD_{12}	Joystick II timer pin. this pin connect to Y positioning variable resistors for the Josystick. (Default)
GP14		I/OD_{12}	General purpose I/O port 1 bit 4.

1.10 Game Port & MIDI Port, continued

SYMBOL	PIN	I/O	FUNCTION
GPBX	125	I/OD_{12}	Joystick II timer pin. this pin connect to X positioning variable resistors for the Josystick. (Default)
GP13		I/OD_{12}	General purpose I/O port 1 bit 3.
GPAX	126	I/OD12	Joystick I timer pin. this pin connect to X positioning variable resistors for the Josystick. (Default)
GP12		I/OD_{12}	General purpose I/O port 1 bit 2.
GPBS1	127	INcs	Active-low, Joystick II switch input 1. This pin has an internal pull-up resistor. (Default)
GP11		I/OD_{12}	General purpose I/O port 1 bit 1.
GPAS1	128	INcs	Active-low, Joystick I switch input 1. This pin has an internal pull-up resistor. (Default)
GP10		I/OD_{12}	General purpose I/O port 1 bit 0.

1.11 POWER PINS

SYMBOL	PIN	FUNCTION
VCC	5, 45, 75,	+5V power supply for the digital circuitry.
VCC3V	22	+3.3V power supply for driving 3V on host interface.
GND	18, 60, 90,	Ground.

2.0 LPC (LOW PIN COUNT) INTERFACE

LPC interface is to replace ISA interface serving as a bus interface between host (chip-set) and peripheral (Winbond I/O). Data transfer on the LPC bus are serialized over a 4 bit bus. The general characteristics of the interface implemented in Winbond LPC I/O are:

- One control line, namely LFRAME#, which is used by the host to start or stop transfers. No peripherals drive this signal.
- The LAD[3:0] bus, which communicates information serially. The information conveyed are cycle type, cycle direction, chip selection, address, data, and wait states.
- MR (master reset) of Winbond ISA I/O is replaced with a active low reset signal, namely LRESET#, in Winbond LPC I/O.
- An additional 33 MHz PCI clock is needed in Winbond LPC I/O for synchronization.
- DMA requests are issued through LDRQ#.
- Interrupt requests are issued through SERIRQ.
- Power management events are issued through PME#.

Comparing to its ISA counterpart, LPC implementation saves up to 40 pin counts free for integrating more devices on a single chip.

The transition from ISA to LPC is transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

3.0 FDC FUNCTIONAL DESCRIPTION

3.1 W83697SF FDC

The floppy disk controller of the W83697SF integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

3.1.1 AT interface

The interface consists of the standard asynchronous signals: RD#, WR#, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

3.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # × (1/DATA/RATE) *8 - 1.5 µS = DELAY

FIFO THRESHOLD	MAXIMUM DELAY TO SERVICING AT 500K BPS
	Data Rate
1 Byte	1 × 16 µS - 1.5 µS = 14.5 µS
2 Byte	2 × 16 µS - 1.5 µS = 30.5 µS
8 Byte	8 × 16 µS - 1.5 µS = 6.5 µS
15 Byte	15 × 16 µS - 1.5 µS = 238.5 µS
FIFO THRESHOLD	**MAXIMUM DELAY TO SERVICING AT 1M BPS**
	Data Rate
1 Byte	1 × 8 µS - 1.5 µS = 6.5 µS
2 Byte	2 × 8 µS - 1.5 µS = 14.5 µS
8 Byte	8 × 8 µS - 1.5 µS = 62.5 µS
15 Byte	15 × 8 µS - 1.5 µS = 118.5 µS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and underrun will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK# and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on DACK#. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.

3.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

3.1.4 Write Precompensation

The write precompensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require precompensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

3.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manSFacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

3.1.6 FDC Core

The W83697SF FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

3.1.7 FDC Commands

Command Symbol Descriptions:

C:	Cylinder number 0 - 256
D:	Data Pattern
DIR:	Step Direction
	DIR = 0, step out
	DIR = 1, step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EOT:	End of Track
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek

EOT:	End of track
FIFOTHR:	FIFO Threshold
GAP:	Gap length selection
GPL:	Gap Length
H:	Head number
HDS:	Head number select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM:	MFM or FM Mode
MT:	Multitrack
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number
ND:	Non-DMA Mode
OW:	Overwritten
PCN:	Present Cylinder Number
POLL:	Polling Disable
PRETRK:	Precompensation Start Track Number
R:	Record
RCN:	Relative Cylinder Number
R/W:	Read/Write
SC:	Sector/per cylinder
SK:	Skip deleted data address mark
SRT:	Step Rate Time
ST0:	Status Register 0
ST1:	Status Register 1
ST2:	Status Register 2
ST3:	Status Register 3
WG:	Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes/Sector
	W	---------- SC ----------								Sectors/Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector Repeat:	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | --------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL | ------ FIFOTHR ----|					
	W	| ----------PRETRK ---------- |								
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	| ---------- RCN ---------- |								

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ----------| --------- HUT --------								
	R	---------- HLT ----------| ND								
	R	---------- SC/EOT ----------								
	R	LOCK 0 D3 D2 D1 D0 GAP WG								
	R	0 EIS EFIFO POLL | ------ FIFOTHR --------								
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation-FDC goes to standby state)

Result	R	---------- ST0 ----------	ST0 = 80H

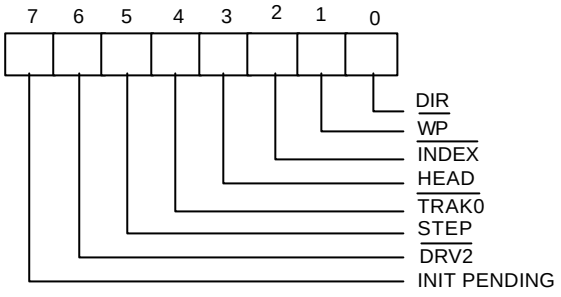
3.2 Register Descriptions

There are several status, data, and control registers in W83697SF. These registers are defined below:

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

3.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRV2# (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of STEP# output.

TRAK0# (Bit 4):

This bit indicates the value of TRAK0# input.

HEAD (Bit 3):

This bit indicates the complement of HEAD# output.

0 side 0

1 side 1

INDEX# (Bit 2):

This bit indicates the value of INDEX# output.

WP# (Bit 1):

0 disk is write-protected

1 disk is not write-protected

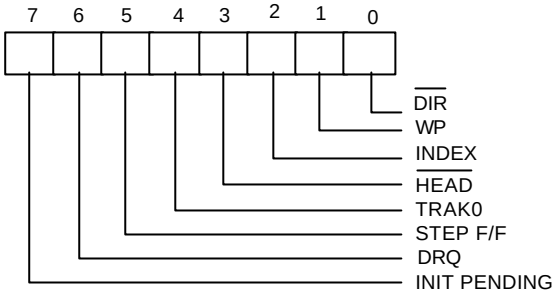
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched STEP# output.

TRAK0 (Bit 4):

This bit indicates the complement of TRAK0# input.

HEAD# (Bit 3):

This bit indicates the value of HEAD# output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of INDEX# output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

DIR# (Bit 0)

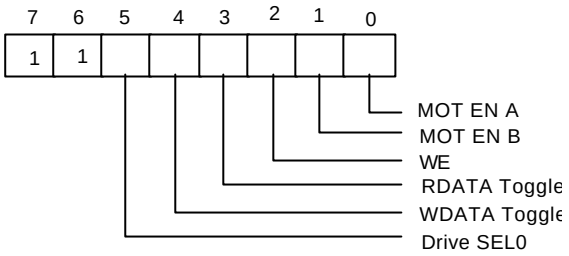
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

3.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the WD# output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the RDATA# output pin.

WE (Bit 2):

This bit indicates the complement of the WE# output pin.

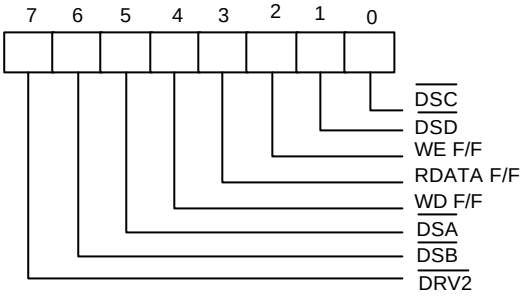
MOT EN B (Bit 1)

This bit indicates the complement of the MOB# output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



DRV2# (Bit 7):

0 A second drive has been installed

1 A second drive has not been installed

DSB# (Bit 6):

This bit indicates the status of DSB# output pin.

DSA# (Bit 5):

This bit indicates the status of DSA# output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched WD# output pin at every rising edge of the WD# output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched RDATA# output pin .

WE F/F (Bit 2):

This bit indicates the complement of latched WE# output pin.

DSD# (Bit 1):

0 Drive D has been selected

1 Drive D has not been selected

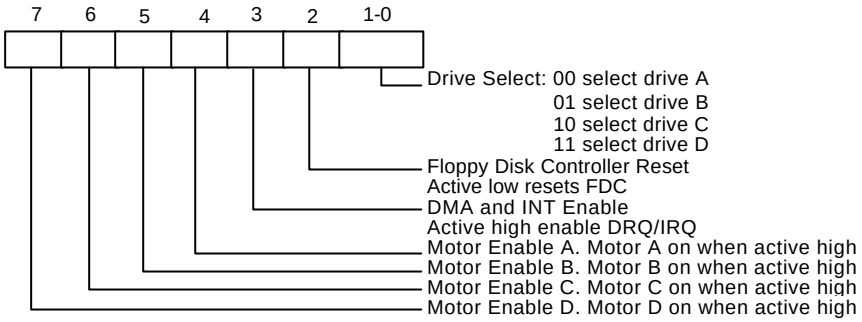
DSC# (Bit 0):

0 Drive C has been selected

1 Drive C has not been selected

3.2.3 Digital Output Register (DO Register) (Write base address + 2)

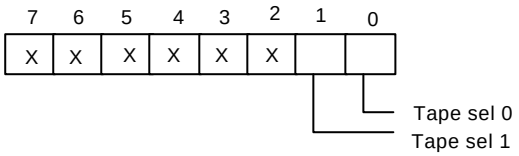
The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits in this register are cleared by the MR pin. The bit definitions are as follows:



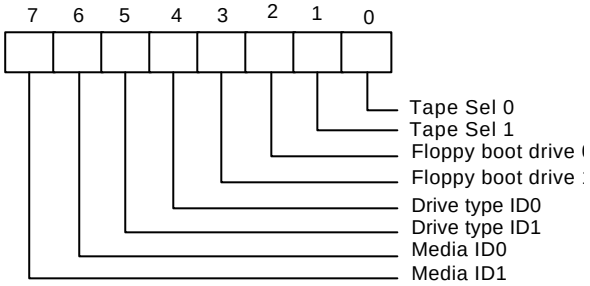
3.2.4. Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy

disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:



If three mode FDD function is enabled (EN3MODE = 1 in CR9), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of CR8 bit 3, 2.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of CR7. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of CR8 bit 1, 0.

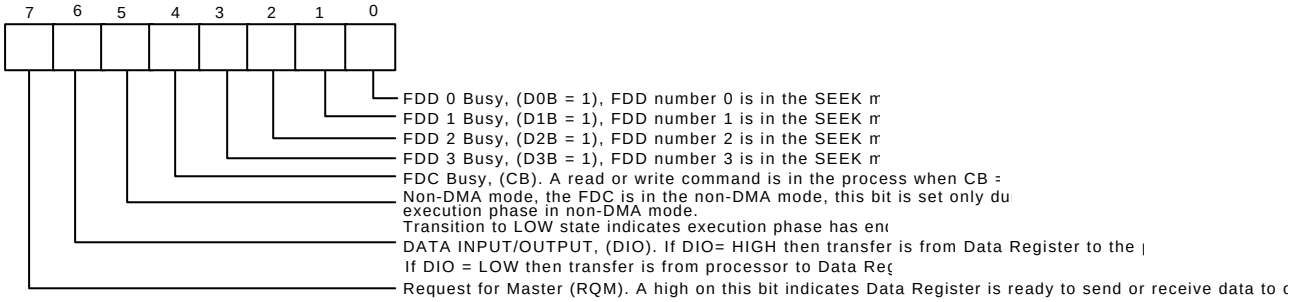
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

TAPE SEL 1	TAPE SEL 0	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

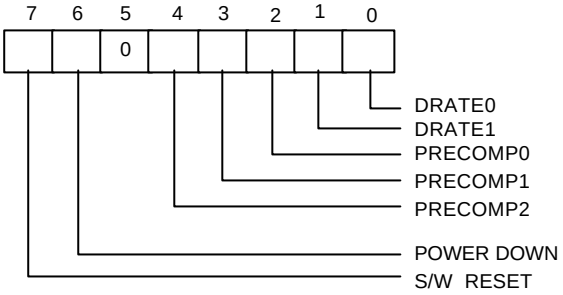
3.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



3.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write precompensation. The data rate of the FDC is programmed by the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode

1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the precompensation values for the combination of these bits.

PRECOMP	PRECOMPENSATION DELAY	
2 1 0	250K - 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 nS	20.8 nS
0 1 0	83.34 nS	41.17 nS
0 1 1	125.00 nS	62.5nS
1 0 0	166.67 nS	83.3 nS
1 0 1	208.33 nS	104.2 nS
1 1 0	250.00 nS	125.00 nS
1 1 1	0.00 nS (disabled)	0.00 nS (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 nS
300 KB/S	125 nS
500 KB/S	125 nS
1 MB/S	41.67nS
2 MB/S	20.8 nS

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC and reduced write current control.

00 500 KB/S (MFM), 250 KB/S (FM), $\overline{RWC}$ = 1

01 300 KB/S (MFM), 150 KB/S (FM), $\overline{RWC}$ = 0

10 250 KB/S (MFM), 125 KB/S (FM), $\overline{RWC}$ = 0

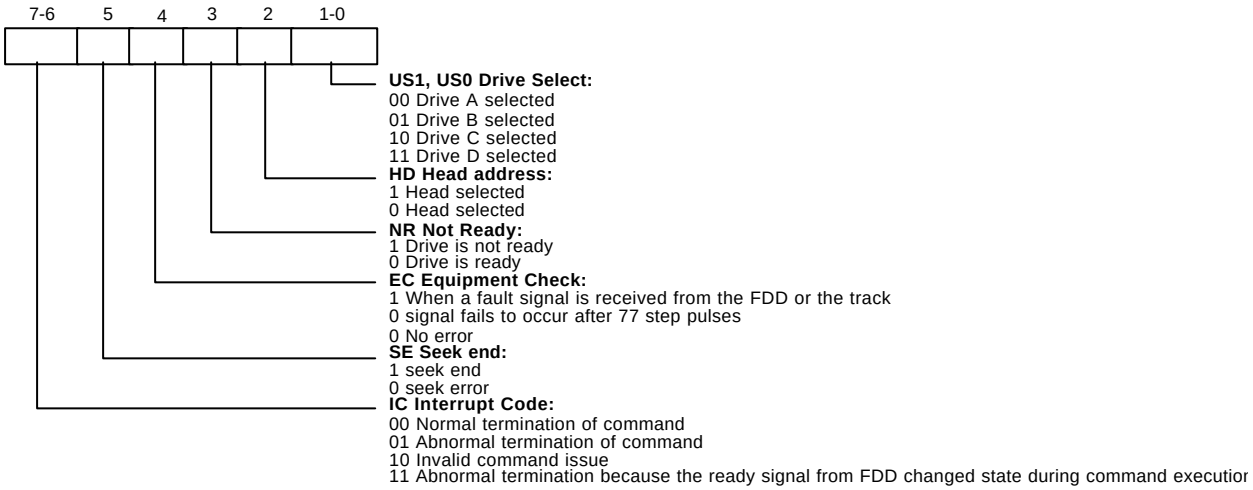
11 1 MB/S (MFM), Illegal (FM), $\overline{RWC}$ = 1

The 2 MB/S data rate for Tape drive is only supported by setting 01 to DRATE1 and DRATE0 bits, as well as setting 10 to DRT1 and DRT0 bits which are two of the Configure Register CRF4 or CRF5 bits in logic device 0. Please refer to the function description of CRF4 or CRF5 and data rate table for individual data rates setting.

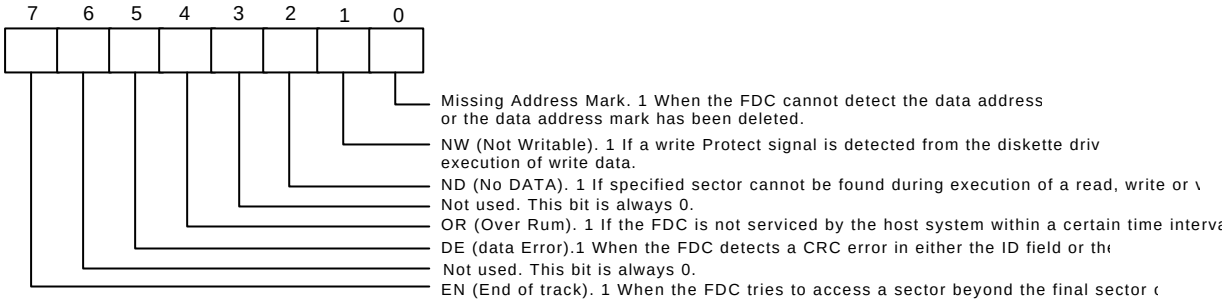
3.2.7 FIFO Register (R/W base address + 5)

The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83697SF, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

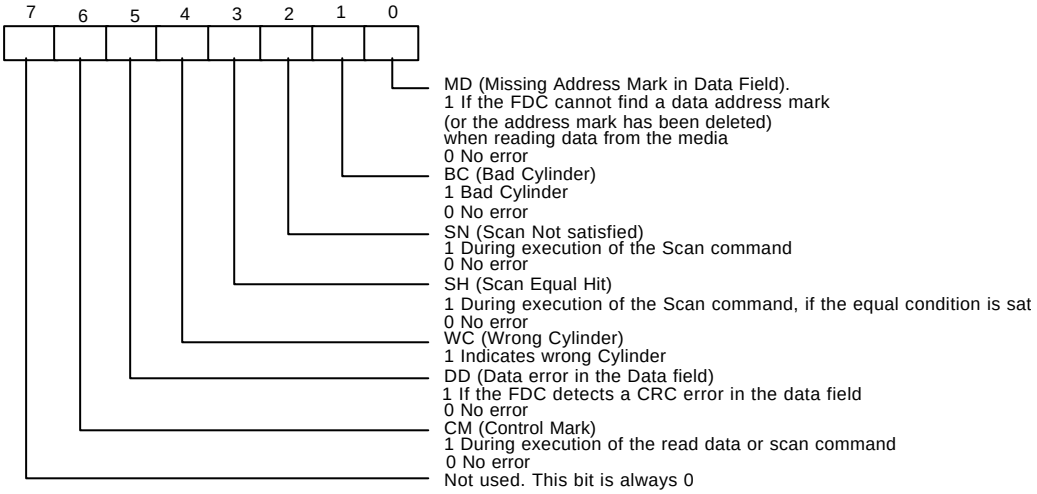
Status Register 0 (ST0)



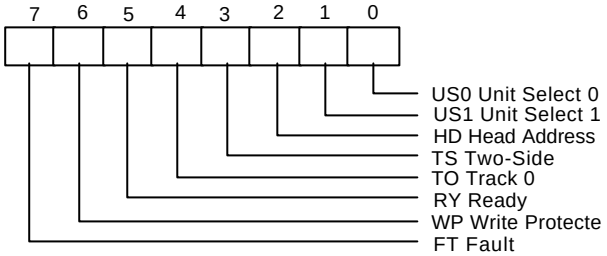
Status Register 1 (ST1)



Status Register 2 (ST2)

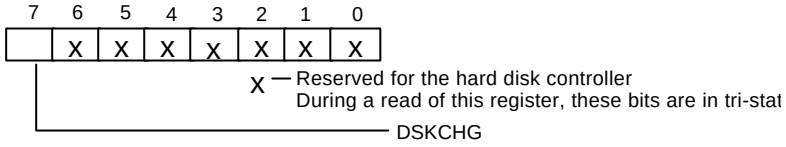


Status Register 3 (ST3)

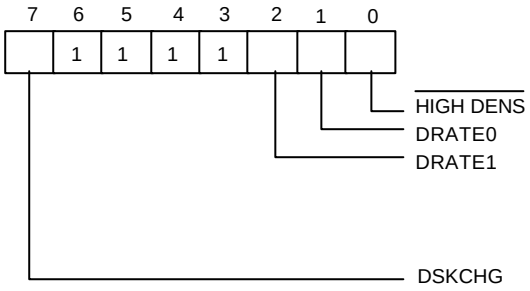


3.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of DSKCHG#, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



In the PS/2 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the complement of the DSKCHG# input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):

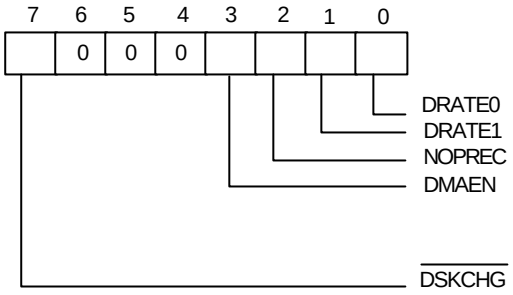
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

HIGH DENS# (Bit 0):

0 500 KB/S or 1 MB/S data rate (high density FDD)

1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the status of DSKCHG# input.

Bit 6-4: These bits are always a logic 1 during a read.

DMAEN (Bit 3):

This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):

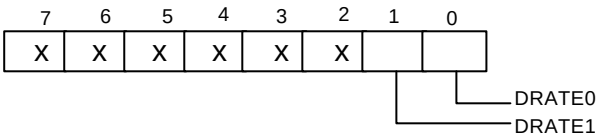
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

3.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



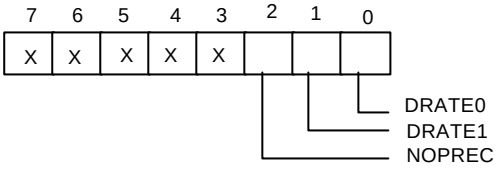
X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

In the PS/2 Model 30 mode, the bit definitions are as follows:



X: Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):

This bit indicates no precompensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

4.0 UART PORT

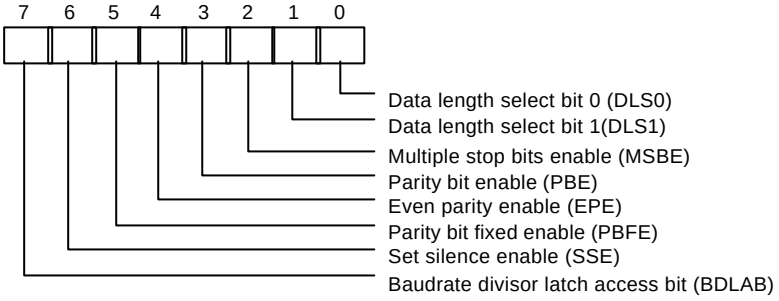
4.1 Universal Asynchronous Receiver/Transmitter (UART A, UART B)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

4.2 Register Address

4.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.



Bit 7 BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baudrate generator during a read or write operation. When this bit is reset, the Receiver BSFfer Register, the Transmitter BSFfer Register, or the Interrupt Control Register can be accessed.

Bit 6 SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected by this bit; the transmitter is not affected.

Bit 5 PBFE. When PBE and PBFE of UCR are both set to a logical 1,

(1) if EPE is logical 1, the parity bit is fixed as logical 0 to transmit and check.

(2) if EPE is logical 0, the parity bit is fixed as logical 1 to transmit and check.

TABLE 4-1 UART Register Bit Map

Register Address Base			Bit Number 0	1	2	3	4	5	6	7
+ 0 BDLAB = 0	Receiver BSFfer Register (Read Only)	RBR	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	Transmitter BSFfer Register (Write Only)	TBR	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	Interrupt Control Register	ICR	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	Interrupt Status Register (Read Only)	ISR	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	UART FIFO Control Register (Write Only)	SFR	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	UART Control Register	UCR	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	Handshake Control Register	HCR	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	UART Status Register	USR	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	Handshake Status Register	HSR	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	User Defined Register	UDR	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	Baudrate Divisor Latch Low	BLL	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	Baudrate Divisor Latch High	BHL	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

**: These bits are always 0 in 16450 Mode.

Bit 4 EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.

Bit 3 PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stSFfed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.

Bit 2 MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to a logical 0, one stop bit is sent and checked.

(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.

(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.

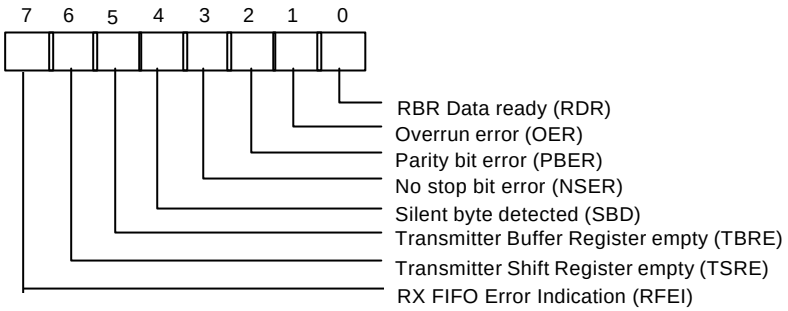
Bits 0 and 1 DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 4-2 WORD LENGTH DEFINITION

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

4.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.



Bit 7 RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6 TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other thanthese two cases, this bit will be reset to a logical 0

Bit 5 TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.

Bit 4 SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 3 NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

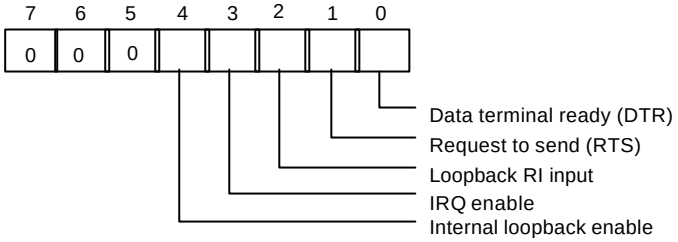
Bit 2 PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 1 OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they were read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0 RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

4.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



Bit 4 When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

(1) SOUT is forced to logical 1, and SIN is isolated from the communication link instead of the TSR.

(2) Modem output pins are set to their inactive state.

(3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) $\rightarrow \overline{DSR}$, RTS (bit 1 of HCR) $\rightarrow \overline{CTS}$, Loopback RI input (bit 2 of HCR) $\rightarrow \overline{RI}$ and IRQ enable (bit 3 of HCR) $\rightarrow \overline{DCD}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3 The UART interrupt output is enabled by setting this bit to a logic 1. In the diagnostic mode this bit is internally connected to the modem control input $\overline{DCD}$.

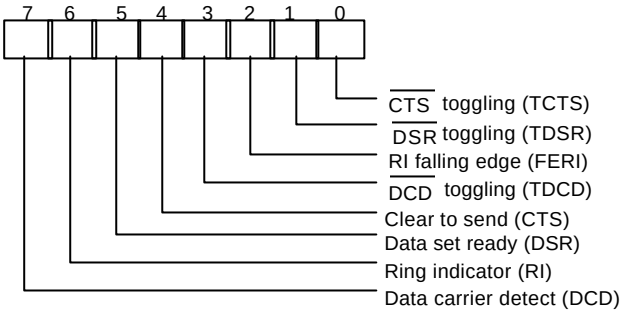
Bit 2 This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input $\overline{RI}$.

Bit 1 This bit controls the $\overline{RTS}$ output. The value of this bit is inverted and output to $\overline{RTS}$.

Bit 0 This bit controls the $\overline{DTR}$ output. The value of this bit is inverted and output to $\overline{DTR}$.

4.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.



Bit 7 This bit is the opposite of the $\overline{DCD}$ input. This bit is equivalent to bit 3 of HCR in loopback mode.

Bit 6 This bit is the opposite of the $\overline{RI}$ input. This bit is equivalent to bit 2 of HCR in loopback mode.

Bit 5 This bit is the opposite of the $\overline{DSR}$ input. This bit is equivalent to bit 0 of HCR in loopback mode.

Bit 4 This bit is the opposite of the $\overline{CTS}$ input. This bit is equivalent to bit 1 of HCR in loopback mode.

Bit 3 TDCD. This bit indicates that the $\overline{DCD}$ pin has changed state after HSR was read by the CPU.

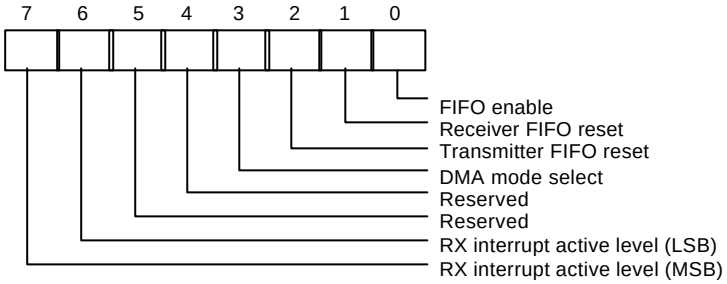
Bit 2 FERI. This bit indicates that the $\overline{RI}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1 TDSR. This bit indicates that the $\overline{DSR}$ pin has changed state after HSR was read by the CPU.

Bit 0 TCTS. This bit indicates that the $\overline{CTS}$ pin has changed state after HSR was read.

4.2.5 UART FIFO Control Register (SFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7 These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 4-3 FIFO TRIGGER LEVEL

BIT 7	BIT 6	RX FIFO INTERRUPT ACTIVE LEVEL (BYTES)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5 Reserved

Bit 3 When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if SFR bit 0 = 1.

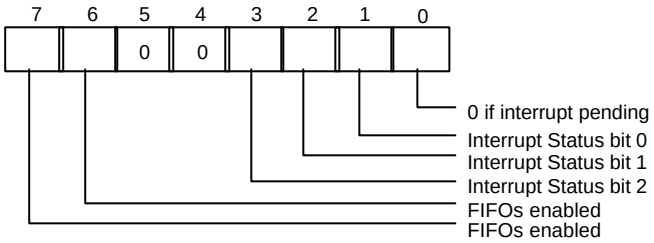
Bit 2 Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1 Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0 This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of SFR are programmed.

4.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Bit 7, 6 These two bits are set to a logical 1 when SFR bit 0 = 1.

Bit 5, 4 These two bits are always logic 0.

Bit 3 In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1 These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0 This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

TABLE 4-4 INTERRUPT CONTROL FUNCTION

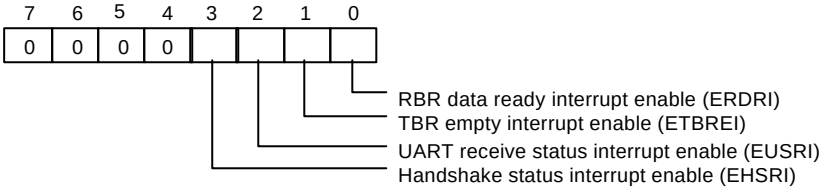
ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR

0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of SFR is logical 1.

4.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled by setting the appropriate bits of this register to a logical 1.



Bit 7-4: These four bits are always logic 0.

Bit 3 EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2 EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1 ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

4.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to 2^{16}-1. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table in the next page illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

4.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 4-5 BAUD RATE TABLE

BAUD RATE FROM DIFFERENT PRE-DIVIDER				
Pre-Div: 13 1.8461M Hz	Pre-Div:1.625 14.769M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage between desired and actual
50	400	650	**2304**	**
75	600	975	**1536**	**
110	880	1430	**1047**	0.18%
134.5	1076	1478.5	**857**	0.099%
150	1200	1950	**768**	**
300	2400	3900	**384**	**
600	4800	7800	**192**	**
1200	9600	15600	**96**	**
1800	14400	23400	**64**	**
2000	16000	26000	**58**	0.53%
2400	19200	31200	**48**	**
3600	28800	46800	**32**	**
4800	38400	62400	**24**	**
7200	57600	93600	**16**	**
9600	76800	124800	**12**	**
19200	153600	249600	**6**	**
38400	307200	499200	**3**	**
57600	460800	748800	**2**	**
115200	921600	1497600	**1**	**

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

Note. Pre-Divisor is determined by CRF0 of UART A and B.

5.0 PARALLEL PORT

5.1 Printer Interface Logic

The parallel port of the W83627SF makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The W83627SF supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), Extension 2FDD mode (EXT2FDD) on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation.

Table 6-1 shows the pin definitions for different modes of the parallel port.

TABLE 6-1-1 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	PIN NUMBER OF W83627SF	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	nSTB	nWrite	nSTB, HostClk[2]
2-9	31-26, 24-23	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	22	I	nACK	Intr	nACK, PeriphClk[2]
11	21	I	BUSY	nWait	BUSY, PeriphAck[2]
12	19	I	PE	PE	PEerror, nAckReverse[2]
13	18	I	SLCT	Select	SLCT, Xflag[2]
14	35	O	nAFD	nDStrb	nAFD, HostAck[2]
15	34	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	33	O	nINIT	nInit	nINIT[1], nReverseRqst[2]
17	32	O	nSLIN	nAStrb	nSLIN[1] , ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode
2. High Speed Mode
3. For more information, refer to the IEEE 1284 standard.

TABLE 6-1-2 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	PIN NUMBER OF W83627SF	PIN ATTRIBUTE	SPP	PIN ATTRIBUTE	EXT2FDD	PIN ATTRIBUTE	EXTFDD
1	36	O	nSTB	---	---	---	---
2	31	I/O	PD0	I	INDEX2#	I	INDEX2#
3	30	I/O	PD1	I	TRAK02#	I	TRAK02#
4	29	I/O	PD2	I	WP2#	I	WP2#
5	28	I/O	PD3	I	RDATA2#	I	RDATA2#
6	27	I/O	PD4	I	DSKCHG2#	I	DSKCHG2#
7	26	I/O	PD5	---	---	---	---
8	24	I/O	PD6	OD	MOA2#	---	---
9	23	I/O	PD7	OD	DSA2#	---	---
10	22	I	nACK	OD	DSB2#	OD	DSB2#
11	21	I	BUSY	OD	MOB2#	OD	MOB2#
12	19	I	PE	OD	WD2#	OD	WD2#
13	18	I	SLCT	OD	WE2#	OD	WE2#
14	35	O	nAFD	OD	RWC2#	OD	RWC2#
15	34	I	nERR	OD	HEAD2#	OD	HEAD2#
16	33	O	nINIT	OD	DIR2#	OD	DIR2#
17	32	O	nSLIN	OD	STEP2#	OD	STEP2#

5.2 Enhanced Parallel Port (EPP)

TABLE 6-2 PRINTER MODE AND EPP REGISTER ADDRESS

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status bSFfer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

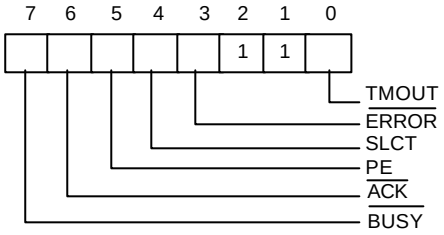
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

5.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

5.2.2 Printer Status BSFfer

The system microprocessor can read the printer status by reading the address of the printer status bSFfer. The bit definitions are as follows:



Bit 7 This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6 This bit represents the current state of the printer's ACK# signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before BUSY# stops.

Bit 5 Logical 1 means the printer has detected the end of paper.

Bit 4 Logical 1 means the printer is selected.

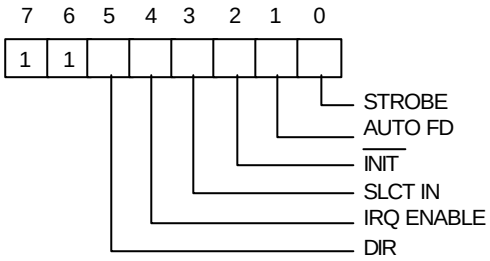
Bit 3 Logical 0 means the printer has encountered an error condition.

Bit 1, 2 These two bits are not implemented and are logic one during a read of the status register.

Bit 0 This bit is valid in EPP mode only. It indicates that a 10 µS time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

5.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



Bit 7, 6 These two bits are a logic one during a read. They can be written.

Bit 5 Direction control bit.

When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4 A 1 in this position allows an interrupt to occur when ACK# changes from low to high.

Bit 3 A 1 in this bit position selects the printer.

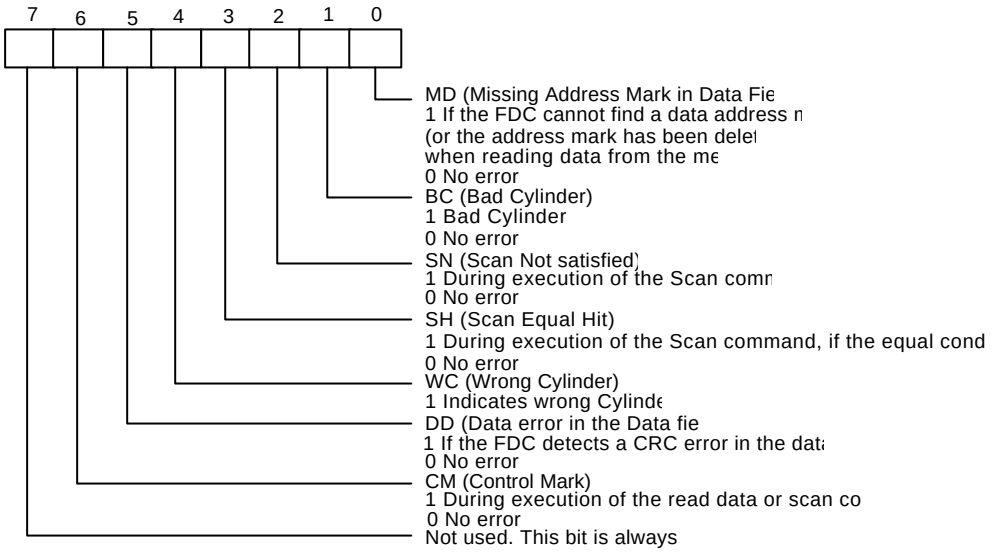
Bit 2 A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1 A 1 causes the printer to line-feed after a line is printed.

Bit 0 A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

5.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

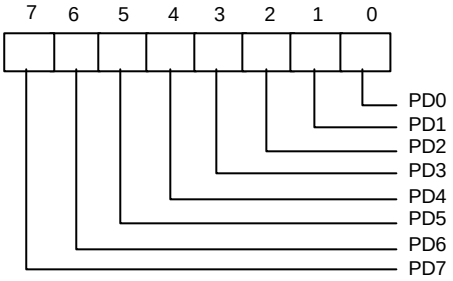


The contents of DB0-DB7 are bSFfered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

5.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are bSFfered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

5.2.6 Bit Map of Parallel Port and EPP Registers

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status BSFfer (Read)	BUSY#	ACK#	PE	SLCT	ERROF#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

EPP Data Port 3 (R/W)	PD7	PD6	PD 5	PD4	PD3	PD2	PD1	PD0

5.2.7 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
nWrite	O	Denotes an address or data read or write operation.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
nWait	I	Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer selected status; same as SPP mode.
nDStrb	O	This signal is active low. It denotes a data read or write operation.
nError	I	Error; same as SPP mode.
nInits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
nAStrb	O	This signal is active low. It denotes an address read or write operation.

5.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 µS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

5.2.8.1 EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

5.2.8.2 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

5.2.8.3 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

5.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

5.3.1 ECP Register and Mode Definitions

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR23, which are determined by configuration register or hardware setting.

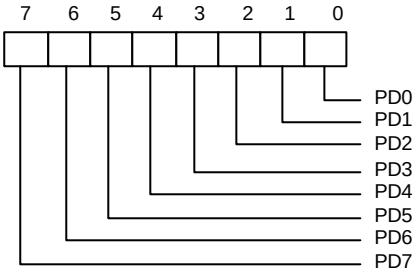
MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

5.3.2 Data and ecpAFifo Port

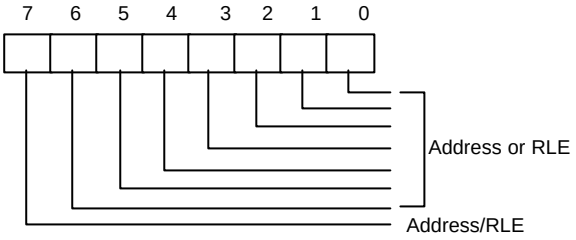
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



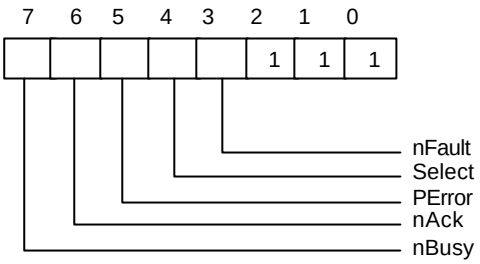
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:



5.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:



Bit 7 This bit reflects the complement of the Busy input.

Bit 6 This bit reflects the nAck input.

Bit 5 This bit reflects the PError input.

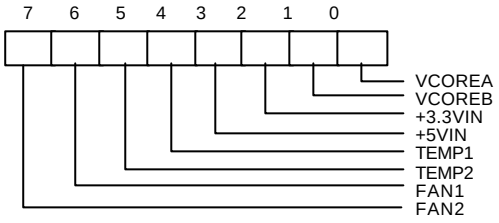
Bit 4 This bit reflects the Select input.

Bit 3 This bit reflects the nFault input.

Bit 2-0 These three bits are not implemented and are always logic one during a read.

5.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Bit 6, 7 These two bits are logic one during a read and cannot be written.

Bit 5 This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0 the parallel port is in output mode.

1 the parallel port is in input mode.

Bit 4 Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the ACK# input.

Bit 3 This bit is inverted and output to the SLIN# output.

0 The printer is not selected.

1 The printer is selected.

Bit 2 This bit is output to the INIT# output.

Bit 1 This bit is inverted and output to the AFD# output.

Bit 0 This bit is inverted and output to the STB# output.

5.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

5.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

5.3.7 tFifo (Test FIFO Mode) Mode = 110

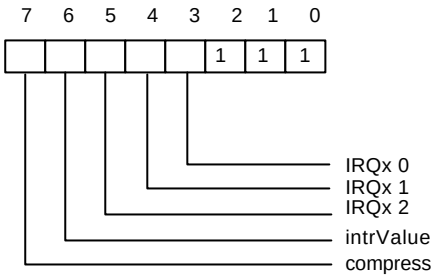
Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

5.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

5.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Bit 7 This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6 Returns the value on the ISA IRQ line to determine possible conflicts.

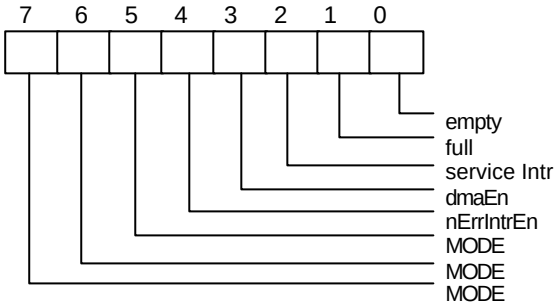
Bit 5-3 Reflect the IRQ resource assigned for ECP port.

cnfgB[5:3]	IRQ resource
000	reflect other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

Bit 2-0 These five bits are at high level during a read and can be written.

5.3.10 ecr (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: These bits are read/write and select the mode.

000 Standard Parallel Port mode. The FIFO is reset in this mode.

001 PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.

010 Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.

011 ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and auto transmitted to the peripheral using ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.

100 Selects EPP Mode. In this mode, EPP is activated if the EPP mode is selected.

101 Reserved.

110 Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.

111 Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

1 Disables the interrupt generated on the asserting edge of nFault.

0 Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

1 Enables DMA.

0 Disables DMA unconditionally.

Bit 2: Read/Write

1 Disables DMA and all of the service interrupts.

0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.

(a) dmaEn = 1: During DMA this bit is set to a 1 when terminal count is reached.

(b) dmaEn = 0 direction = 0: This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.

(c) dmaEn = 0 direction = 1: This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0 The FIFO has at least 1 free byte.

1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

0 The FIFO contains at least 1 byte of data.

1 The FIFO is completely empty.

5.3.11 Bit Map of ECP Port Registers

	D7	D6	D5	D4	D3	D2	D1	D0	NOTE
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
dcr	1	1	Directio	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	1	1	1	1	1	1	
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:

1. These registers are available in all modes.
2. All FIFOs use one common 16 -byte FIFO.

5.3.12 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe (HostClk)	O	The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contains address or data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low.
nFault (nPeriphRequest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

5.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

Mode Switching

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

Data Compression

The W83627SF supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

5.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

5.3.15 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, which will disable the DMA.

5.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. The host must set the direction, state, dmaEn = 0 and serviceIntr = 0 in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

5.4 Extension FDD Mode (EXTFDD)

In this mode, the W83627SF changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 6-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins MOB# and DSB# will be forced to inactive state.

(2) Pins DSKCHG#, RDATA#, WP#, TRAK0#, INDEX# will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

5.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83627SF changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table6-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins MOA#, DSA#, MOB#, and DSB# will be forced to inactive state.

(2) Pins DSKCHG#, RDATA#, WP#, TRAK0#, and INDEX# will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

6.0 GENERAL PURPOSE I/O

W83697SF provides 60 input/output ports that can be individually configured to perform a simple basic I/O function or a pre-defined alternate function. Those 60 GP I/O ports are divided into three groups, each group contains 8 ports. The first group is configured through control registers in logical device 7, the second group in logical device 8, and the third group in logical device 9. Users can configure each individual port to be an input or output port by programming respective bit in selection register (CRF0: 0 = output, 1 = input). Invert port value by setting inversion register (CRF2: 0 = non-inverse, 1 = inverse). Port value is read/written through data register (CRF1). Table 7.1 and 7.2 gives more details on GPIO's assignment. In addition, GPIO1 is designed to be functional even in power loss condition (VCC or VSB is off). Figure 7.1 shows the GP I/O port's structure. Right after Power-on reset, those ports default to perform basic input function except ports in GPIO1 which maintains its previous settings until a battery loss condition.

Table 7.1

SELECTION BIT 0 = OUTPUT 1 = INPUT	INVERSION BIT 0 = NON INVERSE 1 = INVERSE	BASIC I/O OPERATIONS
0	0	Basic non-inverting output
0	1	Basic inverting output
1	0	Basic non-inverting input
1	1	Basic inverting input

Table 7.2

GP I/O PORT DATA REGISTER	REGISTER BIT ASSIGNMENT	GP I/O PORT
GP1	BIT 0	GP10
	BIT 1	GP11
	BIT 2	GP12
	BIT 3	GP13
	BIT 4	GP14
	BIT 5	GP15
	BIT 6	GP16
	BIT 7	GP17
GP2	BIT 0	GP20
	BIT 1	GP21
	BIT 2	GP22
	BIT 3	GP23
	BIT 4	GP24
	BIT 5	GP25
	BIT 6	GP26
	BIT 7	GP27
GP3	BIT 0	GP30
	BIT 1	GP31
	BIT 2	GP32
	BIT 3	GP33
	BIT 4	GP34
	BIT 5	GP35
	BIT 6	GP36
	BIT 7	GP37

Table 7.2, continued

GP I/O PORT DATA REGISTER	REGISTER BIT ASSIGNMENT	GP I/O PORT
GP4	BIT 0	GP40
	BIT 1	GP41
	BIT 2	GP42
	BIT 3	GP43
	BIT 4	GP44
	BIT 5	GP45
	BIT 6	GP46
	BIT 7	GP47
GP5	BIT 0	GP50
	BIT 1	GP51
	BIT 2	GP52
	BIT 3	GP53
	BIT 4	GP54
	BIT 5	GP55
	BIT 6	GP56
	BIT 7	GP57
GP6	BIT 0	GP60
	BIT 1	GP61
	BIT 2	GP62
	BIT 3	GP63
	BIT 4	GP64
	BIT 5	GP65
	BIT 6	GP66
	BIT 7	GP67

Table 7.2, continued

GP I/O PORT DATA REGISTER	REGISTER BIT ASSIGNMENT	GP I/O PORT
GP7	BIT 0	GP70
	BIT 1	GP71
	BIT 2	GP72
	BIT 3	GP73
	BIT 4	GP74
	BIT 5	GP75
	BIT 6	GP76
	BIT 7	GP77
GP8	BIT 0	GP80
	BIT 1	GP81
	BIT 2	GP82
	BIT 3	GP83

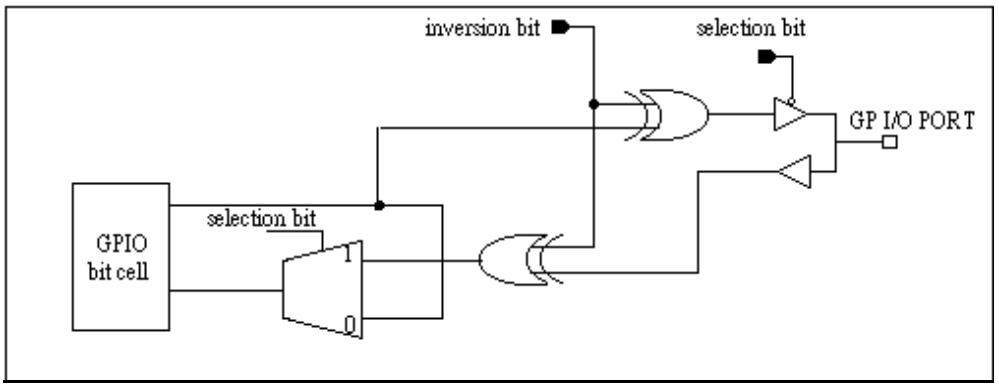
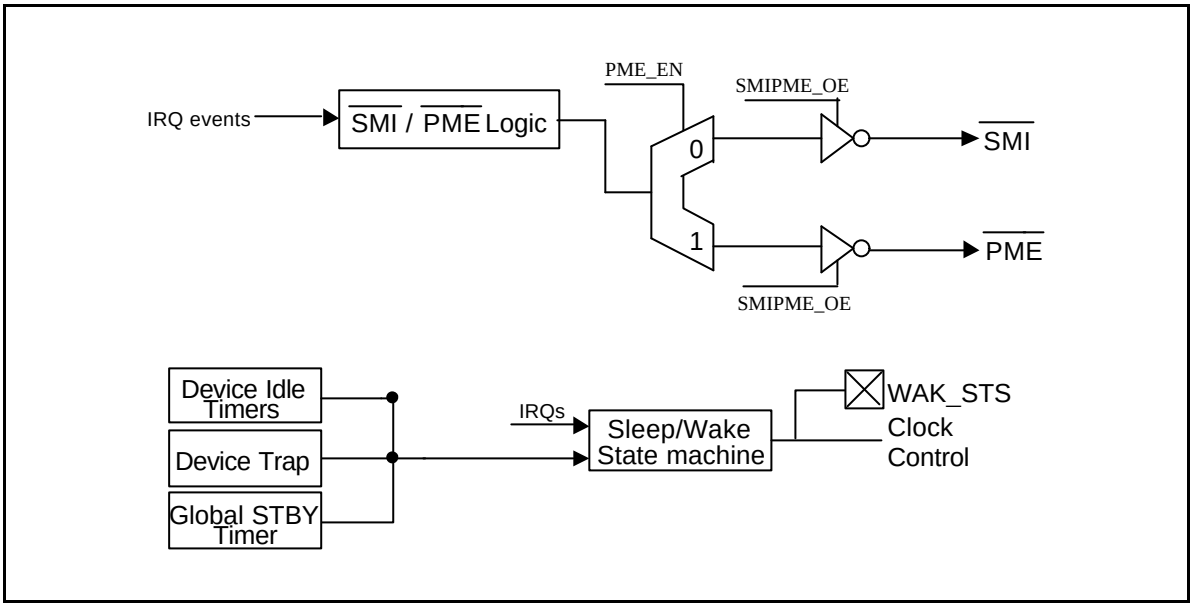


Figure 7.1

7.0 ACPI REGISTERS FEATURES

W83697SF supports both ACPI and legacy power managements. The switch logic of the power management block generates an $\overline{SMI}$ interrupt in the legacy mode and an $\overline{PME}$ interrupt in the ACPI mode. The new ACPI feature routes $\overline{SMI}$ / $\overline{PME}$ logic output either to $\overline{SMI}$ or to $\overline{PME}$ .The $\overline{SMI}$ / $\overline{PME}$ logic routes to $\overline{SMI}$ only when both PME_EN = 0 and SMIPME_OE = 1. Similarly, the $\overline{SMI}$ / $\overline{PME}$ logic routes to $\overline{PME}$ only when both PME_EN = 1 and SMIPME_OE = 1.



8.0 PULSE WIDTH MODULATION (PWM)

8.1 General Description

The W83697SF provides 3 sets for fan PWM speed control. The duty cycle of PWM can be programmed by the 8-bit registers which are defined in the CR01, CR03 and CR11. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. the expression of duty can be represented as follows.

$$\text{Duty}-\text{cycle}\,(\%)=\frac{\text{Programmed 8-bit Register Value}+1}{256}\times 100\,\%,$$

$$\text{Programmed 8-bit register value}\neq 0.$$

$$\text{If programmed 8-bit register value}=0,\ \text{the duty cycle}=0\,\%.$$

The PWM clock frequency also can be program and defined in the CR00, CR02 and CR10. The application circuit is shown as the Figure 9.1.

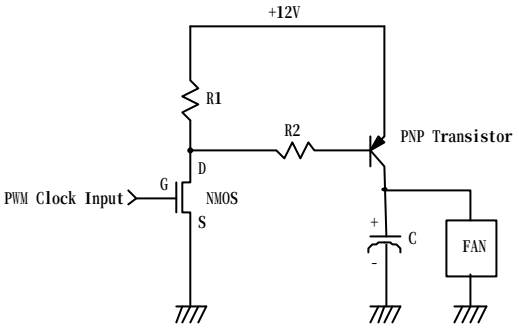


Figure 9.1 : The PWM application circuit

8.2 LPC Interface

The interface uses LPC Bus to access which the ports of low byte (bit2~bit0) are defined in the port 5h and 6h. The other higher bits of these ports is set by W83697SF itself. The general decoded address is set to port 295h and port 296h. These two ports are described as following:

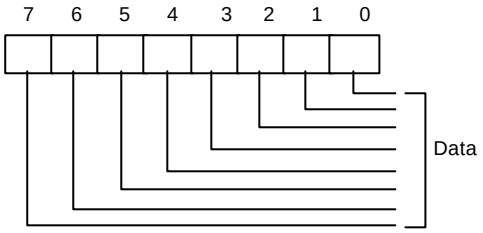
Port 295h: Index port.

Port 296h: Data port.

8.3 REGISTERS

8.3.1 Address Register (Port x5h)

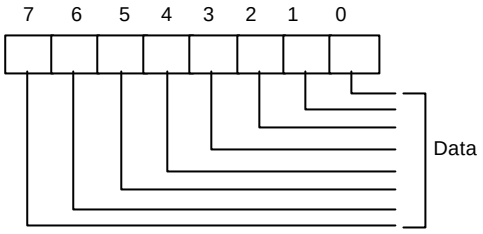
Data Port:	Port x5h
Power on Default Value	FFh
Attribute:	Bit 7:0 Read/write
Size:	8 bits



Bit 7-0: Read/Write address pointer.

8.3.2 Data Register (Port x6h)

Data Port:	Port x6h
Power on Default Value	00h
Attribute:	Read/write
Size:	8 bits



Bit 7-0: Data to be read from or to be written to Register.

8.3.3 PWM 1 Pre-Scale Register -- Index 00h

Power on default [7:0] = 0000-0001 b

Bit	Name	Read/Write	Description
7	PWM_CLK_SEL1	Read/Write	**PWM 1 Input Clock Select.** This bit select PWM 1 input clock to pre-scale divider. 0: 24 MHz 1: 187.5 KHz
6-0	PRE_SCALE1[6:0]	Read/Write	**PWM 1 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM 1 frequency = (Input Clock / Pre-scale) / 256

8.3.4 PWM 1 Duty Cycle Select Register – Index 01h

Power on default [7:0] 1111,1111 b

Bit	Name	Read/Write	Description
7-0	PWM1_DC[7:0]	Read/Write	**PWM 1 Duty Cycle.** This 8-bit register determines the number of the 256-cycle period. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX+1)/256*100% during one cycle.

8.3.5 PWM 2 Pre-Scale Register -- Index 02h

Power on default [7:0] = 0000,0001 b

Bit	Name	Read/Write	Description
7	PWM_CLK_SEL2	Read/Write	**PWM 2 Input Clock Select.** This bit select PWM 2 input clock to pre-scale divider. 0: 24 MHz 1: 187.5 KHz
6-0	PRE_SCALE2[6:0]	Read/Write	**PWM 2 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM 2 frequency = (Input Clock / Pre-scale) / 256

8.3.6 PWM 2 Duty Cycle Select Register -- Index 03h

Power on default [7:0] = 1111,1111 b

Bit	Name	Read/Write	Description
7-0	PWM2_DC[7:0]	Read/Write	**PWM 2 Duty Cycle.** This 8-bit register determines the number of the 256-cycle period. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX+1)/256*100% during one cycle.

8.3.7 PWM 0 Pre-Scale Register -- Index 10h

Power on default [7:0] = 0000-0001 b

Bit	Name	Read/Write	Description
7	PWM_CLK_SEL0	Read/Write	**PWM 0 Input Clock Select.** This bit select PWM 0 input clock to pre-scale divider. 0: 24 MHz 1: 187.5 KHz
6-0	PRE_SCALE0[6:0]	Read/Write	**PWM 0 Input Clock Pre-Scale.** The divider of input clock is the number defined by pre-scale. Thus, writing 0 transfers the input clock directly to counter. The maximum divider is 128 (7Fh). 00h : divider is 1 01h : divider is 2 02h : divider is 3 : :

PWM 0 frequency = (Input Clock / Pre-scale) / 256

8.3.8 PWM 0 Duty Cycle Select Register – Index 11h

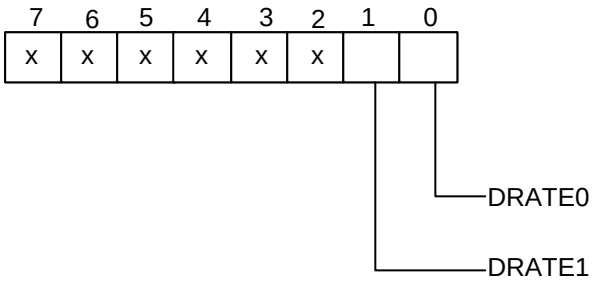
Power on default [7:0] 1111,1111 b

Bit	Name	Read/Write	Description
7-0	PWM0_DC[7:0]	Read/Write	**PWM 0 Duty Cycle.** This 8bit register determines the number of the 256-cycle period. 00h: PWM output is always logical Low. FFh: PWM output is always logical High. XXh: PWM output logical High percentage is (XX+1)/256*100% during one cycle.

9.0 CONFIGURATION REGISTER

9.1 Plug and Play Configuration

The W83697SF uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83697SF, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), UART2 (logical device 3), CIR (Consumer IR, logical device 6), GPIO1 (logical device 7), GPIO5(logical device 8),GPIO2 ~GPIO4(logical device 9), ACPI ((logical device A), and Hardware monitor (logical device B). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR7.



9.2 Compatible PnP

9.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	address and value
0	write 87h to the location 2Eh twice
1	write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 49) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

9.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83697SF enters the default operating mode. Before the W83697SF enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

9.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh (as described in section 12.2.1) on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh (as described in section 9.2.1) on PC/AT systems.

9.3 Configuration Sequence

To program W83697SF configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

9.3.1 Enter the extended function mode

To place the chip into the extended function mode, two successive wrtites of 0x87 must be applied to Extended Function Enable Registers(EFERs, i.e. 2Eh or 4Eh).

9.3.2 Configurate the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register(EFIR) and Extended Function Data Register(EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).
First, write the Logical Device Number (i.e.,0x07) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip(Global) Control Registers, this step is not required.
Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

9.3.3 Exit the extended function mode

To exit the extended function mode, one write of 0xAA to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

9.3.4 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;-------------------------------------------- ----------------------------------
; Enter the extended function mode ,interruptible double-write    |
;-------------------------------------------------------------------------------
MOV     DX,2EH
MOV AL,87H
OUT     DX,AL
OUT     DX,AL
;-------------------------------------------------------------------------------
; Configurate logical device 1, configuration register CRF0   |
;-------------------------------------------------------------------------------
MOV     DX,2EH
MOV     AL,07H
OUT     DX,AL           ; point to Logical Device Number Reg.
MOV     DX,2FH
MOV     AL,01H
OUT     DX,AL           ; select logical device 1
;
MOV     DX,2EH
MOV     AL,F0H
OUT     DX,AL           ; select CRF0
MOV     DX,2FH
MOV AL,3CH
OUT     DX,AL           ; update CRF0 with value 3CH
;----------------------------------------
; Exit extended function mode     |
;----------------------------------------
MOV     DX,2EH
MOV AL,AAH
OUT     DX,AL
```

9.4 Chip (Global) Control Register

CR02 (Default 0x00) (Write only)

Bit [7:1]: Reserved.

Bit 0 = 1 SWRST --> Soft Reset.

CR07

Bit [7:0]: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20 (read only)

Bit [7:0]: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0

= 0x 68 (for W83697SF & W83697SF)

= 0x 60 (for W83697F)

CR21 (read only)

Bit [7:0]: DEVREVB7 - DEBREVB0 --> Device Rev

= 0x1X (for W83697SF)

= 0x0X (for W83697SF)

= 0x1Y (for W83697F)

X : Version change number. (Bit [3:0]) --> begin from 1

Y : Version change number. (Bit [3:0]) --> begin from F

CR22 (Default 0xef)

Bit 7: SCPWD

0 Power down

1 No Power down

Bit 6: URDPWD

0 Power down

1 No Power down

Bit 5: URCPWD

0 Power down

1 No Power down

Bit 4: Reserved

Bit 3: URBPWD

0 Power down

1 No Power down

Bit 2: URAPWD

0 Power down

1 No Power down

Bit 1: PRTPWD

0 Power down

1 No Power down

Bit 0: FDCPWD

0 Power down

1 No Power down

CR23 (Default 0xfe)

Bit [7:1]: Reserved.

Bit 0: IPD (Immediate Power Down).

When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default 0s1000ss)

Bit 7: Flash ROM I/F Address Segment (000F0000h ~ 000FFFFFh) enable/disable

0 Enable

1 Disable

Bit 6: CLKSEL(Enable 48Mhz)

0 The clock input on Pin 1 should be 24 MHz.

1 The clock input on Pin 1 should be 48 MHz.

The corresponding power-on setting pin is SOUTB (pin 61).

Bit [5:4]: ROM size select

00 1M

01 2M

10 4M

11 Reserved

Bit 3: MEMW# Select (PIN97)

0 MEMW# Disable

1 MEMW# Enable

Bit 2: Flash ROM I/F Address Segment (000E0000h ~ 000EFFFFh) enable/disable

0 Enable

1 Disable

Bit 1 : Enable Flash ROM Interface

0 Flash ROM Interface is enabled after hardware reset

1 Flash ROM Interface is disabled after hardware reset

The corresponding power-on setting pin is PENROM#(pin 52)

Bit 0: PNPCSV

0 The Compatible PnP address select registers have default values.

1 The Compatible PnP address select registers have no default value.

The corresponding power-on setting pin is DTRA# (pin 50).

CR25 (Default 0x00)

Bit 7: SCTRI

Bit 6: URDTRI

Bit 5: URCTRI

Bit 4: Reserved

Bit 3: URBTRI

Bit 2: URATRI

Bit 1: PRTTRI

Bit 0: FDCTRI

CR26 (Default 0x00)

Bit 7: SEL4FDD

0 Select two FDD mode.

1 Select four FDD mode.

Bit 6: HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is RTSA #(pin 49).

HEFRAS Address and Value

0 Write 87h to the location 2E twice.

1 Write 87h to the location 4E twice.

Bit 5: LOCKREG

0 Enable R/W Configuration Registers.

1 Disable R/W Configuration Registers.

Bit 4: Reserved

Bit 3: DSFDLGRQ

0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ

0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ

0 Enable UART A/C legacy mode IRQ selecting, then HCR bit 3 is effective on selecting IRQ

1 Disable UART A/C legacy mode IRQ selecting, then HCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ

0 Enable UART B/D legacy mode IRQ selecting, then HCR bit 3 is effective on selecting IRQ

1 Disable UART B/D legacy mode IRQ selecting, then HCR bit 3 is not effective on selecting IRQ

CR28 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3]: Flash ROM I/F Address Segment (FFE80000h ~ FFEFFFFFh) enable/disable

0 Disable

1 Enable

Bit [2:0]: PRTMODS2 - PRTMODS0

0xx Parallel Port Mode

100 Reserved

101 External FDC Mode

110 Reserved

111 External two FDC Mode

CR29 (GPIO1,5(50~51) & Game port & MIDI port Select. Default 0x00)

Bit 7: Port Select (select Game Port or General Purpose I/O Port 1)

0 Game Port

1 General Purpose I/O Port 1 (pin121~128 select function GP10~GP17)

Bit [6:5]: (Pin119)

00 MSI

01 Reserved

10 Reserved

11 GP51

Bit [4:3]: (Pin 120)

00 MSO

01 Reserved

10 Reserved

11 GP50

Bit 2: (Pin117)

OVT# & SMI Select(Pin117)

0 OVT#

1 SMI#

Bit [1:0]: Reserved

CR2A(GPIO2 ~ 5& Fresh ROM Interface Select,
default 0xFF if PENROM# = 0 during POR,
default 0x00 otherwise)

Bit 7: (PIN 86 ~89 & 91 ~94)

0 GPIO 2

1 Fresh IF (xD7 ~ XD0)

Bit 6: (PIN 78 ~ 85)

0 GPIO 3

1 Fresh IF (XA7 ~ XA0)

Bit 5: (PIN 69 ~ 74 & 76 ~77)

0 GPIO 4

1 Fresh IF (XA15 ~ XA10 & XA9 ~ A8)

Bit 4: (PIN 66 ~ 68 & 95 ~ 97)

0 GPIO 5(GP52 ~ 57)

1 Fresh IF(XA18 ~ XA16 , ROMCS#, MEMR #, MEMW#)

Bit [3:0]: Reserved

CR2B(PWM & GPIO8, URC & GPIO6 Select.

Default 0x00 (for W83697SF & W83697F)

Default 0x03 (for W83697SF))

Bit [7]: Reserved.

Bit [6:5]: (Pin115)

00 PWM2

01 PLED

10 Reserved

11 GP83

Bit [4]: (Pin116)

0 PWM1

1 GP82

Bit [3]: (Pin117)

0 PWM0

1 GP81

Bit [2]: (Pin118)

0 WDTO

1 GP80

Bit [1]: (Pin99, Pin100, Pin101, Pin102, Pin105, Pin106)

0 URC(NCTSC, NDSRC, NRTSC, NDTRC, NDCDC, NRIC)

1 GPIO6(GP67, GP66, GP65, GP64, GP61, GP60)

Bit [0]: (Pin103, Pin104)

0 URC(SINC, SOUTC)

1 GPIO6(GP63, GP62)

CR2C(SC & URD & GPIO7 Select.

Default 0x30 (for W83697SF & W83697SF & W83697F)

Bit [7:6]: (Pin107, Pin108, Pin109, Pin110, Pin113)

- 00 SC(SCPSNT, SCIO,SCCLK, SCRST, SCPWR)
- 01 URD(NCTSD,NDSRD, NRTSD, NDTRD, NDCDD)
- 10 Reserved
- 11 GPIO7(GP77, GP76, GP75, GP74, GP71)

Bit [5:4]: (Pin111)

- 00 Reserved
- 01 SIND
- 10 Reserved
- 11 GP73

Bit [3:2]: (Pin112)

- 00 SCC8
- 01 SOUTD
- 10 Reserved
- 11 GP72

Bit [1:0]: (Pin114)

- 00 SCC4
- 01 NRID
- 10 Reserved
- 11 GP70

9.5 Logical Device 0 (FDC)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0:
- 1 Activates the logical device.
- 0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0xf0 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for FDC.

CR74 (Default 0x02 if PNPCSV = 0 during POR, default 0x04 otherwise)

Bit [7:3]: Reserved.

Bit [2:0]: These bits select DRQ resource for FDC.

= 0x00 DMA0

= 0x01 DMA1

= 0x02 DMA2

= 0x03 DMA3

= 0x04 - 0x07 No DMA active

CRF0 (Default 0x0E)

FDD Mode Register

Bit 7: FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

0 The internal pull-up resistors of FDC are turned on.(Default)

1 The internal pull-up resistors of FDC are turned off.

Bit 6: INTVERTZ

This bit determines the polarity of all FDD interface signals.

0 FDD interface signals are active low.

1 FDD interface signals are active high.

Bit 5: DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4: Swap Drive 0, 1 Mode

0 No Swap (Default)

1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 Interface Mode

11 AT Mode (Default)

10 (Reserved)

01 PS/2

00 Model 30

Bit 1: FDC DMA Mode
- 0 Burst Mode is enabled
- 1 Non-Burst Mode (Default)

Bit 0 Floppy Mode
- 0 Normal Floppy Mode (Default)
- 1 Enhanced 3-mode FDD

CRF1 (Default 0x00)

Bit 7 - 6 Boot Floppy
- 00 FDD A
- 01 FDD B
- 10 FDD C
- 11 FDD D

Bit [5:4]: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit [3:2]: Density Select
- 00 Normal (Default)
- 01 Normal
- 10 1 (Forced to logic 1)
- 11 0 (Forced to logic 0)

Bit 1: DISFDDWR
- 0 Enable FDD write.
- 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0: SWWP
- 0 Normal, use WP to determine whether the FDD is write protected or not.
- 1 FDD is always write-protected.

CRF2 (Default 0xFF)

Bit [7:6]: FDD D Drive Type

Bit [5:4]: FDD C Drive Type

Bit [3:2]: FDD B Drive Type

Bit [1:0]: FDD A Drive Type

CRF4 (Default 0x00)

FDD0 Selection:

Bit 7: Reserved.

Bit 6: Precomp. Disable.

1 Disable FDC Precompensation.

0 Enable FDC Precompensation.

Bit 5: Reserved.

Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).

00 Select Regular drives and 2.88 format

01 3-mode drive

10 2 Meg Tape

11 Reserved

Bit 2: Reserved.

Bit [1:0]: DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

CRF5 (Default 0x00)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

Drive Rate Table Select		Data Rate		Selected Data Rate		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0(pin 2)	DRVDEN1(pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5" 2/1 MB 5.25" 2/1.6/1 MB 3.5" (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

9.6 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0x78 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Parallel Port I/O base address.

[0x100:0xFFC] on 4 byte boundary (EPP not supported) or

[0x100:0xFF8] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x03)

Bit [7:3]: Reserved.

Bit [2:0]: These bits select DRQ resource for Parallel Port.

0x00=DMA0

0x01=DMA1

0x02=DMA2

0x03=DMA3

0x04 - 0x07= No DMA active

CRF0 (Default 0x3F)

Bit 7: Reserved.

Bit [6:3]: ECP FIFO Threshold.

Bit [2:0]: Parallel Port Mode (CR28 PRTMODS2 = 0)

100 Printer Mode

000 Standard and Bi-direction (SPP) mode

001 EPP - 1.9 and SPP mode

101 EPP - 1.7 and SPP mode

010 ECP mode

011 ECP and EPP - 1.9 mode

111 ECP and EPP - 1.7 mode (Default)

9.7 Logical Device 2 (UART A)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x03, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 1 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x04 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUACLKB1, SUACLKB0

00 UART A clock source is 1.8462 Mhz (24MHz/13)

01 UART A clock source is 2 Mhz (24MHz/12)

10 UART A clock source is 24 Mhz (24MHz/1)

11 UART A clock source is 14.769 Mhz (24mhz/1.625)

9.8 Logical Device 3 (UART B)

CR30 (Default 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x02, 0xF8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select Serial Port 2 I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x03 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 2.

CRF0 (De fault 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:4]: Reserved.

Bit 3: RXW4C

0 No reception delay when SIR is changed from TX mode to RX mode.

1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

0 No transmission delay when SIR is changed from RX mode to TX mode.

1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit [1:0]: SUBCLKB1, SUBCLKB0

00 UART B clock source is 1.8462 Mhz (24MHz/13)

01 UART B clock source is 2 Mhz (24MHz/12)

10 UART B clock source is 24 Mhz (24MHz/1)

11 UART B clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (Default 0x00)

Bit 7: Reserved.

Bit 6: IRLOCSEL. IR I/O pins' location select.

0 Through SINB/SOUTB.

1 Through IRRX/IRTX.

Bit 5: IRMODE2. IR function mode selection bit 2.

Bit 4: IRMODE1. IR function mode selection bit 1.

Bit 3: IRMODE0. IR function mode selection bit 0.

IR MODE	IR FUNCTION	IRTX	IRRX
00X	Disable	tri-state	high
010*	IrDA	Active pulse 1.6 µS	Demodulation into SINB/IRRX
011*	IrDA	Active pulse 3/16 bit time	Demodulation into SINB/IRRX
100	ASK-IR	Inverting IRTX/SOUTB pin	routed to SINB/IRRX
101	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	routed to SINB/IRRX
110	ASK-IR	Inverting IRTX/SOUTB	Demodulation into SINB/IRRX
111*	ASK-IR	Inverting IRTX/SOUTB & 500 KHZ clock	Demodulation into SINB/IRRX

Note: The notation is normal mode in the IR function.

Bit 2: HDUPLX. IR half/full duplex function select.
- 0 The IR function is Full Duplex.
- 1 The IR function is Half Duplex.

Bit 1: TX2INV.
- 0 the SOUTB pin of UART B function or IRTX pin of IR function in normal condition.
- 1 inverse the SOUTB pin of UART B function or IRTX pin of IR function.

Bit 0: RX2INV.
- 0 the SINB pin of UART B function or IRRX pin of IR function in normal condition.
- 1 inverse the SINB pin of UART B function or IRRX pin of IR function

9.9 Logical Device 7 (Game Port and GPIO Port 1)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0:
- 1 Game/GP1 Port is active.
- 0 Game/GP1 Port is inactive.

CR60, CR61 (Default 0x02, 0x01 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the Game Port base address [0x100:0xFFF] on 8 byte boundary.

CR62, CR63 (Default 0x00, 0x00)

These two registers select the GPIO1 base address [0x100:0xFFF] on 1 byte boundary

IO address : CRF1 base address

CRF0 (GP10-GP17 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP10-GP17 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

9.10 Logical Device 8 (MIDI Port and GPIO Port 5)

CR30 (MIDI Port Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 MIDI/GP5 port is activate

0 MIDI/GP5 port is inactive.

CR60, CR61 (Default 0x03, 0x30 if PNPCSV = 0 during POR, default 0x00 otherwise)

These two registers select the MIDI Port base address [0x100:0xFFF] on 2byte boundary.

CR62, CR63 (Default 0x00, 0x00)

These two registers select the GPIO5 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF1 base address

IO address + 1 : CRF3 base address

IO address + 2 : CRF4 base address

IO address + 3 : CRF5 base address

CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for MIDI Port .

CRF0 (GP5 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP5 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP5 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (PLED mode register. Default 0x00)

Bit [7:3] : Reserved .

Bit 2: select WDTO count mode.

- 0 second
- 1 minute

Bit [1:0]: select PLED mode

- 00 Power LED pin is tri-stated.
- 01 Power LED pin is droved low.
- 10 Power LED pin is a 1Hz toggle pulse with 50 duty cycle.
- 11 Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

CRF4 (Default 0x00)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit [7:0]: = 0x00 Time-out Disable
= 0x01 Time-out occurs after 1 second/minute
= 0x02 Time-out occurs after 2 second/minutes
= 0x03 Time-out occurs after 3 second/minutes
.....
= 0xFF Time-out occurs after 255 second/minutes

CRF5 (Default 0x00)

Bit [7] : Reserved .

Bit [6] : invert Watch Dog Timer Status

Bit 5: Force Watch Dog Timer Time-out, Write only*

- 1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4: Watch Dog Timer Status, R/W

- 1 Watch Dog Timer time-out occurred.
- 0 Watch Dog Timer counting

Bit [3:0]: These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

9.11 Logical Device 9 (GPIO Port 2 ~ GPIO Port 4)

CR30 (Default 0x00)

Bit [7:3]: Reserved.

Bit 2:	1	GP4 port is active.
	0	GP4 port is inactive
Bit 1:	1	GP3 port is active.
	0	GP3 port is inactive
Bit 0:	1	GP2 port is active.
	0	GP2 port is inactive.

CR60,CR61(Default 0x00,0x00).

These two registers select the GP2,3,4 base address(0x100:FFF) ON 3 bytes boundary.

IO address: CRF1 base address

IO address + 1 : CRF4 base address

IO address + 2 : CRF7 base address

CRF0 (GP2 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP2 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP2 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (GP3 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF4 (GP3 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF5 (GP3 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF6 (GP4 I/O selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF7 (GP4 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF8 (GP4 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

9.12 Logical Device A (ACPI)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resources for $\overline{SMI}$ / $\overline{PME}$

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level auto power management enable.

0 disable the auto power management functions

1 enable the auto power management functions.

Bit 6: Reserved. (Return zero when read)

Bit 5: MIDIPME. MIDI port auto power management enable.
- 0 disable the auto power management functions
- 1 enable the auto power management functions

Bit 4: Reserved. (Return zero when read)

Bit 3: PRTPME. PRT auto power management enable.
- 0 disable the auto power management functions.
- 1 enable the auto power management functions.

Bit 2: FDCPME. FDC auto power management enable.
- 0 disable the auto power management functions.
- 1 enable the auto power management functions.

Bit 1: URAPME. UART A auto power management enable.
- 0 disable the auto power management functions.
- 1 enable the auto power management functions.

Bit 0: URBPME. UART B auto power management enable.
- 0 disable the auto power management functions.
- 1 enable the auto power management functions.

CRF1 (Default 0x00)

Bit 7: WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1 to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.
- 0 the chip is in the sleeping state.
- 1 the chip is in the working state.

Bit 6: Reserved. (Return zero when read)

Bit 5: MIDI' s trap status.

Bit 4: Reserved. (Return zero when read)

Bit 3: PRT' s trap status.

Bit 2: FDC' s trap status.

Bit 1: URA' s trap status.

Bit 0: URB' s trap status.

CRF2 (Default 0x00)

Bit [7:3]: Reserved. (Return zero when read)

Bit 2: SC' s trap status.

Bit 1: URD' s trap status.

Bit 0: URC' s trap status.

CRF3 (Default 0x00)

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7: URDIRQSTS. URD IRQ status.

Bit 6: URCIRQSTS. URC IRQ status.

Bit [5:4]: Reserved. (Return zero when read)

Bit 3: PRTIRQSTS. PRT IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. UART B IRQ status.

CRF4 (Default 0x00)

These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 7: Reserved. (Return zero when read)

Bit 6: SCIRQSTS. SC IRQ status.

Bit [5:3]: Reserved. (Return zero when read)

Bit 2: WDTIRQSTS. Watch dog timer IRQ status.

Bit 1: Reserved. (Return zero when read).

Bit 0: MIDIIRQSTS. MIDI IRQ status.

CRF6 (Default 0x00)

These bits enable the generation of an $\overline{SMI}$/$\overline{PME}$ interrupt due to any IRQ of the devices.

$\overline{SMI}$/$\overline{PME}$ logic output = (PRTIRQEN and PRTIRQSTS) or (FDCIRQEN and FDCIRQSTS)
or (URAIRQEN and URAIRQSTS) or (URBIRQEN and URBIRQSTS)
or (URCIRQEN and URCIRQSTS) or (WDTIRQEN and WDTIRQSTS)
or (URDIRQEN and URDIRQEN) or (MIDIIRQEN and MIDIIRQEN)
or (SCIRQEN and SCIRQEN)

Bit 7: URDIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to URD's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to URD's IRQ.

Bit 6: URCIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to URC's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to URC's IRQ.

Bit [5:4]: Reserved (Return zero when read)

Bit 3: PRTIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to PRT' s IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to PRT' s IRQ.

Bit 2: FDCIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to FDC's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to FDC's IRQ.

Bit 1: URAIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART A's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART A's IRQ.

Bit 0: URBIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART B's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to UART B's IRQ.

CRF7 (Default 0x00)

These bits enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to any IRQ of the devices.

Bit 7: Reserved. (Return zero when read)

Bit 6: SCIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to SC timer's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to SC timer's IRQ.

Bit [5:3]: Reserved. (Return zero when read)

Bit 2: WDTIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to watch dog timer's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{SMI}$ interrupt due to watch dog timer's IRQ.

Bit 1: Reserved. (Return zero when read)

Bit 0: MIDIIRQEN.

0 disable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

1 enable the generation of an $\overline{SMI}$ / $\overline{PME}$ interrupt due to MIDI's IRQ.

CRF9 (Default 0x00)

Bit [7:3]: Reserved. Return zero when read.

Bit 2: PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

0 the power management events will generate an $\overline{SMI}$ event.

1 the power management events will generate an $\overline{PME}$ event.

Bit 1: FSLEEP: This bit selects the fast expiry time of individual devices.

0 1 S

1 8 mS

Bit 0: SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

0 neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

1 an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

CRFA (Default 0x00)

Bit [7:3]: Reserved. (Return zero when read)

Bit 2: SCPME. SC auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 1: URDPME. UART D auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

Bit 0: URCPME. UART C auto power management enable.

0 disable the auto power management functions.

1 enable the auto power management functions.

9.13 Logical Device B (PWM)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Pulse Width Modulation base address [0x100:0xFFF] on 8-byte boundary.

9.14 Logical Device C (SMART CARD)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activates the logical device.

0 Logical device is inactive.

CR60, CR61 (Default 0x00, 0x00)

These two registers select Smart Card base address [0x100:0xFFF] on 8-byte boundary.

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bit select IRQ resource for Smart Card interface.

CRF0 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Smart Card present signal (SCPSNT) is LOW active.

0 SCPSNT is HIGH active.

9.15 Logical Device D (URC & GPIO Port 6)

CR30 (Default 0x00)

Bit [7:2]: Reserved.

Bit 1: 1 Activate GPIO6.

0 GPIO6 is inactive

Bit 0: 1 Activate URC.

0 URC is inactive.

CR60, CR61 (Default 0x03, 0xE8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select the Serial Port 3 I/O base address [0x100:0xFF8] on 8byte boundary.

CR62, CR63 (Default 0x00)

These two registers select the GPIO6 base address [0x100:0xFFF] on 4byte boundary.

IO address: CRF2 base address

CR70 (Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 3.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUCCLKB1, SUCCLKB0

00 UART C clock source is 1.8462 Mhz (24MHz/13)

01 UART C clock source is 2 Mhz (24MHz/12)

10 UART C clock source is 24 Mhz (24MHz/1)

11 UART C clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (GP6 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF2 (GP6 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF3 (GP6 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF4 (GP6 output style register. Default 0x00)

When set to a '1', the outgoing port is pulse mode.

When set to a '0', the outgoing port is level mode.

9.16 Logical Device E (URD & GPIO Port 7)

CR30 (Default 0x00)

Bit [7:2]: Reserved.

Bit 1: 1 Activate GPIO7.

0 GPIO7 is inactive

Bit 0: 1 Activate URD.

0 URD is inactive

CR60, CR61 (Default 0x02, 0xE8 if PNPCSV = 0 during POR, default 0x00, 0x00 otherwise)

These two registers select the Serial Port 4 I/O base address [0x100:0xFF8] on 8byte boundary.

CR62, CR63 (Default 0x00)

These two registers select the GPIO7 base address [0x100:0xFFF] on 4byte boundary.

IO address : CRF2 base address

CR70(Default 0x00)

Bit [7:4]: Reserved.

Bit [3:0]: These bits select IRQ resource for Serial Port 4.

CRF0 (Default 0x00)

Bit 7: Reserved.

Bit 6: 1 Activates the logical device IRQ sharing function.

0 Logical device IRQ sharing is inactive.

Bit [5:2]: Reserved.

Bit [1:0]: SUDCLKB1, SUDCLKB0

00 UART D clock source is 1.8462 Mhz (24MHz/13)

01 UART D clock source is 2 Mhz (24MHz/12)

10 UART D clock source is 24 Mhz (24MHz/1)

11 UART D clock source is 14.769 Mhz (24mhz/1.625)

CRF1 (GP7 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF2 (GP7 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF3 (GP7 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

9.17 Logical Device F (GPIO Port 8)

CR30 (Default 0x00)

Bit [7:1]: Reserved.

Bit 0: 1 Activate GPIO8.

0 PIO8 is inactive.

CR60, CR61 (Default 0x00)

These two registers select the GPIO8 base address [0x100:0xFFF] on 2byte boundary.

IO address : CRF1 base address

CRF0 (GP8 selection register. Default 0xFF)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP8 data register. Default 0x00)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP8 inversion register. Default 0x00)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

10.0 ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83697SF	128-pin QFP	

11.0 HOW TO READ THE TOP MARKING

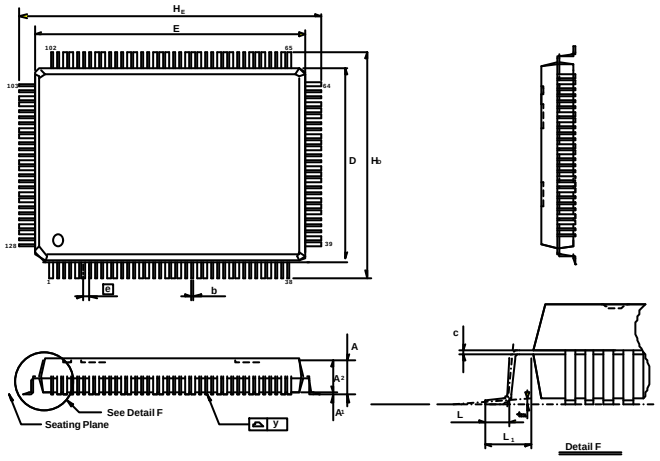
Example: The top marking of W83697SF

1st line: Winbond logo & SMART@IO
2nd line: the type number: W83697SF
3th line: the tracking code 109 G 5B B BA

109: packages made in 2001, week 09
G: assembly house ID; A means ASE, S means SPIL, G means GR, etc.
5B: Winbond internal use.
B: IC revision; A means version A, B means version B
BA: Winbond internal use.

12.0 PACKAGE DIMENSIONS

(128-pin PQFP)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A_1	0.25	0.35	0.45	0.010	0.014	0.018
A_2	2.57	2.72	2.87	0.101	0.107	0.113
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.90	14.00	14.10	0.547	0.551	0.555
E	19.90	20.00	20.10	0.783	0.787	0.791
e	—	0.50	—	—	0.020	—
H_D	17.00	17.20	17.40	0.669	0.677	0.685
H_E	23.00	23.20	23.40	0.905	0.913	0.921
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1	—	1.60	—	—	0.063	—
y	—	—	0.08	—	—	0.003
θ	0	—	7	0	—	7

Note:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion .
3. Controlling dimension : Millimeter
4. General appearance spec. should be based on final visual inspection spec.
5. PCB layout please use the "mm".

Winbond Electronics Corp.

Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668