Winbond Electronics Corp.

I/O COUPLER

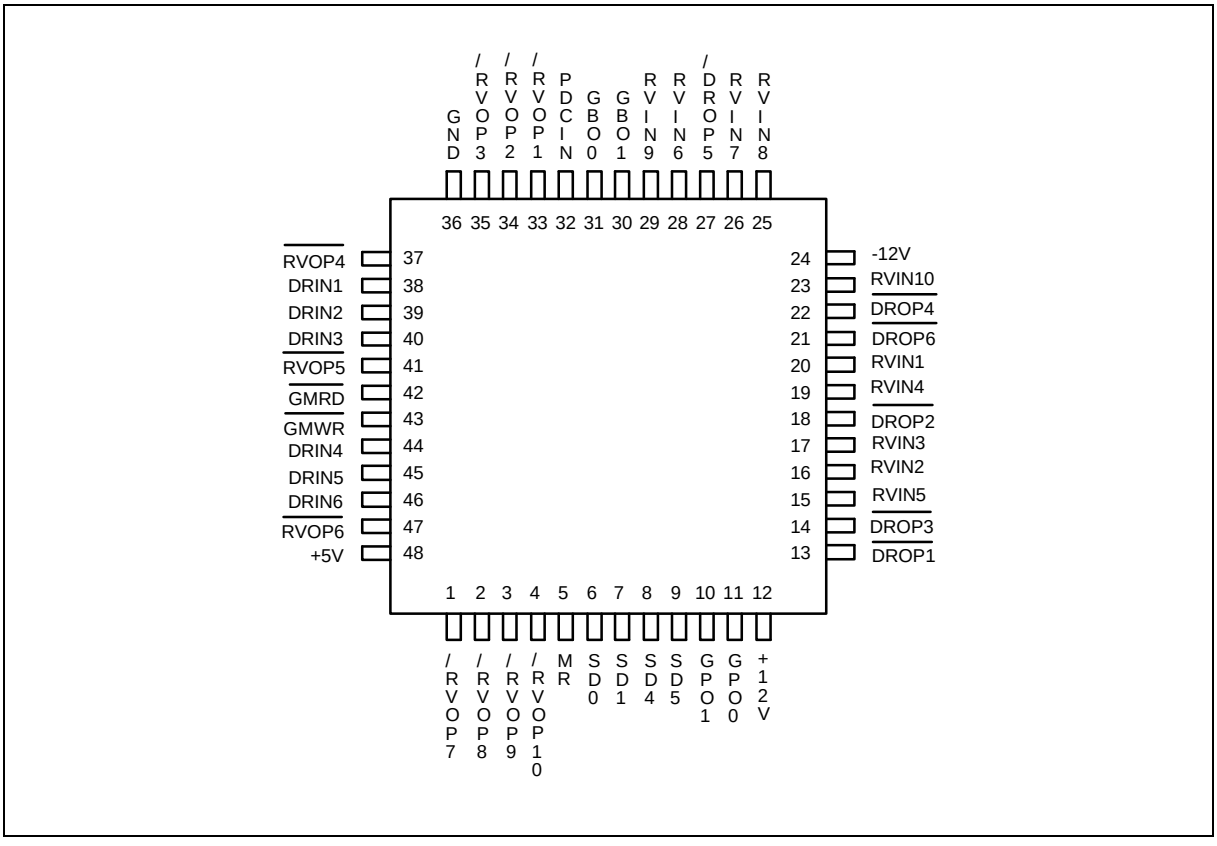
GENERAL DESCRIPTION

The W83768 is an I/O-coupler chip that includes six line drivers (1488), ten line receivers (1489), two timers (556), and one 244-type buffer block for game port signals. It also supports a power-down control circuit to reduce power consumption. This chip is intended for use with an I/O controller, and it is specifically designed to match the pin assignments of the Winbond Power I/O series. With this chip, engineers can easily design an all-in-one I/O circuit for personal computer systems without using any other TTL ICs.

FEATURES

- Six line drivers (1488), ten line receivers (1489), two timers (556), one buffer block for game port signals
- Supports two RS232 serial ports and one game port control logic circuit
- Power-down control function available
- Four power supplies needed: 0V, +5V, +12V, and -12V
- 48-pin QFP package

PIN CONFIGURATION



PIN DESCRIPTION

Power Pins

PIN NO.	SYMBOL	I/O	DESCRIPTION
36	GND	-	Ground
48	V_{CC}	-	+5V Power
12	V_{DD}	-	+12V Power
24	V_{SS}	-	-12V Power

Line Drivers

PIN NO.	SYMBOL	I/O	DESCRIPTION
38	DRIN1	I	Driver input 1
39	DRIN2	I	Driver input 2
40	DRIN3	I	Driver input 3
44	DRIN4	I	Driver input 4
45	DRIN5	I	Driver input 5
46	DRIN6	I	Driver input 6
13	$\overline{\text{DROP1}}$	O	Driver output 1
18	$\overline{\text{DROP2}}$	O	Driver output 2
14	$\overline{\text{DROP3}}$	O	Driver output 3
22	$\overline{\text{DROP4}}$	O	Driver output 4
27	$\overline{\text{DROP5}}$	O	Driver output 5
21	$\overline{\text{DROP6}}$	O	Driver output 6

Line Receivers

PIN NO.	SYMBOL	I/O	DESCRIPTION
20	RVIN1	I	Receiver input 1
16	RVIN2	I	Receiver input 2
17	RVIN3	I	Receiver input 3
19	RVIN4	I	Receiver input 4
15	RVIN5	I	Receiver input 5
28	RVIN6	I	Receiver input 6
26	RVIN7	I	Receiver input 7
25	RVIN8	I	Receiver input 8
29	RVIN9	I	Receiver input 9

Line Receivers, continued

PIN NO.	SYMBOL	I/O	DESCRIPTION
23	RVIN10	I	Receiver input 10
33	$\overline{\text{RVOP1}}$	I/O	During normal operations, this pin works as receiver output #1. During power-on reset, this pin is used to select power-down control (PDC) mode enable level. When $\overline{\text{RVOP1}}$ is set to high at power-on, PDC is high active. When $\overline{\text{RVOP1}}$ is set to low at power-on, PDC is low active.
34	$\overline{\text{RVOP2}}$	O	Receiver output 2
35	$\overline{\text{RVOP3}}$	O	Receiver output 3
37	$\overline{\text{RVOP4}}$	O	Receiver output 4
41	$\overline{\text{RVOP5}}$	O	Receiver output 5
47	$\overline{\text{RVOP6}}$	O	Receiver output 6
1	$\overline{\text{RVOP7}}$	O	Receiver output 7
2	$\overline{\text{RVOP8}}$	O	Receiver output 8
3	$\overline{\text{RVOP9}}$	O	Receiver output 9
4	$\overline{\text{RVOP10}}$	O	Receiver output 10

Game Port

PIN NO.	SYMBOL	I/O	DESCRIPTION
11	GPO0	I/O	Game port RC constant (open drain)
10	GPO1	I/O	Game port RC constant (open drain)
31	GBO0	I	Game port button input
30	GBO1	I	Game port button input
42	$\overline{\text{GMRD}}$	I	Game port read. This pin is internally pulled-up to make it convenient to disable the game port.
43	$\overline{\text{GMWR}}$	I	Game port write

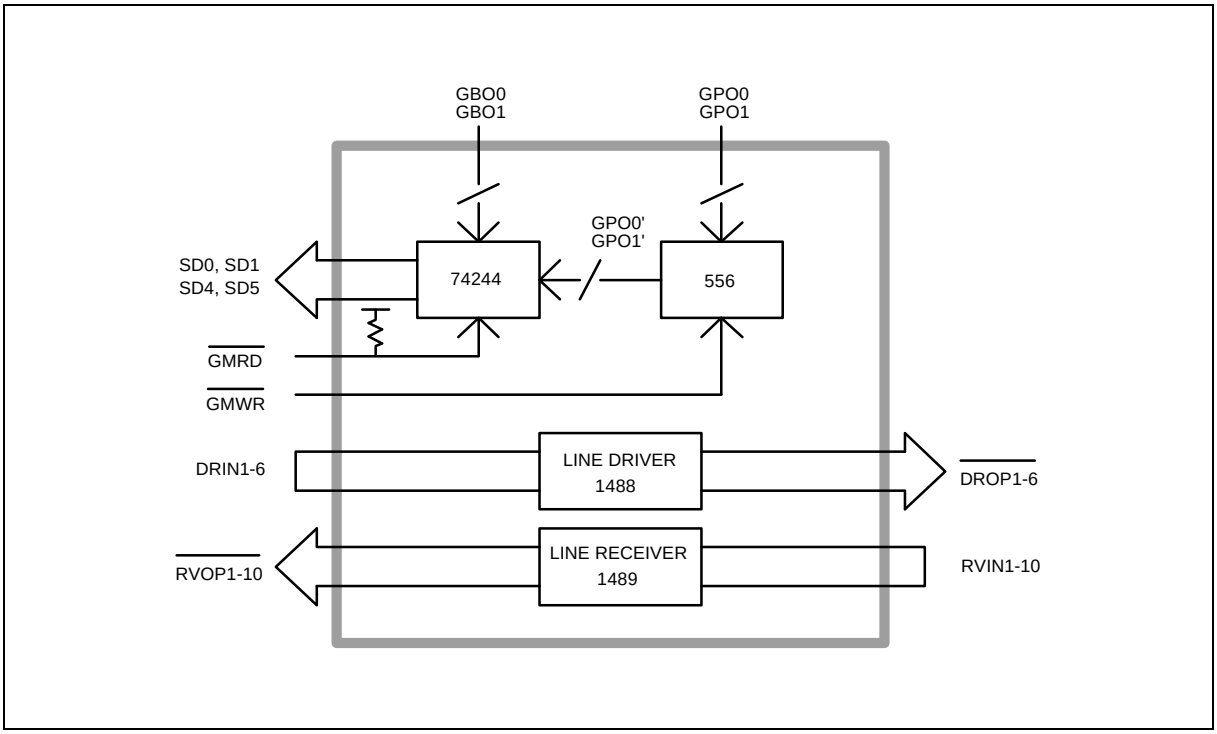
Control Signals

PIN NO.	SYMBOL	I/O	DESCRIPTION
5	MR	I	Master reset signal input
32	PDCIN	I	This pin is used to enable/disable the power-down function. The active level of this pin depends on how pin $\overline{\text{RVOP1}}$ is programmed at power-on. If $\overline{\text{RVOP1}}$ is set high at power-on, for example, then setting PDCIN to high will cause the W83768 to enter power-down mode.

Data Bus

PIN NO.	SYMBOL	I/O	DESCRIPTION
6	SD0	O	System data bit 0
7	SD1	O	System data bit 1
8	SD4	O	System data bit 4
9	SD5	O	System data bit 5

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Block 74244

This 244-type block functions as a buffer for reading game port buttons GBO0 and GBO1 and the status of block 556 output signals GPO0' and GPO1' on data bits 4, 5, 0, and 1, respectively.

Block 556

This block contains two independent 555-type timing circuits that are used to generate two separate one-shot signals. With these two one-shot pulses, the RC inputs of the game port can easily be measured. The $\overline{\text{GMWR}}$ signal is the trigger signal of block 556.

Line Driver Block 1488

This block contains six line drivers that are designed to serve as an interface between data terminal equipment and data communications equipment in conformance with the specifications of EIA standard RS-232C. The power requirements are +12V, 0V, and -12V.

Line Receiver Block 1489

This block contains ten line receivers that are designed to serve as an interface between data terminal equipment and data communications equipment in conformance with the specifications of EIA standard RS-232C. The power requirements are +12V, 0V, and -12V.

Power-Down Control Mode

When pin PDCIN is set active (active high or low determined by $\overline{\text{RVOP1}}$ at power-on reset), the W83768 enters power-down mode, and all output buffers (SD0, SD1, SD4, SD5, $\overline{\text{RVOP1}-10}$, $\overline{\text{DROP1}-6}$) will enter tri-state to reduce power consumption.

ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
Power Supply Voltage	GND, V_{CC}	0 to 5.5	V
	V_{SS}, V_{DD}	-13 to 13	
Input Voltage	Low Voltage	-0.5 to 7.0	V
	High Voltage	-12 to 12	
Operating Temperature		0 to 70	°C
Storage Temperature		-55 to 150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

Ta = 0° C to +70° C, V_{CC} = 5V, V_{DD} = 12V, V_{SS} = -12V, GND = 0V

PARAMETER	SYMBOL	MIN.	MAX.	NOTES
Input low voltage	V_{IL} (TTL)	-0.3V	+0.6V	MR, $\overline{\text{GMRD}}$, $\overline{\text{GMWR}}$
Input high voltage	V_{IH} (TTL)	+2.4V	V_{CC} +0.3V	MR, $\overline{\text{GMRD}}$, $\overline{\text{GMWR}}$
Input low voltage	V_{IL} (CMOS)	-0.3V	0.2 V_{CC}	DRIN1–6, GBO0–1, GPO0–1, PDCIN

DC Characteristics, continued

PARAMETER	SYMBOL	MIN.	MAX.	NOTES
Input high voltage	V_{IH} (CMOS)	+3.9V	V_{CC} +0.3V	DRIN1–6, GBO0–1, GPO0–1, PDCIN
Input low voltage	V_{IL} (HI-V)	V_{SS}	GND	RVIN1–10
Input high voltage	V_{IH} (HI-V)	2V	V_{DD}	RVIN1–10
Output low voltage	V_{OL}	-	0.4V	$\overline{\text{RVOP1–10}}$, SD0, SD1, SD4, SD5
Output high voltage	V_{OH}	+2.4V	-	$\overline{\text{RVOP1–10}}$, SD0, SD1, SD4, SD5
Output low voltage	V_{OL} (HI-V)	V_{SS}	-2V	$\overline{\text{DROP1–6}}$
Output high voltage	V_{OH} (HI-V)	+2V	V_{DD}	$\overline{\text{DROP1–6}}$

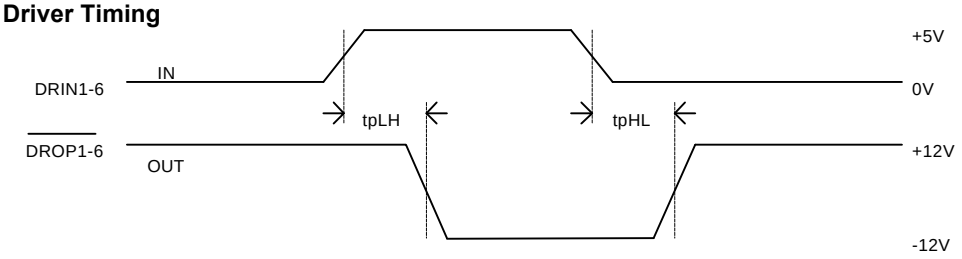
SYMBOL	CURRENT LEVEL					
	MAX.		MIN.		TYP.	
	I_{IL}	I_{IH}	I_{OL}	I_{OH}	I_{OL}	I_{OH}
MR	-20 µA	3 µA	-	-	-	-
PDCIN	-20 µA	3 µA	-	-	-	-
$\overline{\text{GMRD}}$, $\overline{\text{GMWR}}$	-20 µA	3 µA	-	-	-	-
GBO0, GBO1	-20 µA	3 µA	-	-	-	-
RVIN1–10	-1 mA	3 µA	-	-	-	-
GPO0, GPO1	-	-	1.5 mA	-	2 mA	-
SD0, SD1, SD4, SD5	-	-	5.5 mA	4 mA	8 mA	6 mA
$\overline{\text{RVOP1–10}}$	-	-	2 mA	2 mA	3 mA	3 mA
$\overline{\text{DROP1–6}}$	-	-	10 mA	10 mA	14 mA	16 mA

AC CHARACTERISTICS

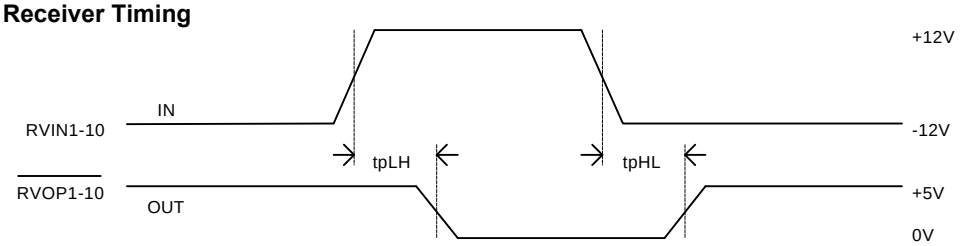
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
1488 tpLH	DRIN1–6	-	60	90	nS
1488 tpHL	$\overline{\text{DROP1–6}}$	-	60	90	nS
1489 tpLH	RVIN1–10	-	60	90	nS
1489 tpHL	$\overline{\text{RVOP1–10}}$	-	60	90	nS
tD	SD0, SD1, SD4, SD5	-	90	120	nS

TIMING WAVEFORMS

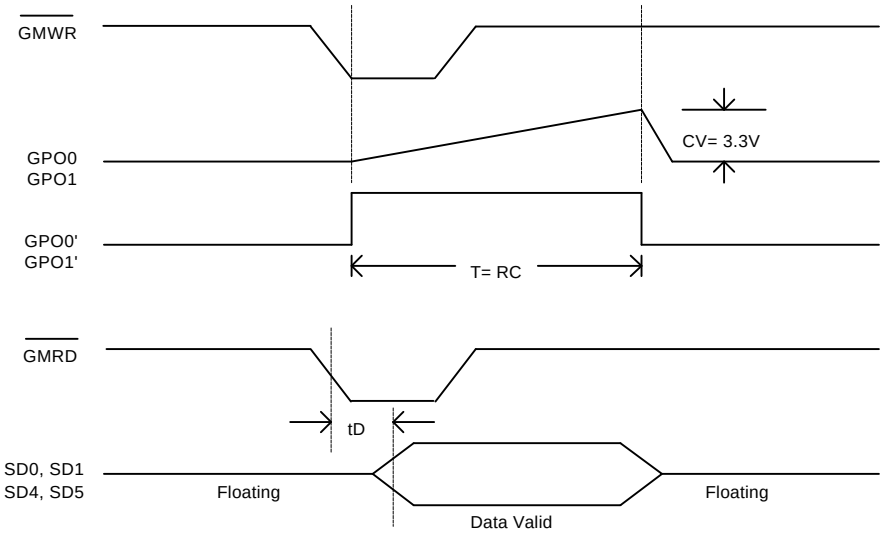
Driver Timing



Receiver Timing

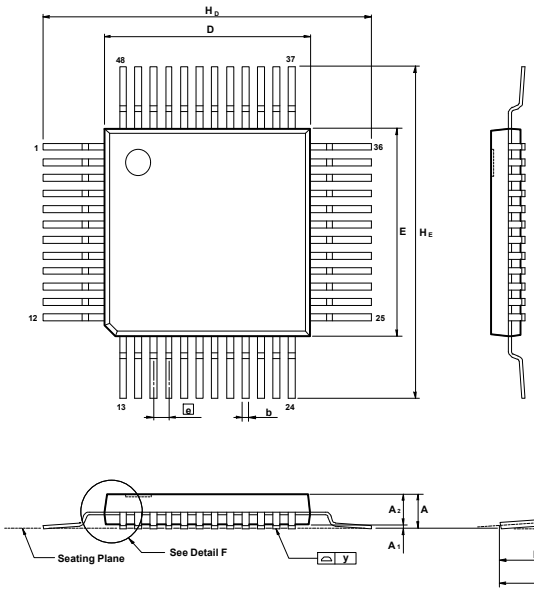


Timer Timing



PACKAGE DIMENSIONS

48-lead QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	0.070	---	---	1.78
A_1	0.004	---	---	0.10	---	---
A_2	0.052	0.057	0.062	1.32	1.45	1.58
b	0.011	0.013	0.017	0.28	0.33	0.43
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.389	0.394	0.399	9.87	10.00	10.13
E	0.389	0.394	0.399	9.87	10.00	10.13
e	0.024		0.036	0.60	0.75	0.90
H_D	0.618	0.630	0.642	15.70	16.00	16.30
H_E	0.618	0.630	0.642	15.70	16.00	16.30
L	0.067	0.075	0.083	1.70	1.90	2.10
L_1	0.110	0.118	0.126	2.79	3.00	3.20
y	---	---	0.006	---	---	0.15
θ	0°	---	15°	0°	---	15°

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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