W83791D
Winbond H/W Monitoring IC

Winbond Electronics Corp.

Preliminary

W83791D Data Sheet Revision History

	Pages	Dates	Version	Version on Web	Main Contents
1	n.a.			n.a.	All version before 0.20 are for internal use.
2	n.a.	01/Jan	0.2	n.a.	First publication.
3	P.7	01/Jan	0.21	n.a.	Revise SLOTOCC# pin description.
4	P.34	01/Jan	0.21	n.a.	Add SMI# /IRQ for Voltage/Fan description.
5	P.43/44	19/Mar	0.3	n.a.	Register Index 1Ah~1Fh revised.
6	P. 40 P. 42 P. 60/61 P. 58/59 P. 66 P. 66 P. 66 P. 87	21/May	0.4	n.a.	This update is for **C version** IC. 1) Add EVNTRAP1-5 polarity (Index Ah) 2) Add VID protection control bit (Index15h bit5) 3) Add FAN1-3/PWMOUT1-3 as GPIn data register. (Index 95h/97h) 4) SMARTFAN™ step up/down time registers exchanged. 5) Add a bit (Index A6 bit7) to know either speech or GPIO function did you use. 6) Pin44 (SMI#/LEDOUT) is a multi-function, it is programmable. 7) EVENTRAP can as GPIO by programming Index A6h bit0-4 . 8) Updated V0.17 schematics adding LEDOUT circuit for SMI# (Pin 44)
7	All pages	09/Aug	0.41	n.a.	Repaginate datasheet

LIFE SUPPORT APPLICATIONS

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1. GENERAL DESCRIPTION

W83791D is an evolving version of the W83782D --- Winbond's most popular hardware status monitoring IC. Besides the conventional functions of W83782D, W83791D uniquely provides several innovative features such as speech function, ASF sensor compliant, SMBus 2.0 ARP command compatible, VID table selection trapping, and 5VID output control. Conventionally, W83791D can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end computer system to work stably and efficiently. As for data access, W83791D provides slave SMBus 2.0 interface which can reply PEC (Packet Error Code) when as ASF sensor.

An 8-bit analog-to-digital converter (ADC) was built inside W83791D. W83791D can simultaneously monitor 10 analog voltage inputs (including power VDD/5VSB monitoring), 5 fan tachometer inputs, 3 remote temperatures, and one case open detection signal. The sense of remote temperature can be performed by thermistors, 2N3904 NPN-type transistors, or directly from Intel™ CPU with thermal diode output. W83791D provides 3 PWM (pulse width modulation) outputs for two modes of smart fan control-**"** Thermal Cruise™ **"** mode and **"**Speed Cruise**"** mode. Under **"** Thermal Cruise™ **"** mode, temperatures of CPU and the system can be maintained within specific programmable ranges under the hardware control. **"**Speed Cruise**"**, namely, is to keep the fan operate in the specific programmable r.p.m . As for warning mechanism, W83791D provides speech voice warning, beep tone warning, and SMI#, OVT#, IRQ signals for system protection events.

Additionally, 5 VID inputs are provided to read the VID of CPU (i.e. Pentium™ II/III) if applicable. These VID inputs provide the information of Vcore voltage that CPU expects. Furthermore, W83791D provides programmable VID output control to alter the voltage CPU consumes. W83791D also uniquely provides an optional feature: early stage (before BIOS was loaded) beep / speech warning to detect if the fatal elements present --- Vcore or +3.3V voltage fail and thus the system can not be boomed up. If the VSB power on setting refers to Intel VRM 9.x, the VID table within W83791D will be according to the new one. W83791D also has 2 specific pins to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C™ interface.

W83791D speech function is enabled by building in a programmable speech synthesizer with a 9-bit current DAC output as well as a connectable external flash memory for storing voice data. W83791D supports 1 CPU present or absent event trap, 5 external event traps, 17 hardware monitor event traps (10 analog voltage, 3 fan tachometer, 3 remote temperature, 1 case open) and 128 internal programmable event traps, amounting to 151 different speech outputs. If more than two events happen simultaneously, the priority set is: SLOTOCC# > EVNTRP1 > EVNTRP2 > EVNTRP3 > EVNTRP4 > EVNTRP5 > 128 Programmable events (Bank0 index 09h) > 17 Hardware status events. Voice data stored in the external flash memory interface with Winbond W55FXX is flexible to change by Winbond application software and **on-line** programming flash data is provided also. Besides, An external resistor is added to provide ring oscillator.

When you do not use the speech function, W83791D provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a pre-defined alternate function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.

W83791D can uniquely serve as an ASF sensor to respond to ASF master's req uest for the implementation of network management in OS-absent state. Through W83791D's compliance with ASF sensor spec , network server is able to monitor the environmental status of the client in OS-absent state by PET frame values returned from W83791D, such as temperatures, voltages, fan speed, and case open. Moreover, W83791D supports SMBus 2.0 ARP command to solve the problem of address conflicts by dynamically assigning a new unique address to W83791D after W83791D's UDID is sent.

Through the application software or BIOS, the users can read all the monitored parameters of the system

from time to time. A pop-up warning can also be activated when the monitored item is out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, Intel™ LDCM (LanDesk Client Management), or other management application software. Besides, the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and activate one programmable and maskable interrupts. An optional beep tone could be used as a warning signal when the monitored parameters are out of the preset range.

2. FEATURES

2.1 Monitoring Items

- 10 voltage inputs
  --- Typical for VCORE, +3.3V, +12V, -12V, +5V, -5V, +5VSB, VBAT, and two reserved
- 5 fan speed monitoring inputs
- 3 temperature inputs from remote thermistors, 2N3904 NPN-type transistors or Pentium™ II (Deschutes) thermal diode output
- Case open detection input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.2 Address Resolution Protocol (ARP) and Alert-Standard Forum(ASF)

- Support System Management Bus (SMBus) version 2.0 specification
- Comply with hardware sensor slave ARP (Address Resolution Protocol)
- Response sensor type ARP command
- Response ASF command --- Get Event Data , Get Event Status
- Comply with ASF sensors (Monitoring fan speed, voltage, temperature, and case open)

2.3 Speech Items

- Programmable speech synthesizer with new high fidelity synthesis algorithm
- Build in 8-bit current D/A converter
- 1 CPU present or absent trigger input
- 5 External trigger inputs
- 128 Internal programmable trigger inputs
- 17 H/W Monitor event trigger inputs
- Programmable 0-255 seconds timeout trigger inputs for firmware or software
- Instruction cycle is ¡ Ø00 £ § typically
- Section control provided in each voice section
- External resistor for ring oscillator

2.4 Actions Enabling

- Beep tone warning separated speech output
- 5 PWM (pulse width modulation) outputs for fan speed control (1~3 support Smart Fan control) and 5 Fan speed inputs for monitoring --- Total up to 5 sets of fan speed monitoring and controlling
- Issue SMI#, OVT#, IRQ signals to activate system protection
- Warning signal pop-up in application software

2.5 Enhance Monitoring VID function

- CPU Voltage ID reading
- VID output control
- Enhance beep warning by detecting Intel VRM 9.0 VID

2.6 General

- I^2C^{TM} serial bus interface
- 5 VID input pins for CPU VCORE identification (for Pentium™ II/III)
- Initial power fault beep (for +3.3V, VCORE)
- 2 pins (A0, A1) to provide selectable address setting for application of multiple devices (up to 4 devices) wired through I^2C^{TM} interface

Winbond hardware monitoring application software (Hardware Doctor™) support, for both Windows 95/98/2000 and Windows NT 4.0/5.0

- Internal clock Oscillator with 3M Hz
- 5V VSB operation

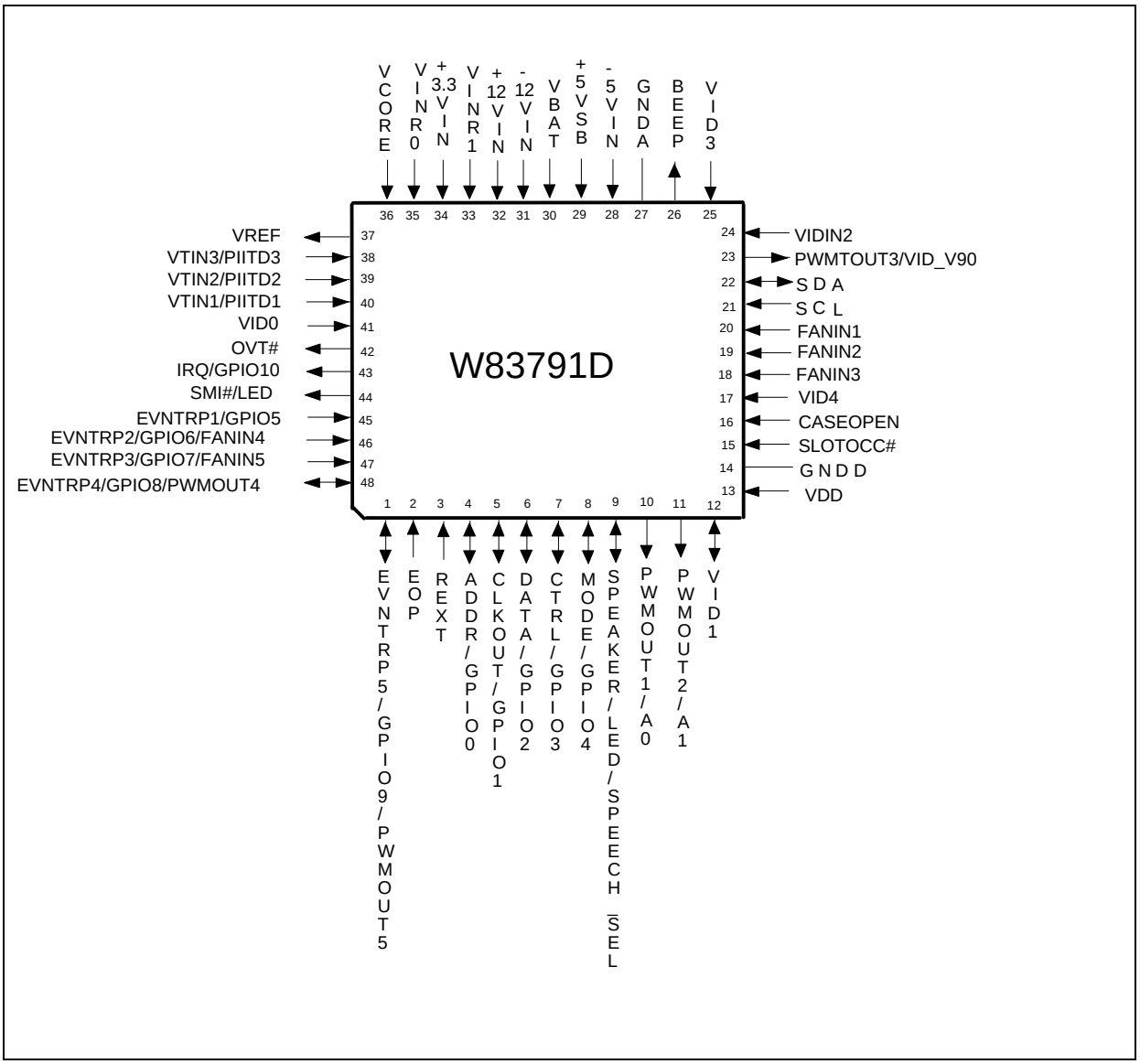
2.7 Package

- 48-pin LQFP

3. KEY SPECIFICATIONS

• Voltage monitoring accuracy	±1% (Max)
• Intel VRM 9.x Voltage monitoring accuracy	±0.5% (Max)
• Monitoring Temperature Range and Accuracy	
- 40°C to +120°C	± 3°C(Max)
• Supply Voltage	5V
• Operating Supply Current	5 mA typ.
• ADC Resolution	8 Bits

4. PIN CONFIGURATION



5. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability
I/O_{12ts} - TTL level and schmitt trigger with 12 mA source-sink capability
I/O_{8ts} - TTL level and schmitt trigger with 8 mA source-sink capability
I/O_{6ts} - TTL level and schmitt trigger with 6 mA source-sink capability
I/OD_{12ts} - TTL level and schmitt trigger open drain output with 12 mA sink capability
OUT_{12} - Output pin with 12 mA source-sink capability
OD_{12} - Open-drain output pin with 12 mA sink capability
AOUT - Output pin(Analog)
IN_t - TTL level input pin
IN_{ts} - TTL level input pin and schmitt trigger
AIN - Input pin(Analog)

Pin Name	Pin No.	Type	Description
EVNTRP5 /	1	I/O_{12t}	Event trapping to selection speech output sound. Default is high edge trigger.
GPIO9/ PWMOUT5			General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or PWMOUT Fan control can be selected by registers, but the PWMOUT can not support Smart Fan.
EOP	2	I	End of Process signal input from cascaded Flash.
GPIO11		I/OD_{12ts}	General purpose I/O function pin. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
REXT	3	I	Resistor(Rosc) connect to VSB used to adjust ring oscillator frequency.
ADDR /	4	OUT_{12}	Speech address pulse output, connect to W55FXX. When this pin translates from logic high to logic low, it will latch the data pin 6 and shift it into a speech flash address counter.
GPIO0		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
CLKOUT /	5	OUT_{12}	Speech clock output, for speech data read-out and write-in, connect to W55FXX. When this pin translates from logic high to logic low, the data pin 6 will be latched by this clock.
GPIO1		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
DATA /	6	I/O_{12t}	Serial data input/output, connect to W55FXX. The pin is latched by CLKOUT and ADDR acted as speech data and address respectively.
GPIO2		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
CTRL /	7	OUT_{12}	Output clock numbers of this pin decide which mode is selected. Connect to W55FXX.
GPIO3		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
MODE /	8	OUT_{12}	Output mode signal to W55FXX serial Flash.

GPIO4		I/OD_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
SPEAKER	9	OUT_{12}	Current type output driving an external speaker. The function is only working in VDD 5V OK.
LED		OUT_{12}	LED output control. This is a multi-function pin with SPEAKER. When the LED_SEL register (Bank0 Index 17h) is set to 1, LED output function will be active. Otherwise, set to 0 (default), this pin serves as SPEAKER output.
SPEECH_SEL		IN_{ts}	During VSB 5V power on, this pin is used to trap whether using speech function or GPIO function. Trapping low means using speech function (i.e. pin45-48, pin1, pin4-8 are as speech function). Trapping high means using GPIO function (i.e. pin45-48, pin1, pin4-8 are as GPIO function). The I/O control and status is defined in BANK0 Index 13h~16h.
PWMOUT1/	10	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A0		IN_{ts}	I^2C device address bit0 trapping during 5VSB power on.
PWMOUT2 /	11	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
A1		IN_{ts}	I^2C device address bit1 trapping during 5VSB power on.
VID1	12	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
VDD (5V)	13	POWER	+5V VDD power. Bypass with the parallel combination of 10µF (electrolytic or tantalum) and 0.1µF (ceramic) bypass capacitors.
GNDD	14	DGROUND	Internally connected to all digital circuitry.
SLOTOCC#	15	IN_{ts}	CPU presence signal. 0, means CPU is present. 1, means CPU is absent.
CASEOPEN	16	I/O_{6ts}	CASE OPEN detection. An active high input from an external device when case is Intruded. This signal can be latched in external circuit which power is supplied by VBAT, even if W83791D is power off.
VID4	17	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
FAN3IN- FAN1IN	18-20	IN_{ts}	0V to +5V amplitude fan tachometer input
SCL	21	IN_{ts}	Serial Bus Clock.
SDA	22	I/OD_{8ts}	Serial Bus bi-directional Data.
PWMOUT3 /	23	OUT_{12}	Fan speed control PWM output. When the power of VDD is 0v, this pin will drive logic 0. The power of this pin is supplied by VSB 5V.
VID_V90		IN_{ts}	VID table selection trapping during RSMRST (0: Intel VRM 8.2/8.3; 1: Intel VRM 9.0). When the trapping pin get a logic 1, the beep warning function is according to Intel VRM 9.0 VID.
VID2	24	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
VID3	25	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.

BEEP	26	OD_{12}	Alarm beep output. Normal, this pin is low. When abnormal event happens, this pin will output alarm frequency.
GNDA	27	AGROUND	Internally connected to all analog circuitry. The ground reference for all analog inputs.
-5VIN	28	AIN	0V to 4.096V FSR Analog Inputs.
+5VSB	29	POWER	This pin is power for W83791D. Bypass with the parallel combination of 10µF (electrolytic or tantalum) and 0.1µF (ceramic) bypass capacitors.
VBAT	30	POWER	This pin is power for W83791D.
-12VIN	31	AIN	0V to 4.096V FSR Analog Inputs.
+12VIN	32	AIN	0V to 4.096V FSR Analog Inputs.
VINR1	33	AIN	0V to 4.096V FSR Analog Inputs.
+3.3VIN	34	AIN	0V to 4.096V FSR Analog Inputs.
VINR0	35	AIN	0V to 4.096V FSR Analog Inputs.
VCORE	36	AIN	0V to 4.096V FSR Analog Inputs.
VREF	37	AOUT	Reference voltage.
VTIN3 / PIITD3	38	AIN	Thermistor 3 terminal input.(Default). Pentium™ II diode 3 input. This multi-functional pin is programmable.
VTIN2 / PIITD2	39	AIN	Thermistor 2 terminal input. (Default). Pentium™ II diode 2 input. This multi-functional pin is programmable.
VTIN1 / PIITD1	40	AIN	Thermistor 1 terminal input. (Default). Pentium™ II diode 1 input. This multi-functional pin is programmable.
VID0	41	I/O_{12ts}	Voltage Supply readouts from CPU. After programming, this pin can be VID output to voltage regulator to generate Vcore for CPU.
OVT#	42	OD_{12}	Over temperature Shutdown Output for temperature sensor 1-3.
IRQ / GPIO10	43	OUT_{12} I/OD_{12ts}	Interrupt request. General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active.
SMI# / LED	44	OD_{12} OUT_{12}	System Management Interrupt (open drain). LED output control. This is a multi-function pin with SMI. When the register (Bank0 Index 17h bit7 and Index A6h bit 6) is set to 1, LED output function will be active. Otherwise, set to 0 (default), this pin serves as SMI#.
EVNTRP2-3/ GPIO6-7/ FANIN4-5	46-47	I/O_{12ts} I/O_{12ts}	Event trapping to selection speech output sound. Default is high edge trigger. General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this speech function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or FAN inputs can be selected by registers.
EVNTRP4/	48	I/O_{12ts}	Event trapping to selection speech output sound.

GPIO8/ PWMOUT4		I/O_{12ts}	General purpose I/O function. If pin 9 (SPEECH_SEL) is trapped to high at VSB power on, this function will be active. The I/O control and status is defined in BANK0 Index 13h~14h. Otherwise, GPIO pin or PWMOUT Fan control can be selected by registers, but the PWMOUT can not support Smart Fan.

6. FUNCTION DESCRIPTION

6.1 General Description

The W83791D provides 10 analog positive inputs, 5 fan speed inputs , at most 5 sets for fan PWM (Pulse Width Modulation) control, 3 thermal inputs from remote thermistors ¡ B2N3904 transistors or Pentium™ II/III (Deschutes) thermal diode outputs, case open detection and beep function output when the monitored values exceed preset ranges , including the voltage, temperature, and fan count. Moreover, W83791D uniquely provides several innovative and practical functions to make the whole system more efficient and compliant with future trend of network management, such as speech function, ASF sensor compliant, SMBus 2.0 ARP command compatible, VID table selection trapping, 5VID output control, and so forth. Once the monitoring function ofW83791D is enabled, the watch dog machine will monitor every function and store the values to registers for comparison with preset ranges. If the monitoring value exceeds the limit value, the interrupt status will be set to 1 and W83791D will issue interrupt signals such as SMI# and IRQ if not masked..

6.2 Access Interface

The W83791D provides I^2C Serial Bus for microprocessor to read/write internal registers. In the W83791D, there are three serial bus addresses. Through the first address defined at CR[48h], all the registers can be read and written except CPUT1/CPUT2 temperature sensor registers. The read/write of the CPUT1/CPUT2 temperature sensor registers can be implemented through the second address (defined at CR[4Ah] bit2-0) and the third address (defined at CR[4Ah] bit6-4).

The first serial bus address of W83791D has 2 hardware setting bits set by pin10-11. The address is 001011[pin11][pin10]. Hence, the content of CR[48h] would be 00101110 if pin11=1 and pin10=0 .

6.2.1 The first serial bus access timing

(a) Serial bus write to internal address register followed by the data byte

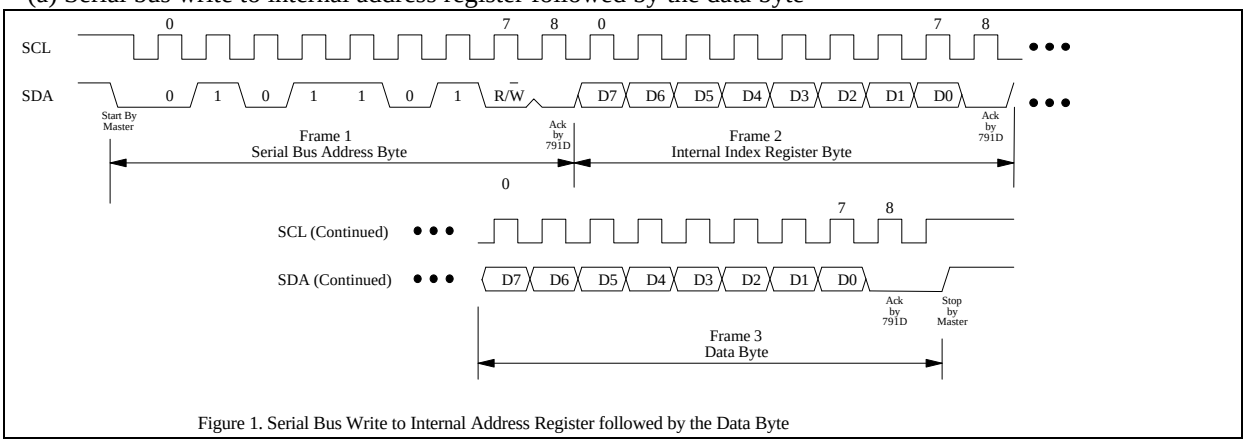


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus read from a register

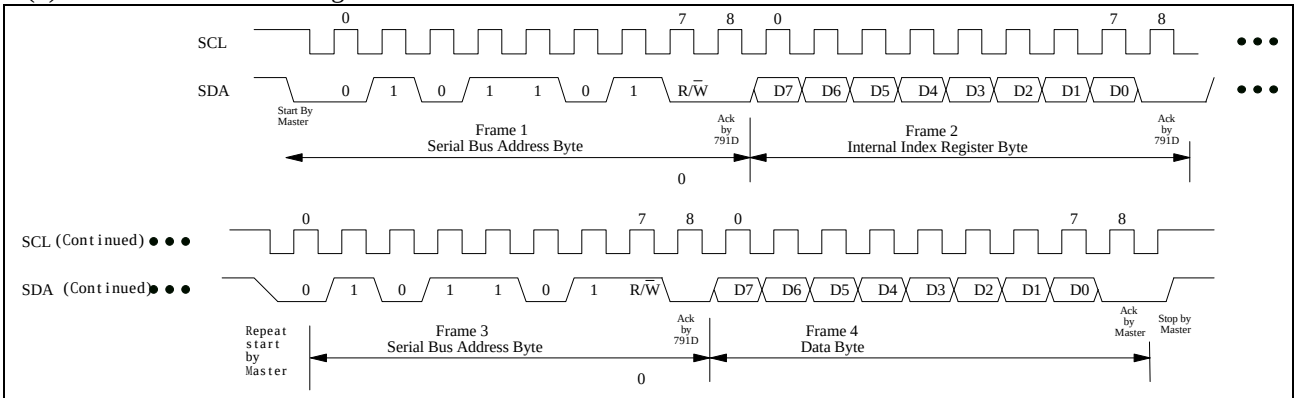


Figure 2. Serial Bus Read from Internal Address Register

6.3 Speech Function

6.3.1 General Description

The W83791D is a derivative of Winbond's *PowerSpeech*™ synthesizers. There are up to 5 hardware trigger inputs, 17 Hardware Monitor event and 128 programmable software event trigger inputs. If more than two events happen simultaneously, the priority set by the internal H/W is: SLOTOCC# > EVNTRAP1 > EVNTRAP2 > EVNTRAP3 > EVNTRAP4 > EVNTRAP5 > TRIGREG(Index 09h) 128 events > VIN0 > VIN1> others (VIN2 – VIN9,TEMP, FAN, case open). Software trigger is able to accommodate 128 event triggers, with timeout register (index 08h) enabled in advance for allowance of time on detecting devices. That is, once the system's power is on, BIOS can fill trigger event and speech voice will not be sent till the system fails owing to timeout. In addition, to prevent events from taking place simultaneously.

6.3.2 Event Trigger Queue

W83791D provides 8 byte FIFO queue to store event trigger, i.e, the first 8 event can be served by speech and speech will clear FIFO queue after service. Coding of Speech program must assign correct CPU_MODE event vector to issue correct speech voices correspondent to speech trigger events. For example, CPU_MODE event vector =1 represents absence of CPU, then coding speech with CPU is absent voice. When W83791D detects no CPU exists, it will send vector = 1 to speech synthesizer and play this voice data. Following is the block diagram of the 8-Byte event trigger queue.

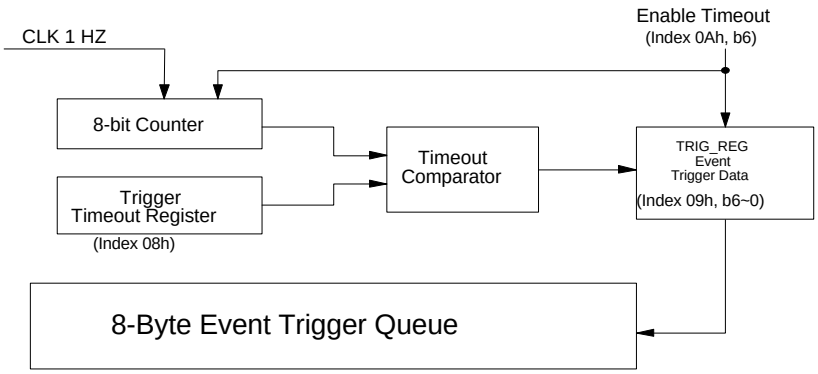


Figure 3. Event trigger Queue

For example: As BIOS usually has POST (Power On Self Test) program, then it will test every item step by step if no failure takes place, however, if it detects a failure on a specific item, it will hang on there. Therefore, BIOS could write timeout value to register 08h and start timer setup speech trigger event (register 09h), then is BIOS test program started. Whenever the system is hang on specific item such as DRAM testing, W83791D would say "DRAM test fails" after the timeout previously set at CR[08h]. On the contrary, if DRAM test is ok, then BIOS could update the timeout value and proceed to the next test program.

Below is the speech CPU_MODE table of W83791D**:**

CPU_MODE item	Definition	Vector (H)
POI	Reserverd	0,32
SLOTOCC	CPU present or absent	1
EVNTRAP1(TG1)	Hardware trgger1	2
EVNTRAP2	Hardware trgger2	3
EVNTRAP3	Hardware trgger3	4
EVNTRAP4	Hardware trgger4	5
EVNTRAP5	Hardware trgger5	6
TRIGREG	I2C setting software trigger	80-FF
IN0	Vcore(VIN0) exceed limit	40
IN1	VINR0(VIN1) exceed limit	41
IN2	(+3.3VIN)VIN2 exceed limit	42
IN3	(5VDD)VIN3 exceed limit	43
IN4	(+12VIN)VIN4 exceed limit	44
IN5	(-12VIN)VIN5 exceed limit	45
IN6	(-5VIN)VIN6 exceed limit	46
IN7	VSB(VIN7) exceed limit	47
IN8	VBAT(VIN8) exceed limit	48
IN9	(VINR1)VIN9 exceed limit	49
TEMP1	VTIN1 exceed limit	4A
TEMP2	VTIN2 exceed limit	4B
TEMP3	VTIN3 exceed limit	4C
FAN1	FAN1 count over limit	4D
FAN2	FAN2 count over limit	4E
FAN3	FAN3 count over limit	4F
CHS_EV	Case open trigger	50

Table 1. CPU_MODE Table

6.3.3 Connection of EEPROM

As is described previously that the W83791D has connectable W55FXX to store voice data. To expand the storage capacity, users can select many W55FXX to connect with each other. The maximum capacity could be up to 16Mbit. Following is the connection chart of W55FX with W83791D.

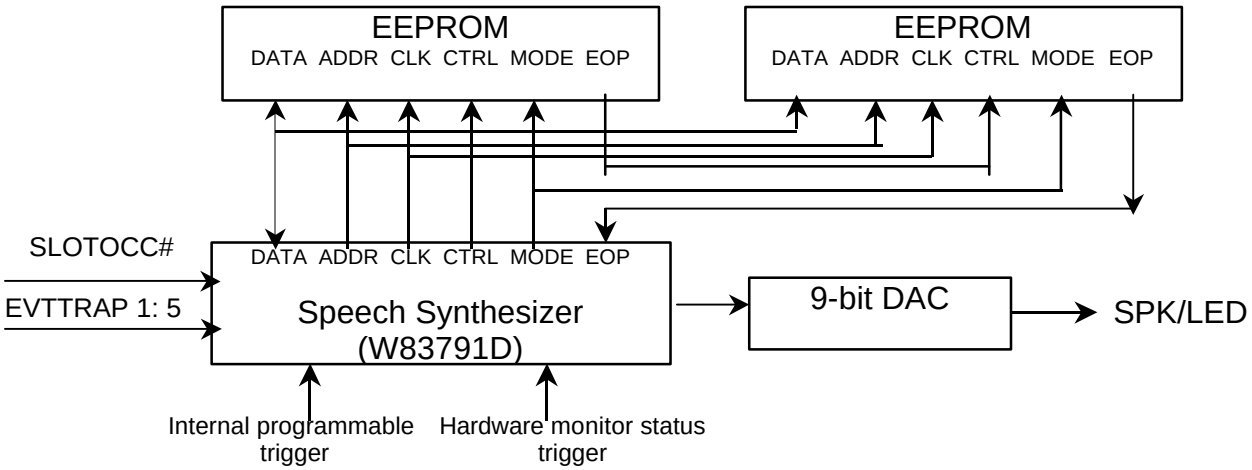


Figure 4. Speech Function Diagram

6.3.4 Speaker Output

Speech output pin is a 8 bit Current D/A converter, with which loading is needed. The resistor could range from 510~1K ohm and bipolar could be a low power NPN bipolar with £]of 120 - 160 . Usually, an 8050D transistor is appropriate. The spec of speaker is 8 Ω. Besides, SPK can also connect to AC97 codec chip Line_Out. C is decouple capacitor and is usually 200p- 0.01uF

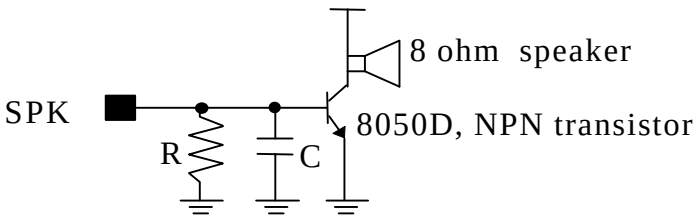


Figure. 5

6.4 Address Resolution Protocol (ARP) Introduction

As the W8791D is a slave device existing on the System Management Bus, it must have a unique address to prevent itself from conflicting with the other devices existing on the same bus. In order to solve the problem of address conflicts, SMBus version 2.0 introduces the concept of dynamically assigned address called Address Resolution Protocol (ARP). By such mechanism, each device existing on the SMBus will be given an unique slave address if it is a ARP-capable device. Thus, to meet the new spec, W83791D uniquely provides ARP compliant function to acquire an unique slave address.

The typical process of ARP contains several steps, including Prepare to ARP, Reset Device, Get UDID, Assign Address, and so on. Whenever the slave device accepts the command of ARP master, it must reply an Acknowledgement to the ARP master, thus the ARP master is able to carry on the next step. In order to provide a mechanism to isolate device for the purpose of address assignment, each device must implement a unique device identifier (UDID). The UDID is a 128-bit number comprised of several field, including Device Capabilities, Version Revision, Vendor ID, Device ID, Interface, Subsystem Vendor ID, Subsystem Device ID, and Vendor Specific ID. After the UDID of the device is sent to the ARP master, the ARP master will then assign a random address not in the Used Address Pool to the device

Generally speaking, there are eleven possible commands to read /write the data of SMBus device, and a slave device may use any or all of the eleven protocols to communicate. These protocols are Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read word, Process Call, Block Write, and Block Write-Block Read Process Call. W83791D itself supports the Block Write-Block Read Process with PEC to communicate with ARP Master. Following is a description of the SMBus packet protocol diagrams element key.. Not all protocol elements will be present in every command, that is, not all packets are required to include the Packet Error Code.

1-bit	7	1	1	8	1	8	1	1-bit
S	Slave Address	Wr	A	Command	A	PEC	A	P

S	Start Condition
Sr	Repeated Start Condition
Rd	Read (bit value of 1)
Wr	Write (bit value of 0)
A	Acknowledge (this bit position may be '0' for an ACK or '1' for a NACK)
P	Stop Condition
PEC	Packet Error Code
☐	Master-to-Slave
▒	Slave-to-Master

Relative command list:

Slave address	Command	Description
C2h	01h	Prepare to ARP
C2h	02h	Reset device (general)
C2h	03h	Get UDID (general)
C2h	04h	Assign address
C2h	Slave_Addr | 1	Direct Get UDID
C2h	Slave_Addr | 0	Direct Reset
C2h	05h-1Fh	Reserved.

Following is an example of the Block Write-Block Read Process Call. The Block Write-Block Read Process Call is a two-part message. It begins with a salve address and a write condition. After the command code the host issues a write count M that describes how many more bytes will be written in the first part of the message. The second part of the message is a block of read data beginning with a repeated start condition followed by thee salve address and a Read Bit. The next read byte count N indicates how many more data will be read in the second part of the message. Note that the combined data payload must not exceed 32bytes. Besides, W83791D also provides packet error code (PEC) to insure the accuracy during data transmission.

1	7	1	1	8	1	8	1	8	1	
S	Slave Address	Wr	A	Command Code	A	Byte Count=M	A	Data Byte 1	A	…

8	1	…	8	1	
Data Byte 2	A	…	Data Byte M	A	…

1	7	1	1	8	1	8	1	1
Sr	Slave Address	Rd	A	Byte Count=N	A	Data Byte 1	A	…

8	1	…	8	1	8	1	1
Data Byte 2	A	…	Data Byte N	A	PEC	A	P

6.5 ASF(Alert Standard Format) Introduction

In order to implement network management in OS-absent, W83791D provides ASF Response Registers to meet ASF sensor spec. As a result, the network server is able to monitor several environmental status of the client in OS-absent by PET frame values returned from W83791D, including temperature, voltage, fan speed, and case open. In below is the ASF diagram:

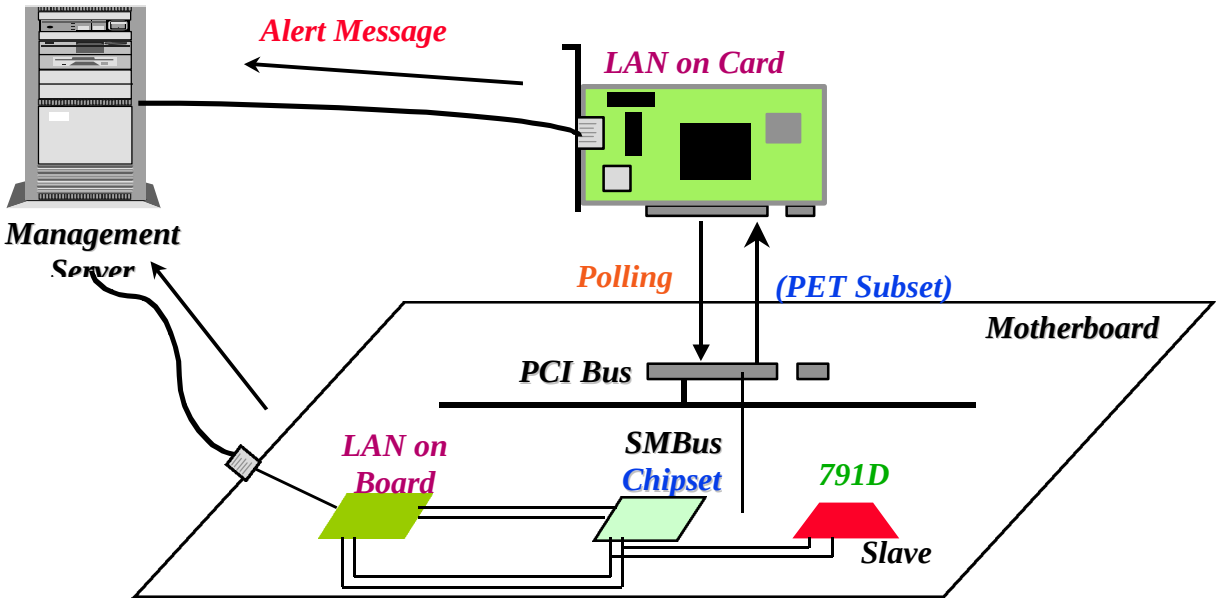


Figure 6. ASF Block Diagram

6.5.1 Platform Event Trap (PET)

PET is the ASF transmit protocol used to provide common fields for trap regardless of trap source. The variable bindings fields in a PET frame contain the system and sensor information for an event, such as event sensor type, event type, event offset, event source type, sensor device, sensor number, entity ID, entity instance, event status index, event status, and event severity. Each field has its definition and is described in the following table.

PET Variable Binding Field	Description
Event Sensor Type	The Event Sensor Type field indicates what types of events the sensor is monitoring. E.g. temperature, voltage, fan, etc.
Event Type	The Event Type indicates what type of transition/state change triggered the trap.
Event Offset	The Event Offset indicates which particular event occurred for a given Even Type.
Event source Type	The Event Source Type describes the originator of the event. It is ASF1.0(68h) for all PET frames defined by this specification.
Sensor Device	The Sensor Device is the SMBus address of the sensor that caused the event for the PET frame.
Sensor Number	The Sensor Number is used to identify a given instance of a sensor relative to the Sensor Device.
Entity ID	The Entity ID indicates the platform entity the event is associated with. E.g. processor, system board, etc.
Entity Instance	The Entity Instance indicates which instance of the Entity the event is for. E.g. processor 1 or processor 2.
Event Status Index	The Event Status Index identifies a unique event monitored by the ASF-sensor. It is zero-based, sequential, continuous, and ranging form 0-37h.
Event Status	The Event Status indicates the event state of the ASF-sensor device associated with the message's Event Status Index.
Event Severity	The Event Severity gives the management station an indication of the severity of the event in the PET frame. Typical values are Monitor (0x01), Non Critical (0x08), or Critical Condition (0x10).

Following is the illustration of ASF SMBus command for Get Event Data.

1	7	1	1	8	1	8	1	
S	Slave Address	Wr	A	Command	A	Wr Byte Count	A	…
	ASF-sensor Address	0	0	Sensor Device 0000 0001	0	0000 0100	0	

8	1	8	1	8	1	8	1	
Wr Data 1	A	Wr Data 2	A	Wr Data 3	A	Wr Data 4	A	…
Sub Command Get Event Data 0001 0001	0	Version Number 0001 0000	0	Event Status Index 00ii iiii	0	Reserved 0000 0000	0	

1	7	1	1	8	1	
Sr	Slave Address	R	A	Rd Byte Count	A	…
	ASF-sensor Address	1	0	0000 1010 to 0000 1111	0	

1	8	1	8	1	8	1	
A	Rd Data 1	A	Rd Data 2	A	Rd Data 3	A	…
0	Status	0	Event Sensor Type	0	Event Type	0	

8	1	8	1	8	1	8	1	
Rd Data 4	A	Rd Data 5	A	Rd Data 6	A	Rd Data 7	A	…
Event Offset	0	Event Source Type	0	Event Severity	0	Sensor Device	0	

8	1	8	1	8	1	
Rd Data 8	A	Rd Data 9	A	Rd Data 10	A	…
Sensor Number	0	Entity	0	Entity Instance	0	

	8	1	1
…	PEC	A	P
From zero to five bytes of Event Data	[data dependent]	1	

6.6 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Actually, the application of the PC monitoring would most often be connected to power supply. The CPU V-core voltage,+3.3V and battery voltage can directly connect to these analog inputs. The –5V, –12V and +12V inputs should be reduced a factor with external resistors to meet the input range. As Figure 7 shows.

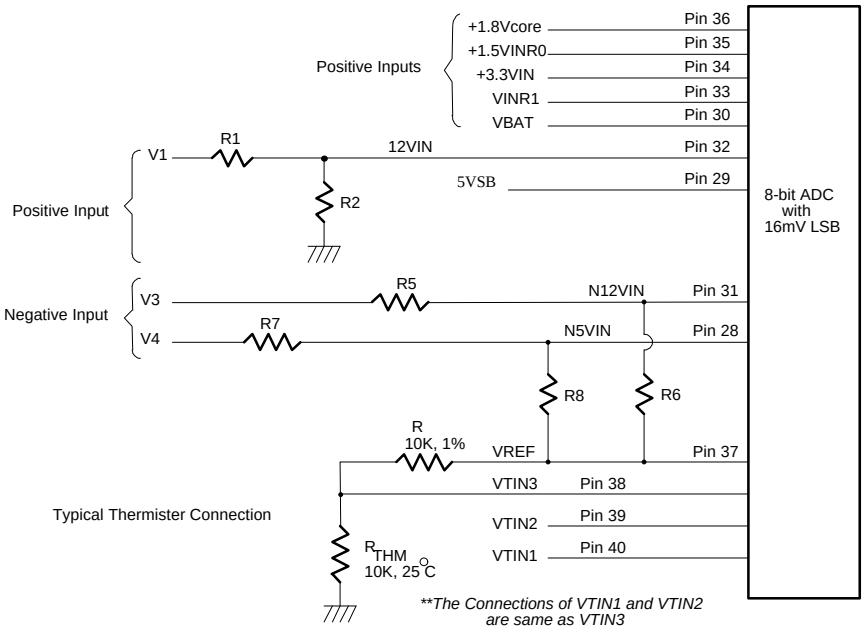


Figure 7.

6.6.1 Monitor over 4.096V voltage:

The input voltage +12VIN can be expressed as the following equation.

$$12VIN = V_1 \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 28K Ohms and 10K Ohms, respectively, when the input voltage V1 is 12V. The node voltage of +12VIN should be subject to under 4.096V for the maximum input range of the 8-bit ADC. The pin 13 and pin 29 are discretely connected to the power supply +5V and 5VSB . There are two functions in these pins with 5V. The first function is to supply internal analog power in the W83791D and the second one is that these voltages are all connected to internal serial resistors to monitor the +5V and 5VSB voltage.

6.6.2 Monitor negative voltage:

The negative voltage should be connected to two series resistors and a positive voltage VREF (equal to 3.6V). In the Figure 11, the voltage V3 and V4 are two negative voltages and are -12V and -5V respectively. The voltage V3 is connected to two serial resistors as well as another positive terminal VREF. Therefore, the voltage node N12VIN would be a positive voltage if the scale of the two serial resistors are carefully selected. It is recommended from Winbond that the scale of the two serial resistors are R5=232K ohms and R6=56K ohm. The input voltage of node -12VIN can be calculated by the following equation.

$$N12VIN = (VREF + |V_5|) \times (\frac{232K\Omega}{232K\Omega + 56K\Omega}) + V_5$$

where VREF is equal to 3.6V.

If the V_5 is equal to -12V then the voltage is equal to 0.567V and the converted hexdecimal data is set to 35h by the 8-bit ADC with 16mV-LSB.This monitored value should be converted to the real negative voltage and the express equation is shown as follows.

$$V_5 = \frac{N12VIN - VREF \times b}{1 - b}$$

Where b is 232K/(232K+56K). If the N2VIN is 0.567 then the V5 is approximately equal to -12V.

The other negative voltage input V6 (approximate -5V) can also be evaluated by the similar method and the serial resistors can be R7=120K ohms and R8=56K ohms by the Winbond recommended. The expression equation of V6 With -5V voltage is shown as follows.

$$V_6 = \frac{N5VIN - VREF \times g}{1 - g}$$

Where the b is set to 120K/(120K+56K). If the monitored ADC value in the N5VIN channel is 0.8635, VREF=3.6V and the parameter b is 0.6818, then the negative voltage of V6 can be evaluated -5V.

6.7 FAN Speed Count and FAN Speed Control

6.7.1 Fan speed count

W83791D support 5 sets of fan counting. Fan inputs are provided for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and the maximum input voltage should not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to meet the input specification. The normal circuit and trimming circuits are shown as Figure 8.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, if the fan speed counter has been read from register CR[28] or CR[29] or CR[2A] or CR[BA] or CR[BB] , then the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR47.bit7~4, CR4B.bit7~6, and Bank0 CR5D.bit5~7 which are three bits for divisor. This provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, RPM, and count.

Divisor	Nominal RPM	Time per Revolution	Counts	70% RPM	Time for 70%
1	8800	6.82 ms	153	6160	9.74 ms
2 (default)	4400	13.64 ms	153	3080	19.48 ms
4	2200	27.27 ms	153	1540	38.96 ms
8	1100	54.54 ms	153	770	77.92 ms
16	550	109.08 ms	153	385	155.84 ms
32	275	218.16 ms	153	192	311.68 ms
64	137	436.32 ms	153	96	623.36 ms
128	68	872.64 ms	153	48	1246.72 ms

Table 2.

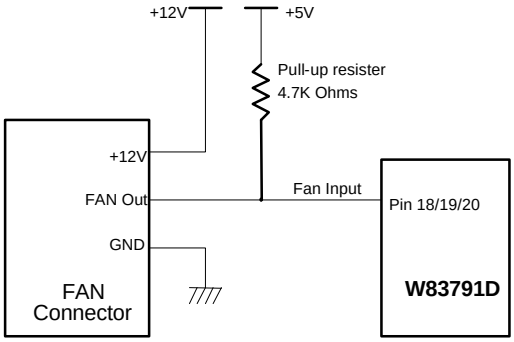


Figure 8-1. Fan with Tach Pull-Up to +5V

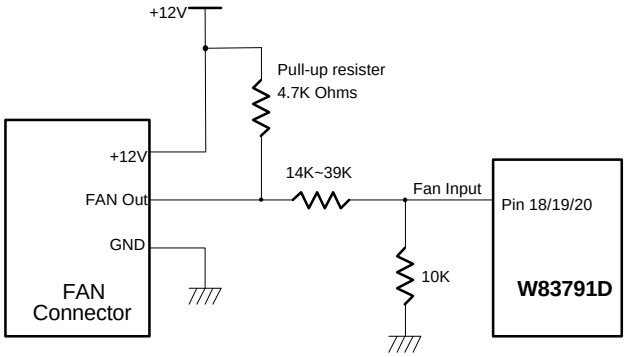


Figure 8-2. Fan with Tach Pull-Up to +12V, or Totem-Pole Output and Register Attenuator

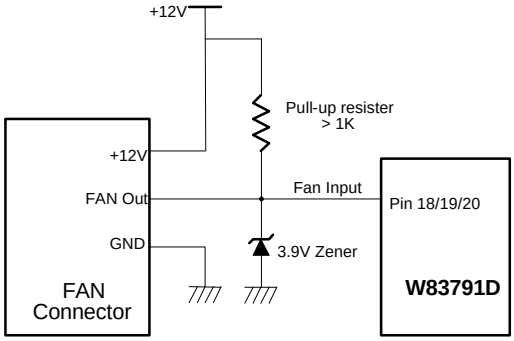


Figure 8-3. Fan with Tach Pull-Up to +12V and Zener Clamp

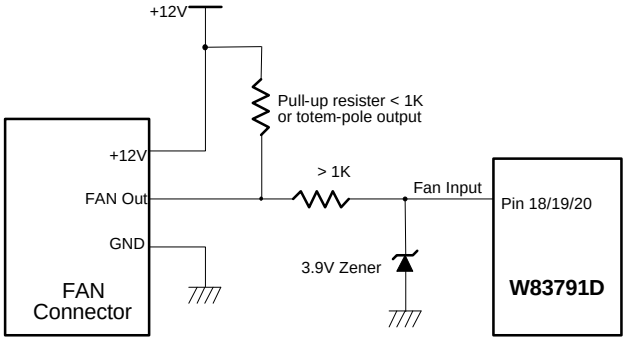


Figure 8-4. Fan with Tach Pull-Up to +12V, or Totem-Pole Putput and Zener Clamp

6.7.2 Fan speed control

The W83791D provides five sets of PWM for fan speed control. The duty cycle of PWM can be programmed by a 8-bit registers defined in the Bank0 CR[81], CR[83], CR[94], CR[9E] and CR[9F] . The default duty cycle is set to 100%, that is, the default 8-bit register is set to 0xFFh. The expression of duty cycle can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

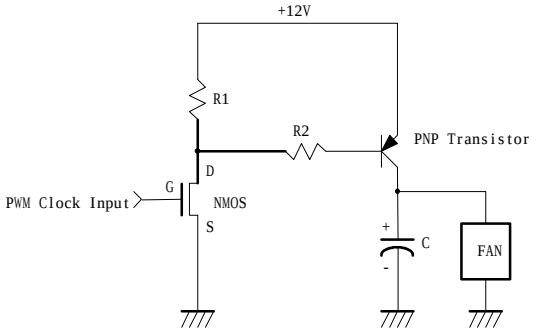


Figure 9.

6.7.3 Smart Fan Control

W83791D supports three Smart Fan function and mapping to temp1 (FAN1, PWMOUT1), temp2 (FAN2, PWMOUT2) , temp3(FAN3, PWMOUT3) .Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode.

6.7.3.1 Thermal Cruise mode

At this mode, W83791D provides the Smart Fan system to automatically control fan speed to keep the temperatures of CPU and the system within specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS and the fan speed will be lowered as long as the current temperature remains below the setting value. Once the temperature exceeds the high limit (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur :

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its full speed but the temperature still exceeds the high limit (ex: 58°C), a warning message will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but still above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target range (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset stop value until the temperature exceeds the low limit.

Figure 10-1, 10-2 gives an illustration of Thermal Cruise Mode.

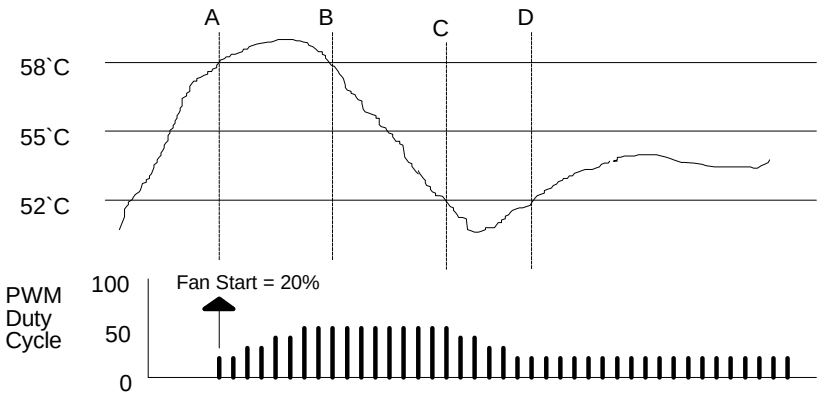


Figure 10-1.

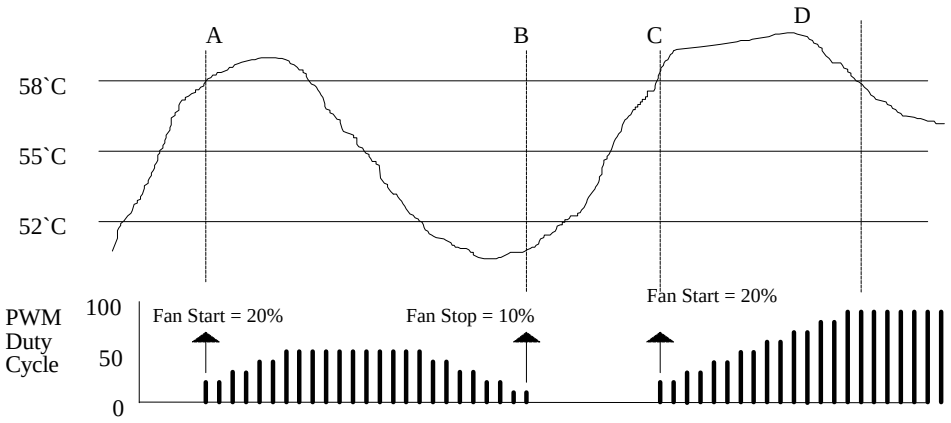


Figure 10-2.

6.7.3.2 Fan Speed Cruise mode

At this mode, W83791D provides the Smart Fan system to automatically control the fan speed within a specific range. In the beginning, a wanted fan speed count and interval must be set (ex. 160± 10) by BIOS. As long as the fan speed count remains in the specific range, PWM duty cycle will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), PWM duty cycle will be increased to make the count under the high limit. On the other hand, if current fan speed count is less than the low limit(ex. 160-10), PWM duty cycle will be decreased to make the count higher than the low limit. See Figure 10-3 example.

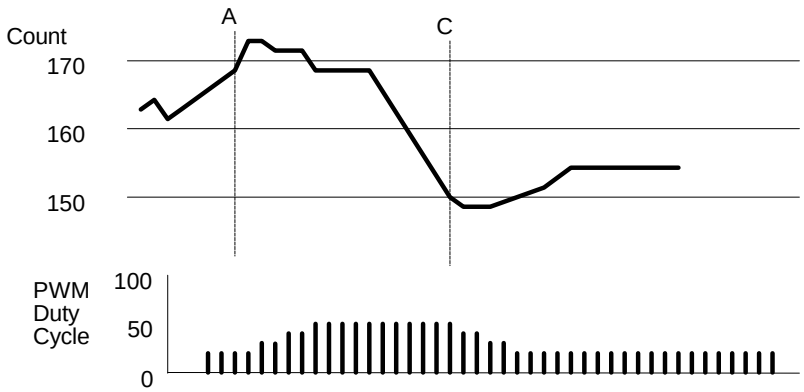


Figure 10-3.

Of course, Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

6.8 Temperature Measurement Machine

The temperature data format is 8-bit two-complement for sensor 1 and 9-bit two-complement for sensor 2/3. The 8-bit temperature data can be obtained by reading the CR[27h]. The 9-bit temperature data can be obtained by reading the 8 MSBs from the bank0 CR[C0/ C8h] and the LSB from the bank0 CR[C1/C9h] bit 7. The format of the temperature data is show in Table 3.

Temperature	8-Bit Digital Output		9-Bit Digital Output	
	8-Bit Binary	8-Bit Hex	9-Bit Binary	9-Bit Hex
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

Table 3.

6.8.1 Monitor temperature from thermistor:

The W83791D can connect three thermistors to measure three different environmental temperatures. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 11, the themistor is connected by a serial resistor with 10K Ohms(1% error), then connect to VREF (Pin 37).

6.8.2 Monitor temperature from Pentium II™ thermal diode or bipolar transistor 2N3904

The W83791D can alternate the thermistor to Pentium II/III™ thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 11. The pin of Pentium II/III™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin PIITDx in the W83791D. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

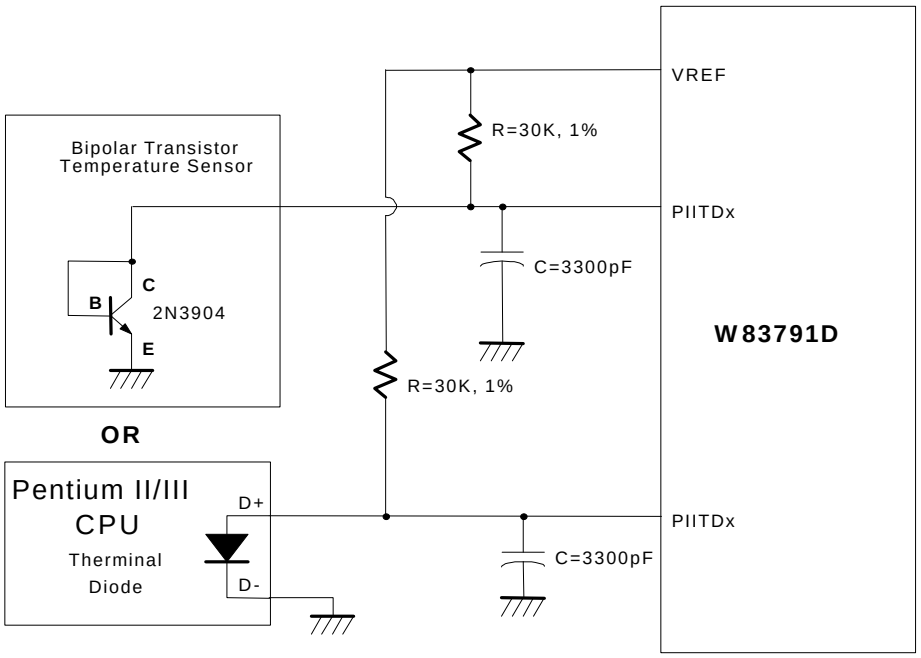


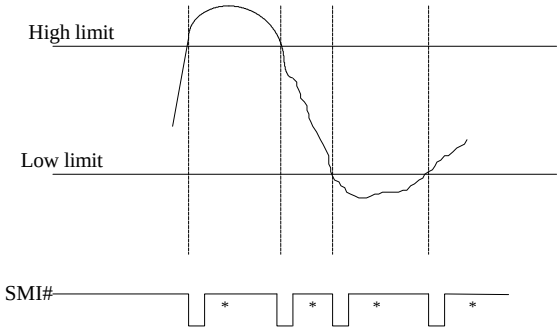
Figure 11.

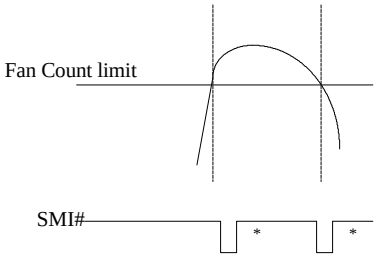
6.8.3 SMI# interrupt for W83791D Voltage

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 12-1.)

6.8.4 SMI# interrupt for W83791D Fan

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit (set at value ram index 3Bh and 3Ch) , will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 12-2.)





*Interrupt Reset when Interrupt Status Registers are read

Figure 12-1. Voltage SMI# Mode

Figure 12-2. Fan SMI# Mode

6.8.5 SMI# interrupt for W83791D temperature sensor 1/2/3

(1) Comparator Interrupt Mode

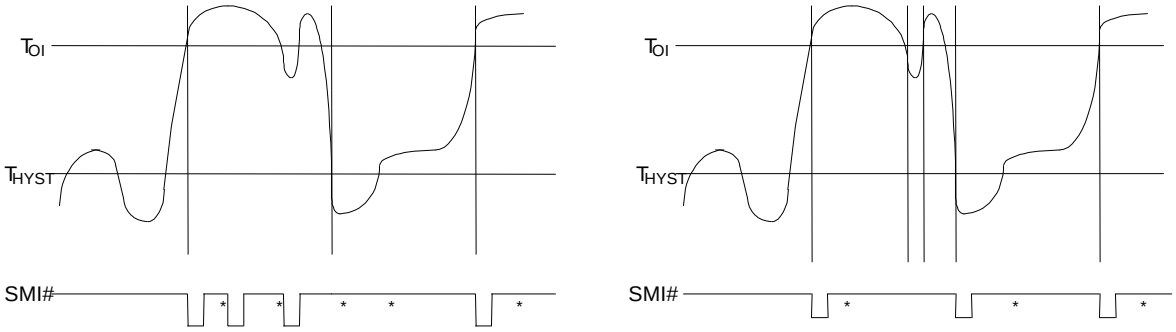
Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O but has not been reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 12-3.)

(2) Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O , then reset, if the temperature remains above the T_{HYST} , the interrupt will not occur. (Figure 12-4.)

(3) One-Time interrupt mode

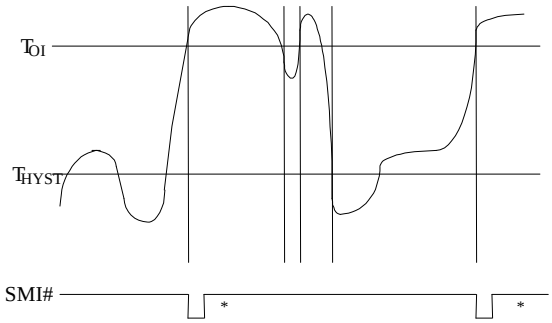
Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below $T_{HYST,}$ an interrupt will not occur again until the temperature exceeding T_O. (Figure 12-5.)



*Interrupt Reset when Interrupt Status Registers are read

Figure 12-3. Comparator Interrupt Mode

Figure 12-4. Two-Times Interrupt Mode



*Interrupt Reset when Interrupt Status Registers are read

Figure 12-5. One-Time Interrupt Mode

Note. The IRQ interrupt action like SMI# , but the IRQ is level signal.

6.8.6 Over-Temperature (OVT#) for W83791D temperature sensor 1/2/3

(1) Comparator Mode:

Temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 13)

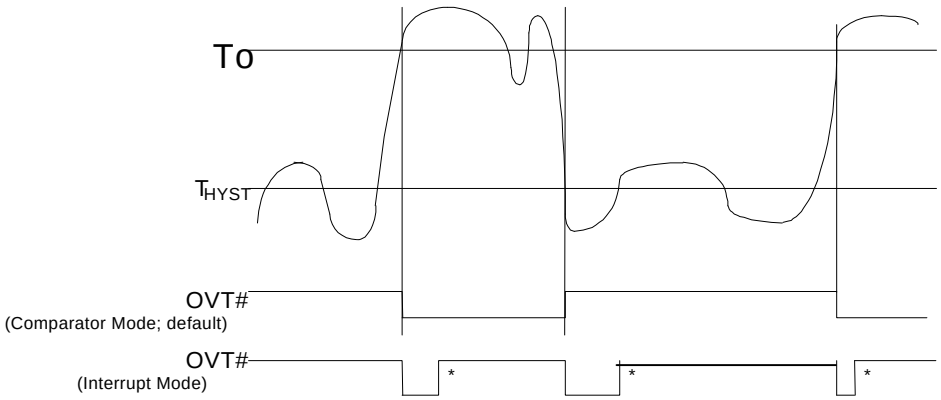
(2) Interrupt Mode:

Temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading temperature sensor 1 or sensor 2 or sensor 3 registers. Temperature exceeding T_O, then OVT# reset, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor 1 or sensor 2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again.(Figure 13)

(3) ACPI Mode

At this mode, temperature exceeding one level of temperature separation, starting from 0 degree, causes the OVT# output activated. OVT# will be activated again once temperature exceeds the next level. OVT# output will act the same manner when temperature goes down. (Figure 13-1).

The granularity of temperature separation between each OVT# output signal can be programmed at Bank0 CR[4Ch] bit 4-5.



*Interrupt Reset when Temperature 1/2/3 is read

Figure 13 Over-Temperature Response Diagram

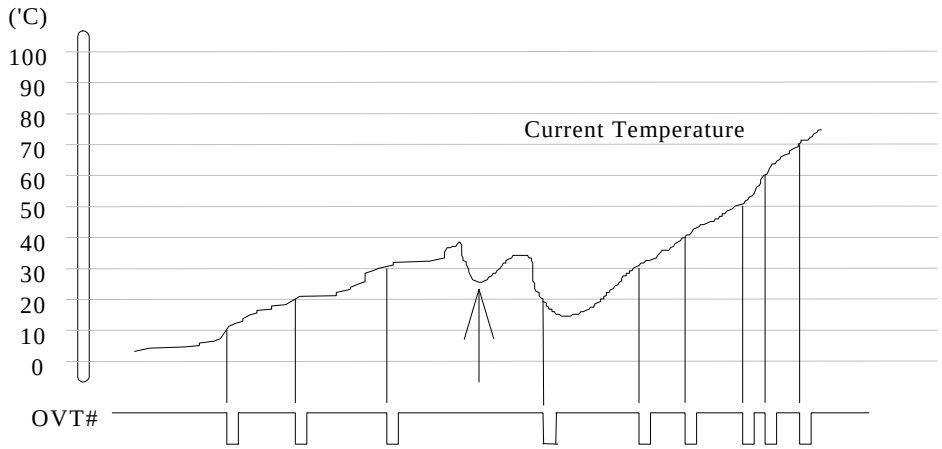


Figure 13-1. ACPI Mode

8 ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.5 to 7.0	V
Input Voltage	-0.5 to V_{DD}+0.5	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to +150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9.2 DC Characteristics

(Ta = 0° C to 70° C, V_{DD} = 5V ± 10%, V_{SS} = 0V)

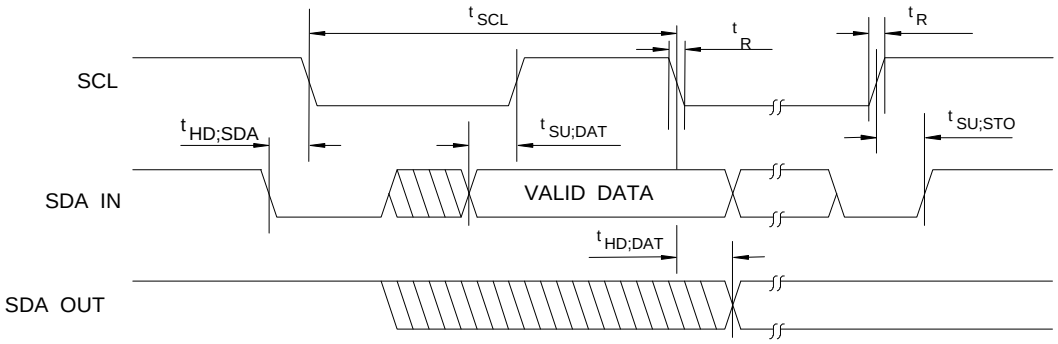
PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I/O_{12t} - TTL level bi-directional pin with source-sink capability of 12 mA						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V
I/O_{12ts} - TTL level bi-directional pin with source-sink capability of 12 mA and schmitt-trigger level input						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = - 12 mA
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0V

7.2 DC Characteristics, continued

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
OUT_{12t} - TTL level output pin with source-sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -12 mA
OD_8 - Open-drain output pin with sink capability of 8 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 8 mA
OD_{12} - Open-drain output pin with sink capability of 12 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 12 mA
OD_{48} - Open-drain output pin with sink capability of 48 mA						
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 48 mA
IN_t - TTL level input pin						
Input Low Voltage	V_{IL}			0.8	V	
Input High Voltage	V_{IH}	2.0			V	
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V
IN_{ts} - TTL level Schmitt-triggered input pin						
Input Low Threshold Voltage	V_{t-}	0.5	0.8	1.1	V	V_{DD} = 5 V
Input High Threshold Voltage	V_{t+}	1.6	2.0	2.4	V	V_{DD} = 5 V
Hysteresis	V_{TH}	0.5	1.2		V	V_{DD} = 5 V
Input High Leakage	I_{LIH}			+10	µA	V_{IN} = V_{DD}
Input Low Leakage	I_{LIL}			-10	µA	V_{IN} = 0 V

9.3 AC Characteristics

9.3.1 Serial Bus Timing Diagram



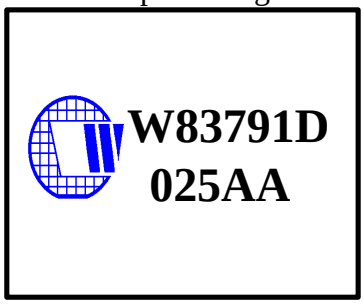
Serial Bus Timing Diagram

Serial Bus Timing

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
SCL clock period	t_{SCL}	10		uS
Start condition hold time	$t_{HD;SDA}$	4.7		uS
Stop condition setup-up time	$t_{SU;STO}$	4.7		uS
DATA to SCL setup time	$t_{SU;DAT}$	120		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
SCL and SDA rise time	t_R		1.0	uS
SCL and SDA fall time	t_F		300	nS

10 HOW TO READ THE TOP MARKING

The top marking of W83791D

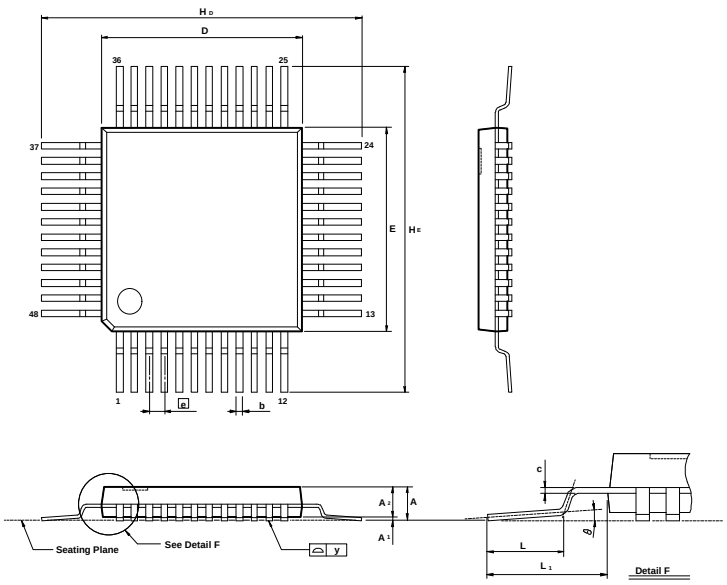


Left: Winbond logo
1st line: Type number W83791D, D means LQFP (Thickness = 1.4 mm).
2nd line: Tracking code 025 A A

025: packages made in 2000, week 25
A: assembly house ID; A means ASE, O means OSE
A: IC revision; A means version A, B means version B

11 PACKAGE SPECIFICATION

(48-pin QFP)



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A				---	---	1.60
A_1				0.05	---	0.15
A_2				1.35	1.40	1.45
b				0.17	0.20	0.27
c				0.09	---	0.20
D					7.00	
E					7.00	
e					0.50	
H_D					9.00	
H_E					9.00	
L				0.45	0.60	0.75
L_1					1.00	
y				---	0.08	---
θ				0	3.5°	7

Notes:

1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

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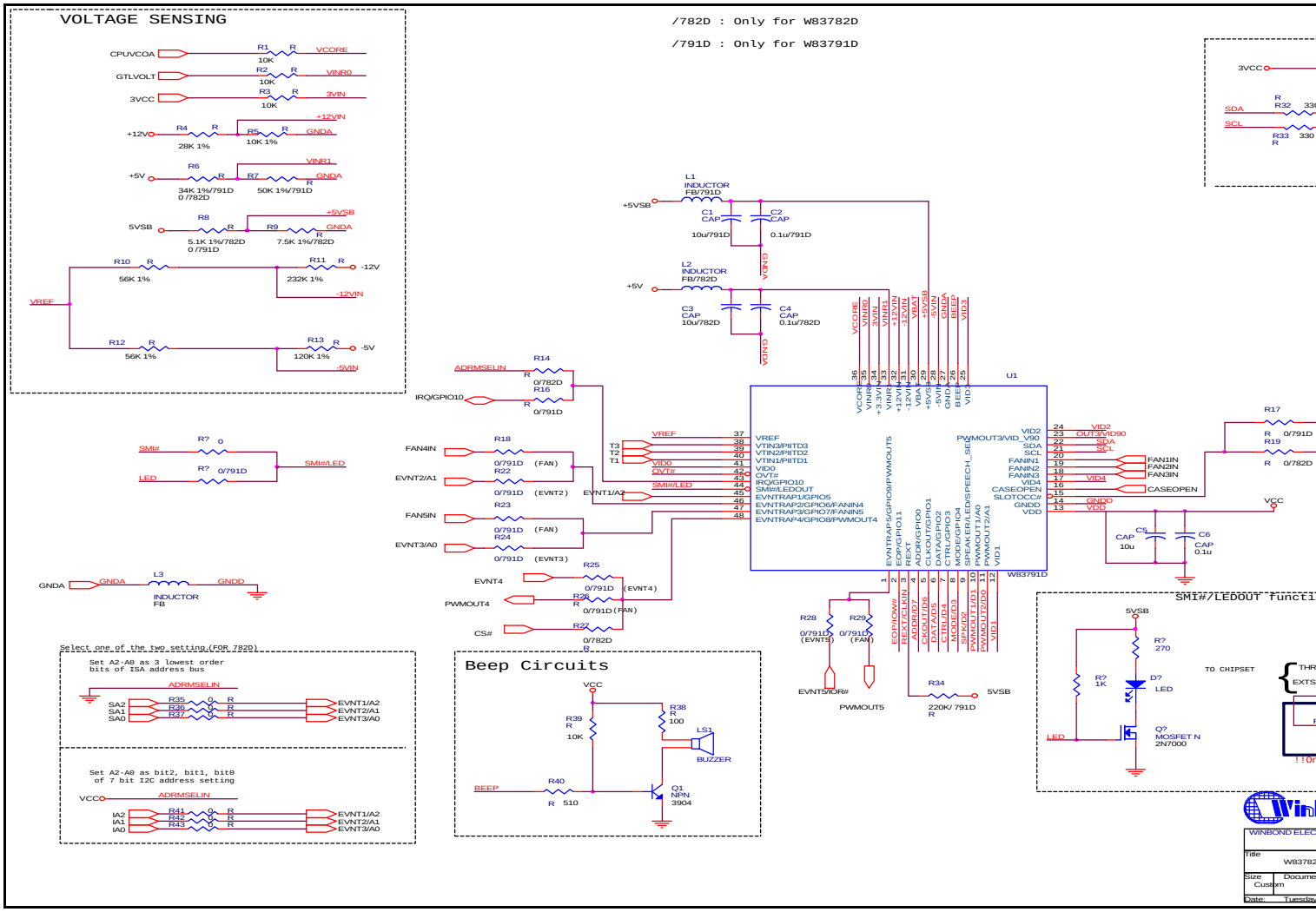
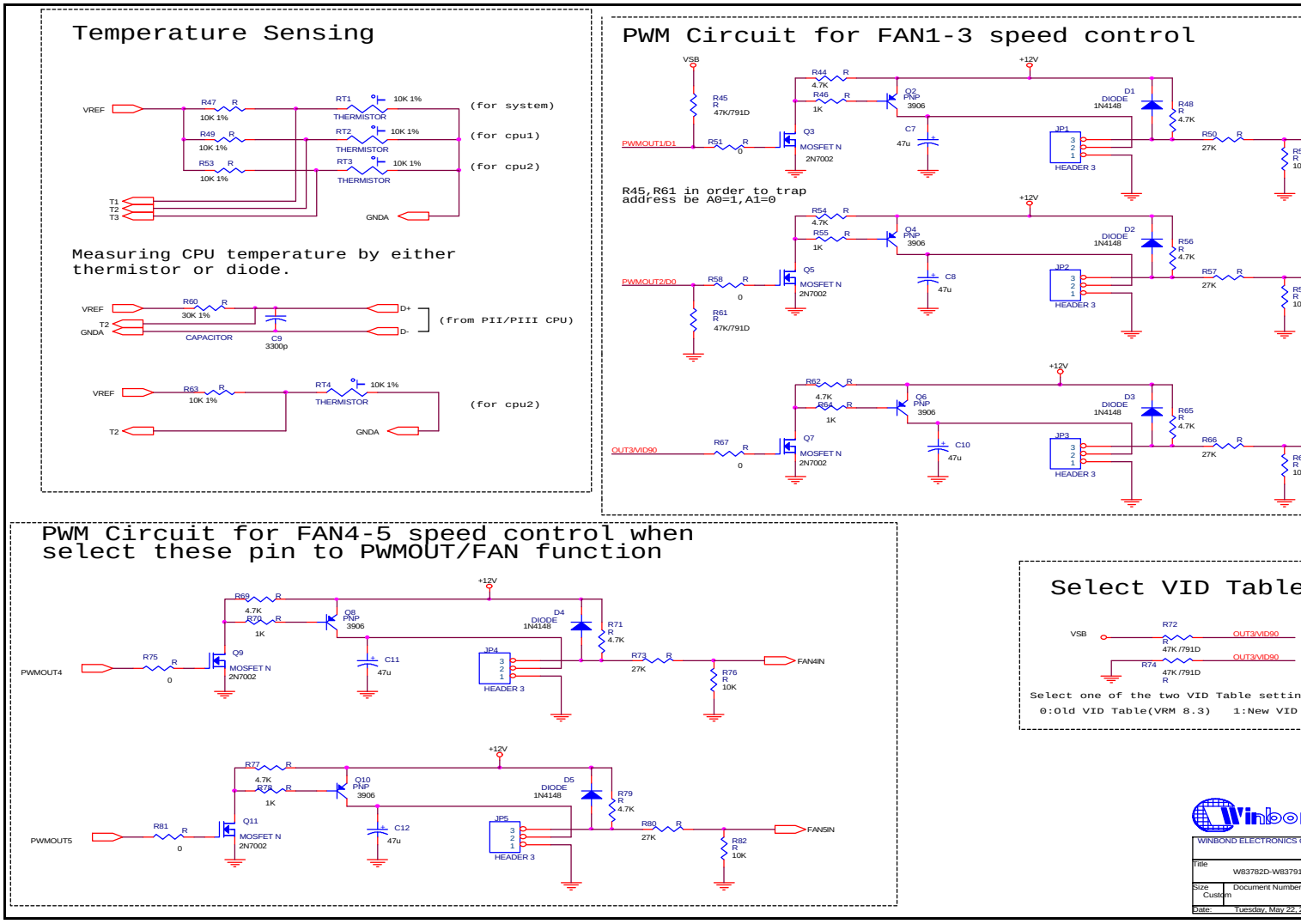
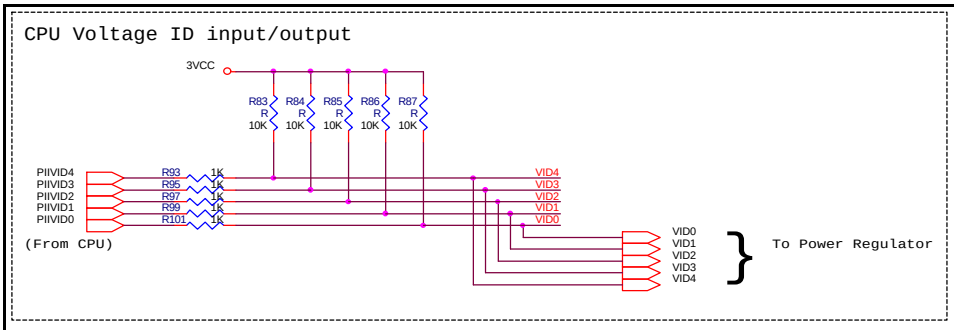
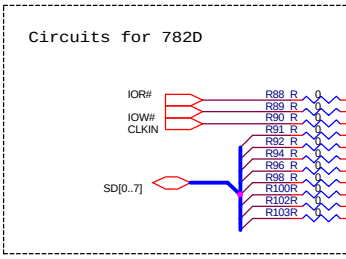
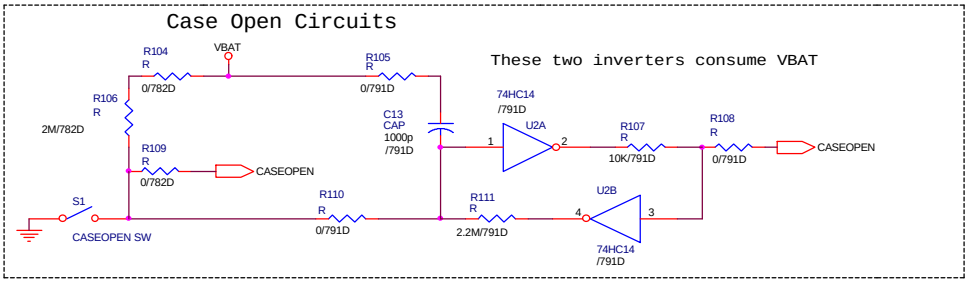

VOLTAGE SENSING
/782D : Only for W83782D
/791D : Only for W83791D
Beep Circuits
SMI#/LEDOUT functi
W83791D
U1
TO CHIPSET


Temperature Sensing
VREF
R47 R 10K 1%
RT1 THERMISTOR 10K 1%
(for system)
R49 R 10K 1%
RT2 THERMISTOR 10K 1%
(for cpu1)
R53 R 10K 1%
RT3 THERMISTOR 10K 1%
(for cpu2)
T1
T2
T3
GNDA
Measuring CPU temperature by either thermistor or diode.
VREF
T2
GNDA
R60 R 30K 1%
CAPACITOR
C9 3300p
D+
D-
(from PII/PIII CPU)
VREF
R63 R 10K 1%
RT4 THERMISTOR 10K 1%
T2
GNDA
(for cpu2)
PWM Circuit for FAN1-3 speed control
VSB
+12V
R45 R 47K/791D
R44 R 4.7K
R46 R 1K
Q2 PNP 3906
D1 DIODE 1N4148
R48 R 4.7K
PWMOUT1/D1
R51 R 0
Q3 MOSFET N 2N7002
C7 47u
JP1 HEADER 3
R50 R 27K
R45,R61 in order to trap address be A0=1,A1=0
R54 R 4.7K
R55 R 1K
Q4 PNP 3906
D2 DIODE 1N4148
R56 R 4.7K
PWMOUT2/D0
R58 R 0
Q5 MOSFET N 2N7002
C8 47u
JP2 HEADER 3
R57 R 27K
R61 R 47K/791D
R62 R 4.7K
R64 R 1K
Q6 PNP 3906
D3 DIODE 1N4148
R65 R 4.7K
OUT3/VID90
R67 R 0
Q7 MOSFET N 2N7002
C10 47u
JP3 HEADER 3
R66 R 27K
PWM Circuit for FAN4-5 speed control when select these pin to PWMOUT/FAN function
+12V
R68 R 4.7K
R70 R 1K
Q8 PNP 3906
D4 DIODE 1N4148
R71 R 4.7K
PWMOUT4
R75 R 0
Q9 MOSFET N 2N7002
C11 47u
JP4 HEADER 3
R73 R 27K
R76 R 10K
FAN4IN
R77 R 4.7K
R78 R 1K
Q10 PNP 3906
D5 DIODE 1N4148
R79 R 4.7K
PWMOUT5
R81 R 0
Q11 MOSFET N 2N7002
C12 47u
JP5 HEADER 3
R80 R 27K
R82 R 10K
FAN5IN
Select VID Table
VSB
R72 R 47K /791D
OUT3/VID90
R74 R 47K /791D
OUT3/VID90
Select one of the two VID Table settin
0:Old VID Table(VRM 8.3) 1:New VID
WINBOND ELECTRONICS
Title
W83782D-W83791
Size Custom
Document Number
Date: Tuesday, May 22,







WINBOND ELECTRONICS

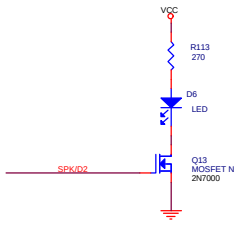
Title W83782D-W83791D A

Size B | Document Number

Date: Tuesday, May 22, 2

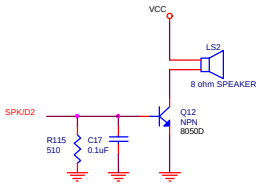
Select SPEECH / LED Function by one of three cricuits. / 791D

1.



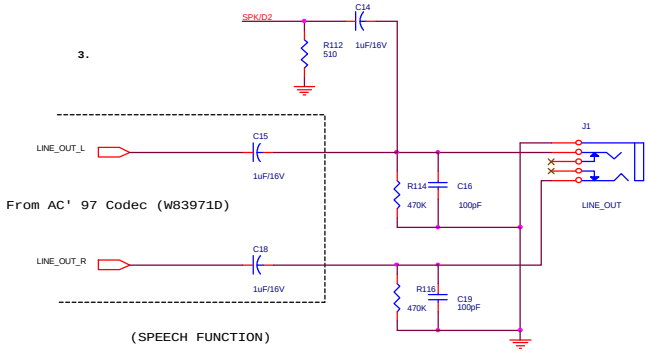
(LED FUNCTION)

2.



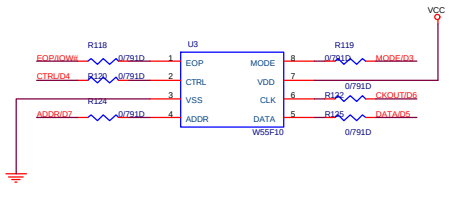
(SPEECH FUNCTION)

3.

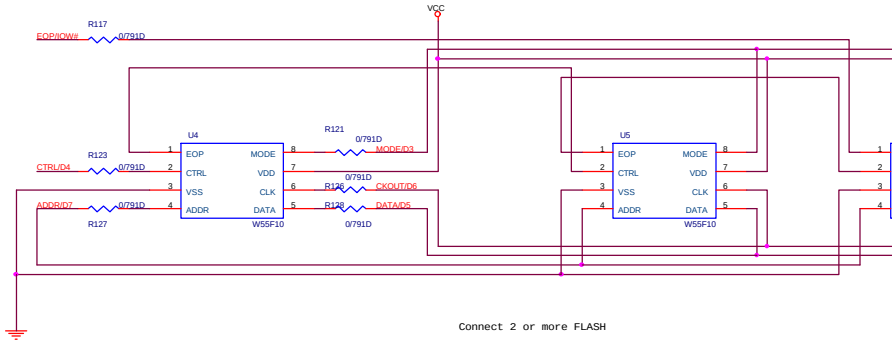


(SPEECH FUNCTION)

Connect to serial FLASH EEPROM (W55FXX) /791D



Connect 1 FLASH



Connect 2 or more FLASH

Publication Release Date: Aug, 2001

REV	Decription
0.1	First Publication
0.15	Add FAN/PWMOUT4-5 circuit
0.16	Change R34 connect to 5VSB
0.17	1. Change R32/R33 value to 330 ohm 2. Modify R34 value as 220K ohm 3. Change SMI# (pin 44) circuit. This update is for B version.
0.2	Update Pin44 (SMI#/LEDOUT) circuit. This update is for C version.

WINBOND ELECTRONICS CORP.

Title: W83782D-W83791D Application circuit

Size: A | Document Number:

Date: Tuesday, May 22, 2001 | She