WINBOND
LPC SUPER I/O
W83L517D

W83L517D Data Sheet Revision History

	Pages	Dates (mm/yy)	Version	Version on Web	Main Contents
1	n.a.	Apr./00	0.50		Not released
2	5	Feb./01	0.60		Content of SERIRQ
3	13	Feb./01	0.60		I/O attributes of KBCS# and MCCS#
4	108	Feb./01	0.60		CR23 Bit6 Description
5	111	Feb./01	0.60		CR2A Default value
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

TABLE OF CONTENTS

GENERAL DESCRIPTION

The W83L517D is evolving product from Winbond's most popular I/O family. They feature a whole new interface, namely LPC (**Low Pin Count**) interface, which will be supported in the new generation chip-set. This interface as its name suggests is to provide an economical implementation of I/O's interface with lower pin count and still maintains equivalent performance as its ISA interface counterpart. Approximately 40 pin counts are saved in LPC I/O comparing to ISA implementation. With this additional freedom, we can implement more devices on a single chip as demonstrated in W83L517D's integration of Flash ROM Interface. It is fully transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

The disk drive adapter functions of W83L517D include a floppy disk drive controller compatible with the industry standard 82077/ 765, data separator, write pre-compensation circuit, decode logic, data rate selection, clock generator, drive interface control logic, and interrupt and DMA logic. The wide range of functions integrated onto the W83L517D greatly reduces the number of components required for interfacing with floppy disk drives. The W83L517D supports four 360K, 720K, 1.2M, 1.44M, or 2.88M disk drives and data transfer rates of 250 Kb/s, 300 Kb/s, 500 Kb/s,1 Mb/s, and 2 Mb/s.

The W83L517D provides one high-speed serial communication ports (UARTs), one of which supports serial Infrared communication. The UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability, and a processor interrupt system. The UART provides legacy speed with baud rate up to 115.2k bps and also advanced speed with baud rates of **230k**, **460k**, or **921k bps** which support higher speed modems. In addition, the W83L517D provides IR functions: **IrDA 1.0** (**SIR** for 1.152K bps) and IrDA 1.1 (MIR for 1.152M bps or FIR for 4M bps), TV remote IR, (**Consumer IR**, supporting NEC, RC-5, extended RC-5, and RECS-80 protocols).

The W83L517D supports one PC-compatible printer port (SPP), Bi-directional Printer port (BPP) and also Enhanced Parallel Port (EPP) and Extended Capabilities Port (ECP). Through the printer port interface pins, also available are: Extension FDD Mode and Extension 2FDD Mode allowing one or two external floppy disk drives to be connected.

The configuration registers support mode selection, function enable/disable, and power down function selection. Furthermore, the configurable PnP features are compatible with the plug-and-play feature demand of Windows 95/98™, which makes system resource allocation more efficient than ever.

The W83L517D provides a set of flexible I/O control functions to the system designer through a set of General Purpose I/O ports. These GPIO ports may serve as simple I/O or may be individually configured to provide a predefined alternate function. General Purpose Port 1 is designed to be functional even in power down mode (VCC is off).

The W83L517D is made to fully comply with Microsoft© PC98 and PC99 Hardware Design Guide, and meet the requirements of ACPI.

The W83L517D provides two important interfaces -- “Flash ROM interface and ISA keyboard controller interface”. The Flash ROM interface can support up to 4M legacy flash ROM. The ISA KBC interface can supports legacy KBC such as Mitsubishi H8 and Intel 8xC51.

FEATURES

General

Meet LPC Spec. 1.01

Support LDRQ#(LPC DMA), SERIRQ (serial IRQ)

Include all the features of Winbond I/O W83877ATF

Compliant with Microsoft PC98/PC99 Hardware Design Guide

Support DPM (Device Power Management), ACPI

Support hardware power down mode

Support printer port/floppy hardware auto-detect and auto-swap

Programmable configuration settings

Single 24 or 48 MHz clock input

FDC

Compatible with IBM PC AT disk drive systems

Variable write pre-compensation with track selectable capability

Support vertical recording format

DMA enable logic

16-byte data FIFOs

Support floppy disk drives and tape drives

Detects all overrun and underrun conditions

Built-in address mark detection circuit to simplify the read electronics

FDD anti-virus functions with software write protect and FDD write enable signal (write data signal was forced to be inactive)

Support up to four 3.5-inch or 5.25-inch floppy disk drives

Completely compatible with industry standard 82077

360K/720K/1.2M/1.44M/2.88M format; 250K, 300K, 500K, 1M, 2M bps data transfer rate

Support **3-mode FDD, and its Win95/98 driver**

UART

High-speed 16550 compatible UARTs with 16-byte send/receive FIFOs

MIDI compatible

Fully programmable serial-interface characteristics:

--- 5, 6, 7 or 8-bit characters

--- Even, odd or no parity bit generation/detection

--- 1, 1.5 or 2 stop bits generation

Internal diagnostic capabilities:

--- Loop-back controls for communications link fault isolation

UART

--- Break, parity, overrun, framing error simulation

Programmable baud generator allows division of 1.8461 MHz and 24 MHz by 1 to (2^{16}-1)

Maximum baud rate up to **921k bps** for 14.769 MHz and 1.5M bps for 24 Mhz

Infrared

Support IrDA version 1.0 SIR protocol with maximum baud rate up to 115.2K bps

Support SHARP ASK-IR protocol with maximum baud rate up to 57,600 bps

Support IrDA version 1.1 MIR (1.152M bps) and FIR (4M bps) protocol

--- Single DMA channel for transmitter or receiver

--- 32-byte FIFO is supported in both FIR TX/RX transmission

--- 8-byte status FIFO is supported to store received frame status (such as overrun, CRC error, etc.)

Support auto-config SIR and FIR

Support full Customer IR

Support driver for Microsoft™ Windows 95™ and Windows 98™ (Memphis ™)

Parallel Port

Compatible with IBM™ parallel port

Support PS/2 compatible bi-directional parallel port

Support Enhanced Parallel Port (EPP) – Compatible with IEEE 1284 specification

Support Extended Capabilities Port (ECP) – Compatible with IEEE 1284 specification

Extension FDD mode supports disk drive B; and Extension 2FDD mode supports disk drives A and B through parallel port

Enhanced printer port back-drive current protection

Flash ROM Interface

Support up to 4M flash ROM

Keyboard Controller Interface

Support Legacy ISA keyboard controller

General Purpose I/O Ports

38 programmable general purpose I/O ports

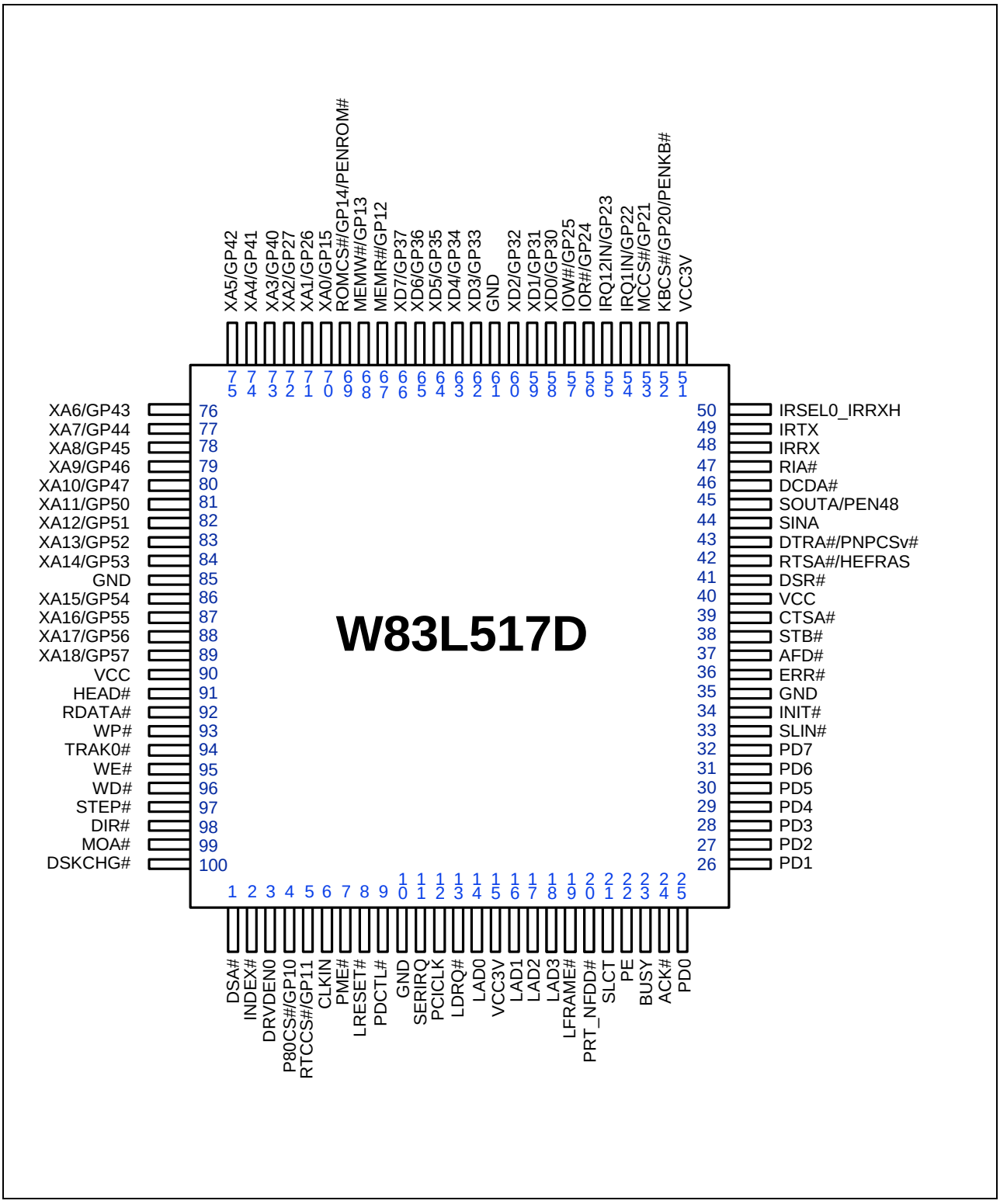
General purpose I/O ports can serve as simple I/O ports, watch dog timer output, power LED output, infrared I/O pins, suspend LED output, Beep output

Functional in power down mode

Package

100-pin LQFP

PIN CONFIGURATION For W83L517D



1. PIN DESCRIPTION

Note: Please refer to Section 13.2 DC CHARACTERISTICS for details.

I/O_{8t} - TTL level bi-directional pin with 8 mA source-sink capability

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12tp3} - 3.3V TTL level bi-directional pin with 12 mA source-sink capability

I/OD_{12t} - TTL level bi-directional pin open drain output with 12 mA sink capability

I/O_{24t} - TTL level bi-directional pin with 24 mA source-sink capability

OUT_{12t} - TTL level output pin with 12 mA source-sink capability

OUT_{12tp3} - 3.3V TTL level output pin with 12 mA source-sink capability

OD_{12} - Open-drain output pin with 12 mA sink capability

OD_{24} - Open-drain output pin with 24 mA sink capability

IN_{cs} - CMOS level Schmitt-trigger input pin

IN_{t} - TTL level input pin

IN_{td} - TTL level input pin with internal pull down resistor

IN_{ts} - TTL level Schmitt-trigger input pin

IN_{tsp3} - 3.3V TTL level Schmitt-trigger input pin

1.1 LPC Interface

SYMBOL	PIN	I/O	FUNCTION
CLKIN	6	IN_t	System clock input. According to the input frequency 24MHz or 48MHz, it is selectable through register. Default is 24MHz input.
PME#	7	OD_{12}	Generated PME event.
PCICLK	12	IN_{tsp3}	PCI clock input.
LDRQ#	13	O_{12tp3}	Encoded DMA Request signal.
SERIRQ	11	I/OD_{12t}	Serial IRQ input/Output.; Support both Continuous and Quiet modes.
LAD[0:3]	14, 16-18	I/O_{12tp3}	These signal lines communicate address, control, and data information over the LPC bus between a host and a peripheral.
LFRAME#	19	IN_{tsp3}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	8	IN_{tsp3}	Reset signal. It can connect to PCIRST# signal on the host.
PDCTL#	9	IN_{tsp3}	Hardware power down input pin for chip power down. Programmable control by registers.

1.2 FDC Interface

SYMBOL	PIN	I/O	FUNCTION
DRVDEN0	3	OD_{24}	Drive Density Select bit 0.
INDEX#	2	IN_{cs}	This Schmitt-triggered input from the disk drive is active low when the head is positioned over the beginning of a track marked by an index hole. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
DSA#	1	OD_{24}	Drive Select A. When set to 0, this pin enables disk drive A. This is an open drain output.
DSKCHG#	100	IN_{cs}	Diskette change. This signal is active low at power on and whenever the diskette is removed. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
MOA#	99	OD_{24}	Motor A On. When set to 0, this pin enables disk drive 0. This is an open drain output.
DIR#	98	OD_{24}	Direction of the head step motor. An open drain output. Logic 1 = outward motion Logic 0 = inward motion
STEP#	97	OD_{24}	Step output pulses. This active low open drain output produces a pulse to move the head to another track.
WD#	96	OD_{24}	Write data. This logic low open drain writes pre-compensation serial data to the selected FDD. An open drain output.
WE#	95	OD_{24}	Write enable. An open drain output.
TRAK0#	94	IN_{cs}	Track 0. This Schmitt-triggered input from the disk drive is active low when the head is positioned over the outermost track. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
WP#	93	IN_{cs}	Write protected. This active low Schmitt input from the disk drive indicates that the diskette is write-protected. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
RDATA#	92	IN_{cs}	The read data input signal from the FDD. This input pin is pulled up internally by a 1 KΩ resistor. The resistor can be disabled by bit 7 of L0-CRF0 (FIPURDWN).
HEAD#	91	OD_{24}	Head select. This open drain output determines which disk drive head is active. Logic 1 = side 0 Logic 0 = side 1

1.3 Multi-Mode Parallel Port

The following pins have alternate functions, which are controlled by CR28 and L3-CRF0.

SYMBOL	PIN	I/O	FUNCTION
PRT_NFDD#	20	IN_{tsp3}	PRT_NFDD# is the printer Not Floppy signal. It indicated the connected device as Printer or Floppy Disk on printer port. If the default function(Printer mode) is used, it must connect to low level.
SLCT	21	IN_t	PRINTER MODE: An active high input on this pin indicates that the printer is selected. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
(WE2#)		OD_{12}	EXTENSION FDD MODE: WE2# This pin is for Extension FDD B; its function is the same as the WE# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: WE2# This pin is for Extension FDD A and B; its function is the same as the WE# pin of FDC.
PE	22	IN_t	PRINTER MODE: An active high input on this pin indicates that the printer has detected the end of the paper. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(WD2#)		OD_{12}	EXTENSION FDD MODE: WD2# This pin is for Extension FDD B; its function is the same as the WD# pin of FDC.
		OD12	EXTENSION 2FDD MODE: WD2# This pin is for Extension FDD A and B; its function is the same as the WD# pin of FDC.
BUSY	23	IN_t	PRINTER MODE: An active high input indicates that the printer is not ready to receive data. This pin is pulled high internally. Refer to the description of the parallel port for definition of this pin in ECP and EPP mode.
(MOB2#)		OD_{12}	EXTENSION FDD MODE: MOB2# This pin is for Extension FDD B; its function is the same as the MOB# pin of FDC.
		OD12	EXTENSION 2FDD MODE: MOB2# This pin is for Extension FDD A and B; its function is the same as the MOB# pin of FDC.

1.3 Multi-Mode Parallel Port (Conts')

SYMBOL	PIN	I/O	FUNCTION
ACK#	24	IN_t	PRINTER MODE: ACK# An active low input on this pin indicates that the printer has received data and is ready to accept more data. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(DSB#)		OD_{12}	EXTENSION FDD MODE: DSB2# This pin is for the Extension FDD B; its functions is the same as the DSB# pin of FDC.
		OD12	EXTENSION 2FDD MODE: DSB2# This pin is for Extension FDD A and B; its function is the same as the DSB# pin of FDC.
PD0	25	I/O_{12t}	PRINTER MODE: PD0 Parallel port data bus bit 0. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(INDEX2#)		IN_t	EXTENSION FDD MODE: INDEX2# This pin is for Extension FDD B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION 2FDD MODE: INDEX2# This pin is for Extension FDD A and B; its function is the same as the INDEX# pin of FDC. It is pulled high internally.
PD1	26	I/O_{12t}	PRINTER MODE: PD1 Parallel port data bus bit 1. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(TRAK02#)		IN_t	EXTENSION FDD MODE: TRAK02# This pin is for Extension FDD B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: TRAK02# This pin is for Extension FDD A and B; its function is the same as the TRAK0# pin of FDC. It is pulled high internally.
PD2	27	I/O_{12t}	PRINTER MODE: PD2 Parallel port data bus bit 2. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(WP2#)		IN_t	EXTENSION FDD MODE: WP2# This pin is for Extension FDD B; its function is the same as the WP# pin of FDC. It is pulled high internally.
		IN_t	EXTENSION. 2FDD MODE: WP2# This pin is for Extension FDD A and B; its function is the same as the WP# pin of FDC. It is pulled high internally.

1.3 Multi-Mode Parallel Port (Conts')

SYMBOL	PIN	I/O	FUNCTION
PD3 (RDATA2#)	28	I/O_{12t} IN_t IN_t	PRINTER MODE: PD3 Parallel port data bus bit 3. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: RDATA2# This pin is for Extension FDD B; its function is the same as the RDATA# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: RDATA2# This pin is for Extension FDD A and B; its function is the same as the RDATA# pin of FDC. It is pulled high internally.
PD4 (DSKCHG2#)	29	I/O_{12t} IN_t IN_t	PRINTER MODE: PD4 Parallel port data bus bit 4. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: DSKCHG2# This pin is for Extension FDD B; the function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally. EXTENSION 2FDD MODE: DSKCHG2# This pin is for Extension FDD A and B; this function of this pin is the same as the DSKCHG# pin of FDC. It is pulled high internally.
PD5	30	I/O_{12t} - -	PRINTER MODE: PD5 Parallel port data bus bit 5. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: This pin is a tri-state output.
PD6 (MOA2#)	31	I/OD_{12t} - OD_{12}	PRINTER MODE: PD6 Parallel port data bus bit 6. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION. 2FDD MODE: MOA2# This pin is for Extension FDD A; its function is the same as the MOA# pin of FDC.
PD7 (DSA2#)	32	I/OD_{12t} - OD_{12}	PRINTER MODE: PD7 Parallel port data bus bit 7. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode. EXTENSION FDD MODE: This pin is a tri-state output. EXTENSION 2FDD MODE: DSA2# This pin is for Extension FDD A; its function is the same as the DSA# pin of FDC.

1.3 Multi-Mode Parallel Port (Conts')

SYMBOL	PIN	I/O	FUNCTION
SLIN#	33	OD_{12}	PRINTER MODE: SLIN# Output line for detection of printer selection. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(STEP2#)		OD_{12}	EXTENSION FDD MODE: STEP2# This pin is for Extension FDD B; its function is the same as the STEP# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: STEP2# This pin is for Extension FDD A and B; its function is the same as the STEP# pin of FDC.
INIT#	34	OD_{12}	PRINTER MODE: INIT# Output line for the printer initialization. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(DIR2#)		OD_{12}	EXTENSION FDD MODE: DIR2# This pin is for Extension FDD B; its function is the same as the DIR# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DIR2# This pin is for Extension FDD A and B; its function is the same as the DIR# pin of FDC.
ERR#	36	IN_t	PRINTER MODE: ERR# An active low input on this pin indicates that the printer has encountered an error condition. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(HEAD2#)		OD_{12}	EXTENSION FDD MODE: HEAD2# This pin is for Extension FDD B; its function is the same as the HEAD# pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: HEAD2# This pin is for Extension FDD A and B; its function is the same as the HEAD# pin of FDC.

1.3 Multi-Mode Parallel Port (Conts')

SYMBOL	PIN	I/O	FUNCTION
AFD#	37	OD_{12}	PRINTER MODE: AFD# An active low output from this pin causes the printer to auto feed a line after a line is printed. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
(DRVDEN0)		OD_{12}	EXTENSION FDD MODE: DRVDEN0 This pin is for Extension FDD B; its function is the same as the DRVDEN0 pin of FDC.
		OD_{12}	EXTENSION 2FDD MODE: DRVDEN0 This pin is for Extension FDD A and B; its function is the same as the DRVDEN0 pin of FDC.
STB#	38	OD_{12}	PRINTER MODE: STB# An active low output is used to latch the parallel data into the printer. This pin is pulled high internally. Refer to the description of the parallel port for the definition of this pin in ECP and EPP mode.
		-	EXTENSION FDD MODE: This pin is a tri-state output.
		-	EXTENSION 2FDD MODE: This pin is a tri-state output.

1.4 Serial Port Interface and Infrared Port

SYMBOL	PIN	I/O	FUNCTION
CTSA#	39	In_t	Clear To Send. It is the modem control input. The function of these pins can be tested by reading bit 4 of the handshake status register.
DSRA#	41	In_t	Data Set Ready. An active low signal indicates the modem or data set is ready to establish a communication link and transfer data to the UART.
RTSA# (HEFRAS)	42	I/O_{8t}	UART A Request To Send. An active low signal informs the modem or data set that the controller is ready to send data. During power-on reset, this pin is pulled down internally and is defined as HEFRAS and configuration port's address is slected to 2Eh, which provides the power-on value for CRXX bit X (HEFRAS). A 4.7 kΩ resistor is recommended if intends to pull up and selects 4EH as configuration I/O port's address)

1.4 Serial Port Interface (Conts')

SYMBOL	PIN	I/O	FUNCTION
DTRA# (PNPCSV#) 	43	I/O_{8t}	UART A Data Terminal Ready. An active low signal informs the modem or data set that the controller is ready to communicate. During power-on reset, this pin is pulled down internally and is defined as PNPCSV#, which provides the power-on value for CR24 bit 0 (PNPCSV#). A 4.7 kΩ is recommended if intends to pull up. (clear the default value of FDC, UARTs, and PRT)
SINA	44	IN_t	Serial Input. It is used to receive serial data through the communication link.
SOUTA (PEN48)	45	I/O_8 IN_t	UART A Serial Output. It is used to transmit serial data out to the communication link. During power-on reset, this pin is pulled down internally and is defined as PEN48 and the clock input (Pin 6) should be 48MHz, which provides the power-on value for CRxx bit x (EN48). A 4.7 kΩ resistor is recommended if intends to pull up and 24MHz input is slected.
DCDA#	46	IN_t	Data Carrier Detect. An active low signal indicates the modem or data set has detected a data carrier.
RIA#	47	IN_t	Ring Indicator. An active low signal indicates that a ring signal is being received from the modem or data set.
IRRX	48	IN_{ts}	Alternate Function Input: Infrared Receiver input.
IRTX	49	OUT_{12t}	Alternate Function Output: Infrared Transmitter Output.
IRSEL0_ IRRXH	50	I/O_{12t}	After reset, this pin is Infrared Control Signal 0 , this signal is output and selecte FIR or SIR mode for IR module . This pin can be set as IRRXH , the signal is high speed infrared receiver input

1.5 KBC and FLASH ROM Interface

SYMBOL	PIN	I/O	FUNCTION
P80CS# (GP10) (PLED)	4	I/OD12	Decoded I/O write asserted and the address 0x80h to output selected signal. General purpose I/O PORT 1 , Programmable Power LED.
RTCCS# (GP11) (WDTO)	5	I/OD12	Decoded the address 0x70h and 0x71h to output selected signal . General purpose I/O PORT 1 , Programmable watch dog timer.
KBCS# (GP20) (PENKB#)	52	O12 I/O12 IN_t	Decode the address 60h and 64h to output selected signal. Enable by PENKB# signal with Low-level during power-on setting. General purpose I/O PORT 2 , During power-on reset, this pin is pulled down internally and is defined as PENKB# and all the K/B interface will be active, which provides the power on value for CR24 bit 7. A 4.7kΩ resistor is recommended if intends to pull up and disable K/B functions.
MCCS# (GP21)	53	O12 I/O12	Decode the address 62h and 66h to output selected signal Enable by PENKB# signal with Lo-level during power-on setting. General purpose I/O PORT 2 ,
IRQ1IN (GP22)	54	In_t I/O12	Parallel Interrupt Requested Input 1. This interrupt request is used for specific K/B functions. General purpose I/O PORT 2 ,
IRQ12IN (GP23)	55	In_t I/O12	Parallel Interrupt Requested Input 12. This interrupt request is used for specific K/B functions. General purpose I/O PORT 2 ,
IOR# (GP24)	56	O12t I/O12t	**I/O Read.** IOR# is the command to an ISA I/O slave device that the slave may drive data on to the ISA data bus (XD[0:7]). General purpose I/O PORT 2 ,.
IOW# (GP25)	57	O12t I/O12t	**I/O Write.** IOW# is the command to an ISA I/O slave device that the slave may latch data from the ISA data bus (XD[0:7]). General purpose I/O PORT 2 ,
XD[0:7] (GP30-GP37)	58-60 62-66	I/O_{12t} I/O_{12t}	**XData BUS. X**D[0:7] provide the 8-bit data path for KBC and ROM devices residing on the ISA Bus. General purpose I/O PORT 3 ,

1.5 KBC and FLASH ROM Interface (Conts')

SYMBOL	PIN	I/O	FUNCTION
MEMR# (GP12)	67	O_{12t} I/O_{12t}	Flash ROM interface Memory Read Enable General purpose I/O PORT 1 ,
MEMW# (GP13)	68	O_{12t} I/O_{12t}	Flash ROM interface Memory Write Enable General purpose I/O PORT 1 ,
ROMCS# (GP14) (PENROM#)	69	OD_{12} I/OD_{12} IN_t	Flash ROM interface Chip Select General purpose I/O PORT 1 , During power-on reset , this pin is pulled down internally and is defined as PENROM# and decoded memory address of BIOS to output selected signal, which provides the power on value for CR24 bit 1. A 4.7kΩ is recommended if intends to pull up and disable BIOS ROM function .
XA0 (GP15)	70	O I/O_{12t}	Flash ROM interface Address 0. General purpose I/O PORT 1 ,
XA1 (GP26)	71	O I/O_{12t}	Flash ROM interface Address 1. General purpose I/O PORT 2 ,
XA2 (GP27)	72	O I/O_{12t}	Flash ROM interface Address 2. General purpose I/O PORT 2 ,
XA3-XA10 (GP40-GP47)	73-80	O I/O_{12t}	Flash ROM interface Address [3:10]. General purpose I/O PORT 4 ,
XA11-XA18 (GP50-GP57)	81-84 86-89	O I/O_{12t}	Flash ROM interface Address [11:18]. General purpose I/O PORT 5 ,

1.6 POWER PINS

SYMBOL	PIN	FUNCTION
VCC3V	15, 51	+3.3V power supply for core logic and driving 3V on host interface.
VCC	40, 90	+5V or +3.3V power supply for device output pad.
GND	10, 35, 61, 85	Ground.

2 LPC Interface

LPC interface is to replace ISA interface serving as a bus interface between host (chip-set) and peripheral (Winbond I/O). Data transfer on the LPC bus are serialized over a 4 bit bus. The general characteristics of the interface implemented in Winbond LPC I/O are:

- One control line, namely LFRAME#, which is used by the host to start or stop transfers. No peripherals drive this signal.
- The LAD[3:0] bus, which communicates information serially. The information conveyed are cycle type, cycle direction, chip selection, address, data, and wait states.
- MR (master reset) of Winbond ISA I/O is replaced with a active low reset signal, namely LRESET#, in Winbond LPC I/O.
- An additional 33 MHz PCI clock is needed in Winbond LPC I/O for synchronization.
- DMA requests are issued through LDRQ#.
- Interrupt requests are issued through SERIRQ.
- Power management events are issued through PME#.

Comparing to its ISA counterpart, LPC implementation saves up to 40 pin counts free for integrating more devices on a single chip.

The transition from ISA to LPC is transparent in terms of software which means no BIOS or device driver update is needed except chip-specific configuration.

3. FDC FUNCTIONAL DESCRIPTION

3.1 W83L517D FDC

The floppy disk controller of the W8369L517D integrates all of the logic required for floppy disk control. The FDC implements a PC/AT or PS/2 solution. All programmable options default to compatible values. The FIFO provides better system performance in multi-master systems. The digital data separator supports up to 2 M bits/sec data rate.

The FDC includes the following blocks: AT interface, Precompensation, Data Rate Selection, Digital Data Separator, FIFO, and FDC Core.

3.1.1 AT interface

The interface consists of the standard asynchronous signals: RD#, WR#, A0-A3, IRQ, DMA control, and a data bus. The address lines select between the configuration registers, the FIFO and control/status registers. This interface can be switched between PC/AT, Model 30, or PS/2 normal modes. The PS/2 register sets are a superset of the registers found in a PC/AT.

3.1.2 FIFO (Data)

The FIFO is 16 bytes in size and has programmable threshold values. All command parameter information and disk data transfers go through the FIFO. Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The FIFO defaults to disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the CONFIGURE command. The advantage of the FIFO is that it allows the system a larger DMA latency without causing disk errors. The following tables give several examples of the delays with a FIFO. The data are based upon the following formula:

THRESHOLD # $\times$ (1/DATA/RATE) *8 - 1.5 µS = DELAY

FIFO THRESHOLD	Maximum Delay to Servicing at 500K bps
	Data Rate
1 Byte	1 $\times$ 16 µS - 1.5 µS = 14.5 µS
2 Byte	2 $\times$ 16 µS - 1.5 µS = 30.5 µS
8 Byte	8 $\times$ 16 µS - 1.5 µS = 6.5 µS
15 Byte	15 $\times$ 16 µS - 1.5 µS = 238.5 µS
FIFO Threshold	Maximum Delay to Servicing at 1M bps
	Data Rate
1 Byte	1 $\times$ 8 µS - 1.5 µS = 6.5 µS
2 Byte	2 $\times$ 8 µS - 1.5 µS = 14.5 µS
8 Byte	8 $\times$ 8 µS - 1.5 µS = 62.5 µS
15 Byte	15 $\times$ 8 µS - 1.5 µS = 118.5 µS

At the start of a command the FIFO is always disabled and command parameters must be sent based upon the RQM and DIO bit settings in the main status register. When the FDC enters the command execution phase, it clears the FIFO of any data to ensure that invalid data are not transferred.

An overrun and under run will terminate the current command and the data transfer. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

DMA transfers are enabled with the SPECIFY command and are initiated by the FDC by activating the DRQ pin during a data transfer command. The FIFO is enabled directly by asserting DACK# and addresses need not be valid.

Note that if the DMA controller is programmed to function in verify mode a pseudo read is performed by the FDC based only on DACK#. This mode is only available when the FDC has been configured into byte mode (FIFO disabled) and is programmed to do a read. With the FIFO enabled the above operation is performed by using the new VERIFY command. No DMA operation is needed.

3.1.3 Data Separator

The function of the data separator is to lock onto the incoming serial read data. When a lock is achieved the serial front end logic of the chip is provided with a clock which is synchronized to the read data. The synchronized clock, called the Data Window, is used to internally sample the serial data portion of the bit cell, and the alternate state samples the clock portion. Serial to parallel conversion logic separates the read data into clock and data bytes.

The Digital Data Separator (DDS) has three parts: control logic, error adjustment, and speed tracking. The DDS circuit cycles once every 12 clock cycles ideally. Any data pulse input will be synchronized and then adjusted by immediate error adjustment. The control logic will generate RDD and RWD for every pulse input. During any cycle where no data pulse is present, the DDS cycles are based on speed. A digital integrator is used to keep track of the speed changes in the input data stream.

3.1.4 Write Pre-compensation

The write pre-compensation logic is used to minimize bit shifts in the RDDATA stream from the disk drive. Shifting of bits is a known phenomenon in magnetic media and is dependent on the disk media and the floppy drive.

The FDC monitors the bit stream that is being sent to the drive. The data patterns that require pre-compensation are well known. Depending upon the pattern, the bit is shifted either early or late relative to the surrounding bits.

3.1.5 Perpendicular Recording Mode

The FDC is also capable of interfacing directly to perpendicular recording floppy drives. Perpendicular recording differs from the traditional longitudinal method in that the magnetic bits are oriented vertically. This scheme packs more data bits into the same area.

FDCs with perpendicular recording drives can read standard 3.5" floppy disks and can read and write perpendicular media. Some manufacturers offer drives that can read and write standard and perpendicular media in a perpendicular media drive.

A single command puts the FDC into perpendicular mode. All other commands operate as they normally do. The perpendicular mode requires a 1 Mbps data rate for the FDC. At this data rate the FIFO eases the host interface bottleneck due to the speed of data transfer to or from the disk.

3.1.6 FDC Core

The W83L517D FDC is capable of performing twenty commands. Each command is initiated by a multi-byte transfer from the microprocessor. The result can also be a multi-byte transfer back to the microprocessor. Each command consists of three phases: command, execution, and result.

Command

The microprocessor issues all required information to the controller to perform a specific operation.

Execution

The controller performs the specified operation.

Result

After the operation is completed, status information and other housekeeping information is provided to the microprocessor.

3.1.7 FDC Commands

Command Symbol Descriptions:

C:	Cylinder number 0 - 256
D:	Data Pattern
DIR:	Step Direction
	DIR = 0, step out
	DIR = 1, step in
DS0:	Disk Drive Select 0
DS1:	Disk Drive Select 1
DTL:	Data Length
EC:	Enable Count
EOT:	End of Track
EFIFO:	Enable FIFO
EIS:	Enable Implied Seek
EOT:	End of track
FIFOTHR:	FIFO Threshold
GAP:	Gap length selection
GPL:	Gap Length
H:	Head number
HDS:	Head number select
HLT:	Head Load Time
HUT:	Head Unload Time
LOCK:	Lock EFIFO, FIFOTHR, PTRTRK bits prevent affected by software reset
MFM:	MFM or FM Mode
MT:	Multi-track
N:	The number of data bytes written in a sector
NCN:	New Cylinder Number

ND: Non-DMA Mode
OW: Overwritten
PCN: Present Cylinder Number
POLL: Polling Disable
PRETRK: Pre-compensation Start Track Number
R: Record
RCN: Relative Cylinder Number
R/W: Read/Write
SC: Sector/per cylinder
SK: Skip deleted data address mark
SRT: Step Rate Time
ST0: Status Register 0
ST1: Status Register 1
ST2: Status Register 2
ST3: Status Register 3
WG: Write gate alters timing of WE

(1) Read Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(2) Read Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(3) Read A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system; FDD reads contents of all cylinders from index hole to EOT
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(4) Read ID

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the cylinder is stored in Data Register
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Disk status after the command has been completed
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(5) Verify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
		---------- DTL/SC ----------								
Execution										No data transfer takes place
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(6) Version

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command code
Result	R	1	0	0	1	0	0	0	0	Enhanced controller

(7) Write Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to Command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after Command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after Command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(8) Write Deleted Data

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- C ----------								Sector ID information prior to command execution
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
	W	---------- EOT ----------								
	W	---------- GPL ----------								
	W	---------- DTL ----------								
Execution										Data transfer between the FDD and system
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- C ----------								Sector ID information after command execution
	R	---------- H ----------								
	R	---------- R ----------								
	R	---------- N ----------								

(9) Format A Track

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- N ----------								Bytes/Sector
	W	---------- SC ----------								Sectors/Cylinder
	W	---------- GPL ----------								Gap 3
	W	---------- D ----------								Filler Byte
Execution for Each Sector Repeat:	W	---------- C ----------								Input Sector Parameters
	W	---------- H ----------								
	W	---------- R ----------								
	W	---------- N ----------								
Result	R	---------- ST0 ----------								Status information after command execution
	R	---------- ST1 ----------								
	R	---------- ST2 ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								
	R	---------- Undefined ----------								

(10) Recalibrate

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt

(11) Sense Interrupt Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command code
Result	R	---------- ST0 ----------								Status information at the end of each seek operation
	R	---------- PCN ----------								

(12) Specify

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	| ---------SRT ---------- | --------- HUT ---------- |								
	W	|---------- HLT ----------| ND								

(13) Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	---------- NCN ----------								
Execution	R									Head positioned over proper cylinder on diskette

(14) Configure

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	------ FIFOTHR ----				
	W		----------PRETRK ----------							
Execution										Internal registers written

(15) Relative Seek

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	Command codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W		---------- RCN ----------							

(16) Dumpreg

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	Registers placed in FIFO
Result	R	---------- PCN-Drive 0----------								
	R	---------- PCN-Drive 1 ----------								
	R	---------- PCN-Drive 2----------								
	R	---------- PCN-Drive 3 ----------								
	R	--------SRT ---------- | --------- HUT --------								
	R	---------- HLT ----------| ND							
	R	---------- SC/EOT ----------								
	R	LOCK	0	D3	D2	D1	D0	GAP	WG	
	R	0	EIS	EFIFO	POLL	------ FIFOTHR --------				
	R	----------PRETRK ----------								

(17) Perpendicular Mode

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Code
	W	OW	0	D3	D2	D1	D0	GAP	WG	

(18) Lock

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Code
Result	R	0	0	0	LOCK	0	0	0	0	

(19) Sense Drive Status

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Code
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	---------- ST3 ----------								Status information about disk drive

(20) Invalid

PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	---------- Invalid Codes ----------								Invalid codes (no operation- FDC goes to standby state)
Result	R	---------- ST0 ----------								ST0 = 80H

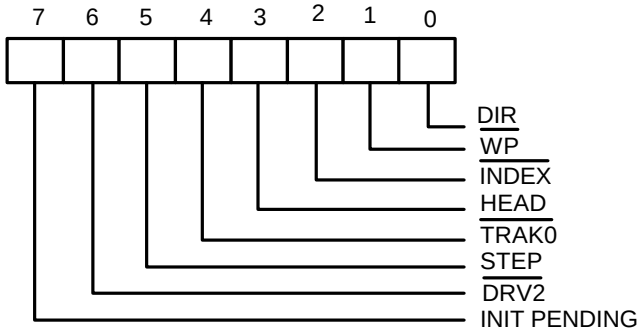
3.2 Register Descriptions

There are several status, data, and control registers in W83L517D. These registers are defined below:

ADDRESS OFFSET	REGISTER	
	READ	WRITE
base address + 0	SA REGISTER	
base address + 1	SB REGISTER	
base address + 2		DO REGISTER
base address + 3	TD REGISTER	TD REGISTER
base address + 4	MS REGISTER	DR REGISTER
base address + 5	DT (FIFO) REGISTER	DT (FIFO) REGISTER
base address + 7	DI REGISTER	CC REGISTER

3.2.1 Status Register A (SA Register) (Read base address + 0)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRV2# (Bit 6):

0 A second drive has been installed

1 A second drive has not been installed

STEP (Bit 5):

This bit indicates the complement of STEP# output.

TRAK0# (Bit 4):

This bit indicates the value of TRAK0# input.

HEAD (Bit 3):

This bit indicates the complement of HEAD# output.

0 side 0

1 side 1

INDEX# (Bit 2):

This bit indicates the value of INDEX# output.

WP# (Bit 1):

0 disk is write-protected

1 disk is not write-protected

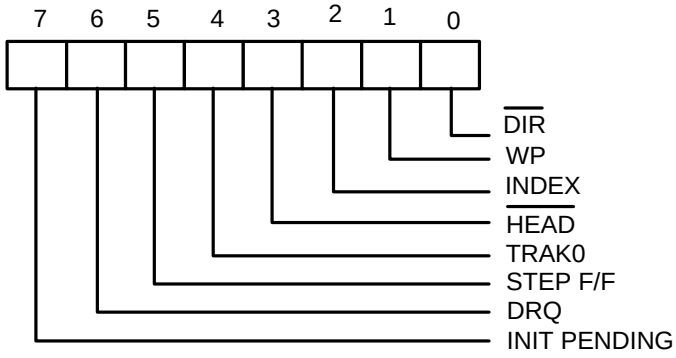
DIR (Bit 0)

This bit indicates the direction of head movement.

0 outward direction

1 inward direction

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



INIT PENDING (Bit 7):

This bit indicates the value of the floppy disk interrupt output.

DRQ (Bit 6):

This bit indicates the value of DRQ output pin.

STEP F/F (Bit 5):

This bit indicates the complement of latched STEP# output.

TRAK0 (Bit 4):

This bit indicates the complement of TRAK0# input.

HEAD# (Bit 3):

This bit indicates the value of HEAD# output.

0 side 1

1 side 0

INDEX (Bit 2):

This bit indicates the complement of INDEX# output.

WP (Bit 1):

0 disk is not write-protected

1 disk is write-protected

DIR# (Bit 0)

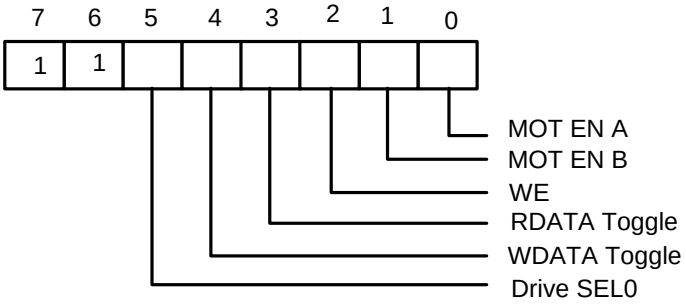
This bit indicates the direction of head movement.

0 inward direction

1 outward direction

3.2.2 Status Register B (SB Register) (Read base address + 1)

This register is used to monitor several disk interface pins in PS/2 and Model 30 modes. In PS/2 mode, the bit definitions for this register are as follows:



Drive SEL0 (Bit 5):

This bit indicates the status of DO REGISTER bit 0 (drive select bit 0).

WDATA Toggle (Bit 4):

This bit changes state at every rising edge of the WD# output pin.

RDATA Toggle (Bit 3):

This bit changes state at every rising edge of the RDATA# output pin.

WE (Bit 2):

This bit indicates the complement of the WE# output pin.

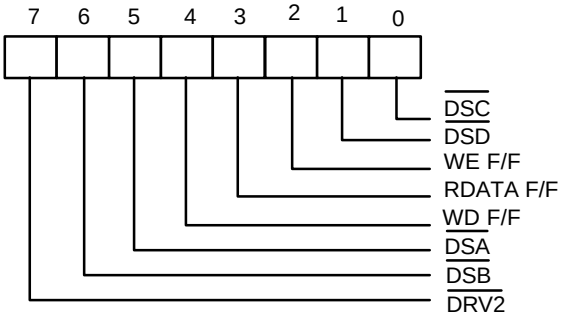
MOT EN B (Bit 1)

This bit indicates the complement of the MOB# output pin.

MOT EN A (Bit 0)

This bit indicates the complement of the MOA# output pin.

In PS/2 Model 30 mode, the bit definitions for this register are as follows:



DRV2# (Bit 7):

0 A second drive has been installed

1 A second drive has not been installed

DSB# (Bit 6):

This bit indicates the status of DSB# output pin.

DSA# (Bit 5):

This bit indicates the status of DSA# output pin.

WD F/F(Bit 4):

This bit indicates the complement of the latched WD# output pin at every rising edge of the WD# output pin.

RDATA F/F(Bit 3):

This bit indicates the complement of the latched RDATA# output pin.

WE F/F (Bit 2):

This bit indicates the complement of latched WE# output pin.

DSD# (Bit 1):

0 Drive D has been selected

1 Drive D has not been selected

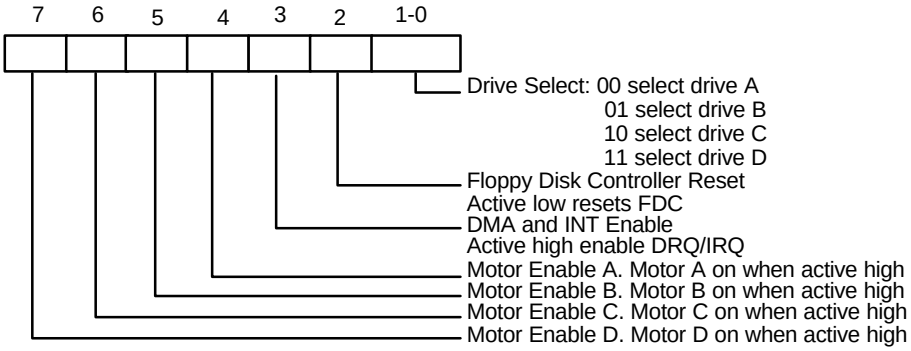
DSC# (Bit 0):

0 Drive C has been selected

1 Drive C has not been selected

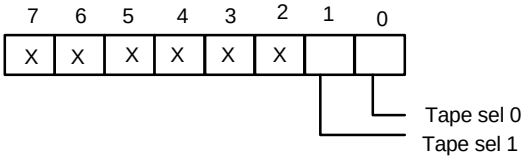
3.2.3 Digital Output Register (DO Register) (Write base address + 2)

The Digital Output Register is a write-only register controlling drive motors, drive selection, DRQ/IRQ enable, and FDC resetting. All the bits of the register are cleared via the MR pin. The bit definitions are as follows:

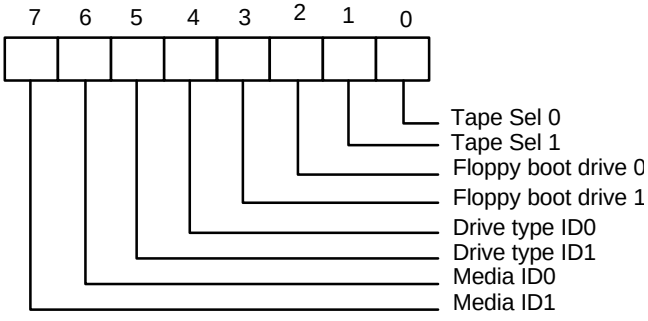


3.2.4 Tape Drive Register (TD Register) (Read base address + 3)

This register is used to assign a particular drive number to the tape drive support mode of the data separator. This register also holds the media ID, drive type, and floppy boot drive information of the floppy disk drive. In normal floppy mode, this register includes only bit 0 and 1. The bit definitions are as follows:



If three mode FDD function is enabled (EN3MODE = 1 in CR9), the bit definitions are as follows:



Media ID1 Media ID0 (Bit 7, 6):

These two bits are read only. These two bits reflect the value of CR8 bit 3, 2.

Drive type ID1 Drive type ID0 (Bit 5, 4):

These two bits reflect two of the bits of CR7. Which two bits are reflected depends on the last drive selected in the DO REGISTER.

Floppy Boot drive 1, 0 (Bit 3, 2):

These two bits reflect the value of CR8 bit 1, 0.

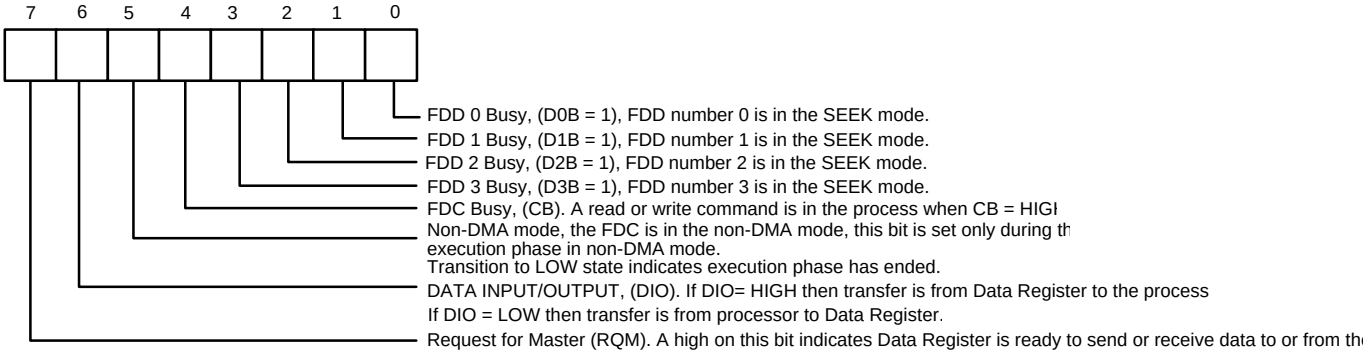
Tape Sel 1, Tape Sel 0 (Bit 1, 0):

These two bits assign a logical drive number to the tape drive. Drive 0 is not available as a tape drive and is reserved as the floppy disk boot drive.

Tape Sel 1	Tape Sel 0	Drive Selected
0	0	None
0	1	1
1	0	2
1	1	3

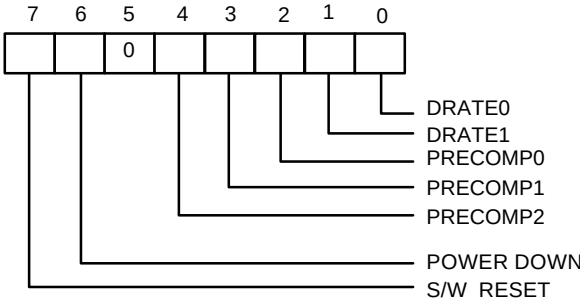
3.2.5 Main Status Register (MS Register) (Read base address + 4)

The Main Status Register is used to control the flow of data between the microprocessor and the controller. The bit definitions for this register are as follows:



3.2.6 Data Rate Register (DR Register) (Write base address + 4)

The Data Rate Register is used to set the transfer rate and write pre-compensation. The data rate of the FDC is programmed via the CC REGISTER for PC-AT and PS/2 Model 30 and PS/2 mode, and not by the DR REGISTER. The real data rate is determined by the most recent write to either of the DR REGISTER or CC REGISTER.



S/W RESET (Bit 7):

This bit is the software reset bit.

POWER-DOWN (Bit 6):

0 FDC in normal mode

1 FDC in power-down mode

PRECOMP2 PRECOMP1 PRECOMP0 (Bit 4, 3, 2):

These three bits select the value of write precompensation. The following tables show the pre-compensation values for the combination of these bits.

PRECOMP	**PRECOMPENSATION DELAY**	
2 1 0	250K - 1 Mbps	2 Mbps Tape drive
0 0 0	Default Delays	Default Delays
0 0 1	41.67 nS	20.8 nS
0 1 0	83.34 nS	41.17 nS
0 1 1	125.00 nS	62.5nS
1 0 0	166.67 nS	83.3 nS
1 0 1	208.33 nS	104.2 nS
1 1 0	250.00 nS	125.00 nS
1 1 1	0.00 nS (disabled)	0.00 nS (disabled)

DATA RATE	DEFAULT PRECOMPENSATION DELAYS
250 KB/S	125 nS
300 KB/S	125 nS
500 KB/S	125 nS
1 MB/S	41.67nS
2 MB/S	20.8 nS

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC and reduced write current control.

00 500 KB/S (MFM), 250 KB/S (FM), $\overline{RWC}$ = 1

01 300 KB/S (MFM), 150 KB/S (FM), $\overline{RWC}$ = 0

10 250 KB/S (MFM), 125 KB/S (FM), $\overline{RWC}$ = 0

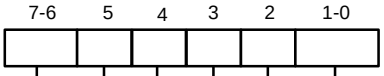
11 1 MB/S (MFM), Illegal (FM), $\overline{RWC}$ = 1

The 2 MB/S data rate for Tape drive is only supported by setting 01 to DRATE1 and DRATE0 bits, as well as setting 10 to DRT1 and DRT0 bits which are two of the Configure Register CRF4 or CRF5 bits in logic device 0. Please refer to the function description of CRF4 or CRF5 and data rate table for individual data rates setting.

3.2.7 FIFO Register (R/W base address + 5)

The Data Register consists of four status registers in a stack with only one register presented to the data bus at a time. This register stores data, commands, and parameters and provides diskette-drive status information. Data bytes are passed through the data register to program or obtain results after a command. In the W83697HF, this register defaults to FIFO disabled mode after reset. The FIFO can change its value and enable its operation through the CONFIGURE command.

Status Register 0 (ST0)



US1, US0 Drive Select:
00 Drive A selected
01 Drive B selected
10 Drive C selected
11 Drive D selected

HD Head address:
1 Head selected
0 Head selected

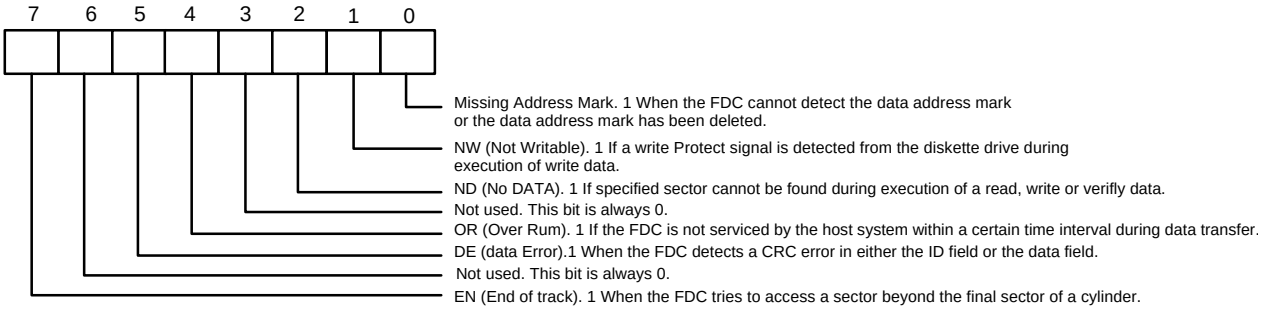
NR Not Ready:
1 Drive is not ready
0 Drive is ready

EC Equipment Check:
1 When a fault signal is received from the FDD or the track 0 signal fails to occur after 77 step pulses
0 No error

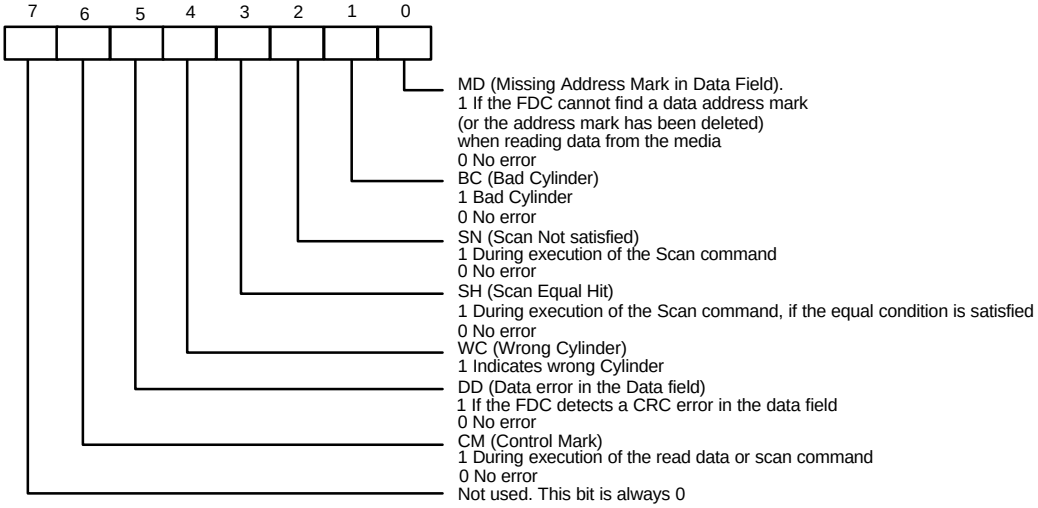
SE Seek end:
1 seek end
0 seek error

IC Interrupt Code:
00 Normal termination of command
01 Abnormal termination of command
10 Invalid command issue
11 Abnormal termination because the ready signal from FDD changed state during command execution

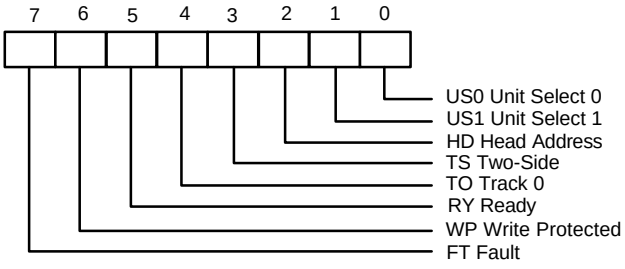
Status Register 1 (ST1)



Status Register 2 (ST2)

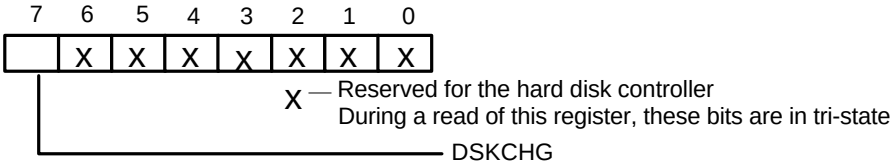


Status Register 3 (ST3)

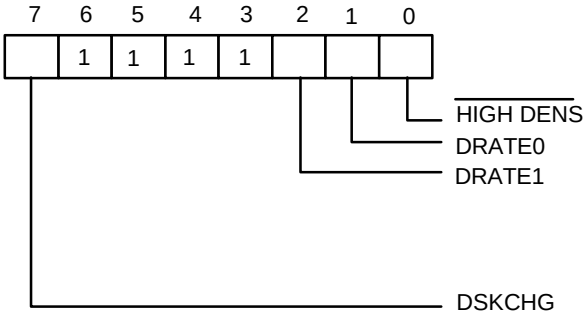


3.2.8 Digital Input Register (DI Register) (Read base address + 7)

The Digital Input Register is an 8-bit read-only register used for diagnostic purposes. In a PC/XT or AT only Bit 7 is checked by the BIOS. When the register is read, Bit 7 shows the complement of DSKCHG#, while other bits of the data bus remain in tri-state. Bit definitions are as follows:



In the PS/2 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the complement of the DSKCHG# input.

Bit 6-3: These bits are always a logic 1 during a read.

DRATE1 DRATE0 (Bit 2, 1):

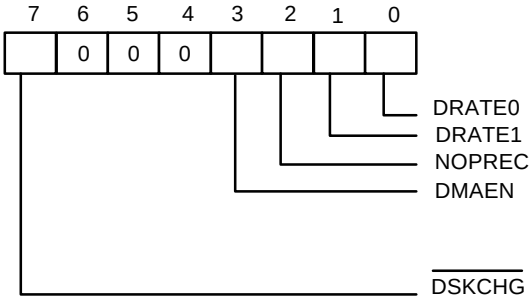
These two bits select the data rate of the FDC. Refer to the DR register bits 1 and 0 for the settings corresponding to the individual data rates.

HIGH DENS# (Bit 0):

0 500 KB/S or 1 MB/S data rate (high density FDD)

1 250 KB/S or 300 KB/S data rate

In the PS/2 Model 30 mode, the bit definitions are as follows:



DSKCHG (Bit 7):

This bit indicates the status of DSKCHG# input.

Bit 6-4: These bits are always logic 1 during a read.

DMAEN (Bit 3):

This bit indicates the value of DO REGISTER bit 3.

NOPREC (Bit 2):

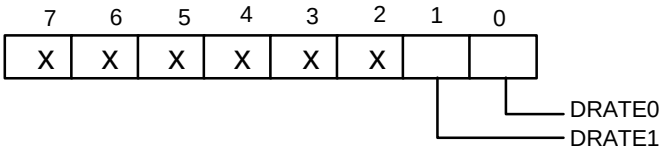
This bit indicates the value of CC REGISTER NOPREC bit.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

3.2.9 Configuration Control Register (CC Register) (Write base address + 7)

This register is used to control the data rate. In the PC/AT and PS/2 mode, the bit definitions are as follows:



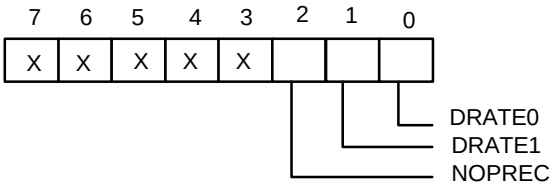
X: Reserved

Bit 7-2: Reserved. These bits should be set to 0.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

In the PS/2 Model 30 mode, the bit definitions are as follows:



X: Reserved

Bit 7-3: Reserved. These bits should be set to 0.

NOPREC (Bit 2):

This bit indicates no pre-compensation. It has no function and can be set by software.

DRATE1 DRATE0 (Bit 1, 0):

These two bits select the data rate of the FDC.

4. UART PORT

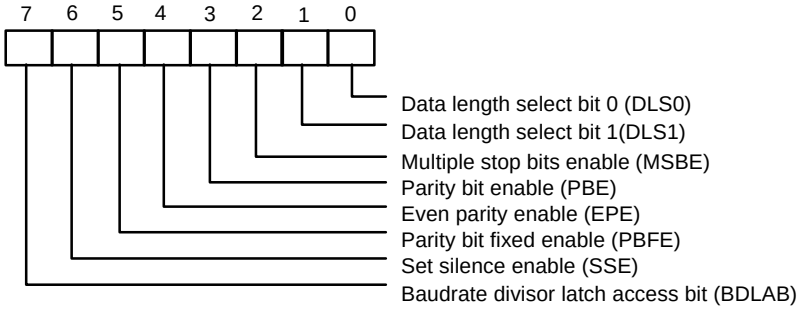
4.1 Universal Asynchronous Receiver/Transmitter (UART A)

The UARTs are used to convert parallel data into serial format on the transmit side and convert serial data to parallel format on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five-bit format only) or two stop bits. The UARTs are capable of handling divisors of 1 to 65535 and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. The UARTs also support the MIDI data rate. Furthermore, the UARTs also include complete modem control capability and a processor interrupt system that may be software trailed to the computing time required to handle the communication link. The UARTs have a FIFO mode to reduce the number of interrupts presented to the CPU. In each UART, there are 16-byte FIFOs for both receive and transmit mode.

4.2 Register Address

4.2.1 UART Control Register (UCR) (Read/Write)

The UART Control Register controls and defines the protocol for asynchronous data communications, including data length, stop bit, parity, and baud rate selection.



Bit 7: BDLAB. When this bit is set to a logical 1, designers can access the divisor (in 16-bit binary format) from the divisor latches of the baud rate generator during a read or write operation. When this bit is reset, the Receiver Buffer Register, the Transmitter Buffer Register, or the Interrupt Control Register can be accessed.

Bit 6: SSE. A logical 1 forces the Serial Output (SOUT) to a silent state (a logical 0). Only IRTX is affected via this bit; the transmitter is not affected.

Bit 5: PBFE. When PBE and PBFE of UCR are both set to a logical 1,

(1) If EPE is logical 1, the parity bit is fixed as logical 0 to transmit and check.

(2) If EPE is logical 0, the parity bit is fixed as logical 1 to transmit and check.

TABLE 4-1 UART Register Bit Map

BIT NUMBER										
REGISTER ADDRESS BASE			0	1	2	3	4	5	6	7
+ 0 BDLAB = 0	**RECEIVER BUFFER REGISTER (READ ONLY)**	**RBR**	RX Data Bit 0	RX Data Bit 1	RX Data Bit 2	RX Data Bit 3	RX Data Bit 4	RX Data Bit 5	RX Data Bit 6	RX Data Bit 7
+ 0 BDLAB = 0	**TRANSMITTER BUFFER REGISTER (WRITE ONLY)**	**TBR**	TX Data Bit 0	TX Data Bit 1	TX Data Bit 2	TX Data Bit 3	TX Data Bit 4	TX Data Bit 5	TX Data Bit 6	TX Data Bit 7
+ 1 BDLAB = 0	**INTERRUPT CONTROL REGISTER**	**ICR**	RBR Data Ready Interrupt Enable (ERDRI)	TBR Empty Interrupt Enable (ETBREI)	USR Interrupt Enable (EUSRI)	HSR Interrupt Enable (EHSRI)	0	0	0	0
+ 2	**INTERRUPT STATUS REGISTER (READ ONLY)**	**ISR**	"0" if Interrupt Pending	Interrupt Status Bit (0)	Interrupt Status Bit (1)	Interrupt Status Bit (2)**	0	0	FIFOs Enabled **	FIFOs Enabled **
+ 2	**UART FIFO CONTROL REGISTER (WRITE ONLY)**	**UFR**	FIFO Enable	RCVR FIFO Reset	XMIT FIFO Reset	DMA Mode Select	Reserved	Reversed	RX Interrupt Active Level (LSB)	RX Interrupt Active Level (MSB)
+ 3	**UART CONTROL REGISTER**	**UCR**	Data Length Select Bit 0 (DLS0)	Data Length Select Bit 1 (DLS1)	Multiple Stop Bits Enable (MSBE)	Parity Bit Enable (PBE)	Even Parity Enable (EPE)	Parity Bit Fixed Enable PBFE)	Set Silence Enable (SSE)	Baudrate Divisor Latch Access Bit (BDLAB)
+ 4	**HANDSHAKE CONTROL REGISTER**	**HCR**	Data Terminal Ready (DTR)	Request to Send (RTS)	Loopback RI Input	IRQ Enable	Internal Loopback Enable	0	0	0
+ 5	**UART STATUS REGISTER**	**USR**	RBR Data Ready (RDR)	Overrun Error (OER)	Parity Bit Error (PBER)	No Stop Bit Error (NSER)	Silent Byte Detected (SBD)	TBR Empty (TBRE)	TSR Empty (TSRE)	RX FIFO Error Indication (RFEI) **
+ 6	**HANDSHAKE STATUS REGISTER**	**HSR**	CTS Toggling (TCTS)	DSR Toggling (TDSR)	RI Falling Edge (FERI)	DCD Toggling (TDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
+ 7	**USER DEFINED REGISTER**	**UDR**	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 0 BDLAB = 1	**BAUDRATE DIVISOR LATCH LOW**	**BLL**	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
+ 1 BDLAB = 1	**BAUDRATE DIVISOR LATCH HIGH**	**BHL**	Bit 8	Bit 9	Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*: Bit 0 is the least significant bit. The least significant bit is the first bit serially transmitted or received.

**: These bits are always 0 in 16450 Mode.

Bit 4: EPE. This bit describes the number of logic 1's in the data word bits and parity bit only when bit 3 is programmed. When this bit is set, an even number of logic 1's are sent or checked. When the bit is reset, an odd number of logic 1's are sent or checked.

Bit 3: PBE. When this bit is set, the position between the last data bit and the stop bit of the SOUT will be stuffed with the parity bit at the transmitter. For the receiver, the parity bit in the same position as the transmitter will be detected.

Bit 2: MSBE. This bit defines the number of stop bits in each serial character that is transmitted or received.

(1) If MSBE is set to a logical 0, one stop bit is sent and checked.

(2) If MSBE is set to a logical 1, and data length is 5 bits, one and a half stop bits are sent and checked.

(3) If MSBE is set to a logical 1, and data length is 6, 7, or 8 bits, two stop bits are sent and checked.

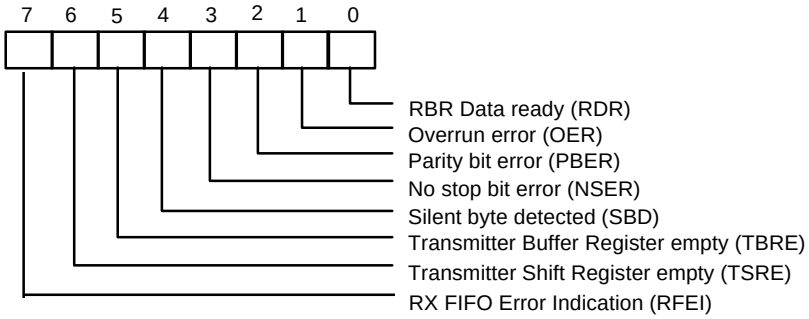
Bits 0 and 1: DLS0, DLS1. These two bits define the number of data bits that are sent or checked in each serial character.

TABLE 4-2 WORD LENGTH DEFINITION

DLS1	DLS0	DATA LENGTH
0	0	5 bits
0	1	6 bits
1	0	7 bits
1	1	8 bits

4.2.2 UART Status Register (USR) (Read/Write)

This 8-bit register provides information about the status of the data transfer during communication.



Bit 7: RFEI. In 16450 mode, this bit is always set to a logic 0. In 16550 mode, this bit is set to a logic 1 when there is at least one parity bit error, no stop bit error or silent byte detected in the FIFO. In 16550 mode, this bit is cleared by reading from the USR if there are no remaining errors left in the FIFO.

Bit 6: TSRE. In 16450 mode, when TBR and TSR are both empty, this bit will be set to a logical 1. In 16550 mode, if the transmit FIFO and TSR are both empty, it will be set to a logical 1. Other thanthese

two cases, this bit will be reset to a logical 0.

Bit 5: TBRE. In 16450 mode, when a data character is transferred from TBR to TSR, this bit will be set to a logical 1. If ETREI of ICR is a logical 1, an interrupt will be generated to notify the CPU to write the next data. In 16550 mode, this bit will be set to a logical 1 when the transmit FIFO is empty. It will be reset to a logical 0 when the CPU writes data into TBR or FIFO.

Bit 4: SBD. This bit is set to a logical 1 to indicate that received data are kept in silent state for a full word time, including start bit, data bits, parity bit, and stop bits. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 3: NSER. This bit is set to a logical 1 to indicate that the received data have no stop bit. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

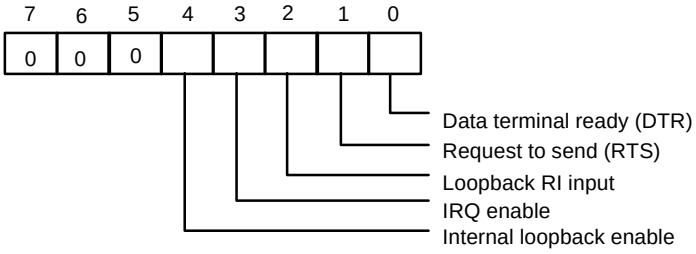
Bit 2: PBER. This bit is set to a logical 1 to indicate that the parity bit of received data is wrong. In 16550 mode, it indicates the same condition for the data on top of the FIFO. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 1: OER. This bit is set to a logical 1 to indicate received data have been overwritten by the next received data before they read by the CPU. In 16550 mode, it indicates the same condition instead of FIFO full. When the CPU reads USR, it will clear this bit to a logical 0.

Bit 0: RDR. This bit is set to a logical 1 to indicate received data are ready to be read by the CPU in the RBR or FIFO. After no data are left in the RBR or FIFO, the bit will be reset to a logical 0.

4.2.3 Handshake Control Register (HCR) (Read/Write)

This register controls the pins of the UART used for handshaking peripherals such as modem, and controls the diagnostic mode of the UART.



Bit 4: When this bit is set to a logical 1, the UART enters diagnostic mode by an internal loopback, as follows:

(1) SOUT is forced to logical 1, and SIN is isolated from the communication link instead of the TSR.

(2) Modem output pins are set to their inactive state.

(3) Modem input pins are isolated from the communication link and connect internally as DTR (bit 0 of HCR) $\rightarrow \overline{DSR}$, RTS (bit 1 of HCR) $\rightarrow \overline{CTS}$, Loop-back RI input (bit 2 of HCR) $\rightarrow \overline{RI}$ and IRQ enable (bit 3 of HCR) $\rightarrow \overline{DCD}$.

Aside from the above connections, the UART operates normally. This method allows the CPU to test the UART in a convenient way.

Bit 3: The UART interrupt output is enabled by setting this bit to be logic 1. In the diagnostic mode this bit is internally connected to the modem control input $\overline{DCD}$.

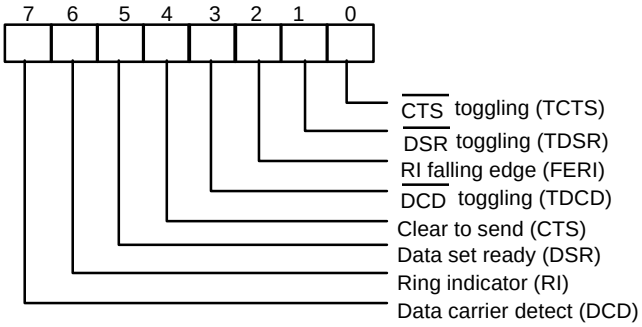
Bit 2: This bit is used only in the diagnostic mode. In the diagnostic mode this bit is internally connected to the modem control input $\overline{RI}$.

Bit 1: This bit controls the $\overline{RTS}$ output. The value of this bit is inverted and output to $\overline{RTS}$.

Bit 0: This bit controls the $\overline{DTR}$ output. The value of this bit is inverted and output to $\overline{DTR}$.

4.2.4 Handshake Status Register (HSR) (Read/Write)

This register reflects the current state of four input pins for handshake peripherals such as a modem and records changes on these pins.



Bit 7: This bit is the opposite of the $\overline{DCD}$ input. This bit is equivalent to bit 3 of HCR in loop-back mode.

Bit 6: This bit is the opposite of the $\overline{RI}$ input. This bit is equivalent to bit 2 of HCR in loop-back mode.

Bit 5: This bit is the opposite of the $\overline{DSR}$ input. This bit is equivalent to bit 0 of HCR in loop-back mode.

Bit 4: This bit is the opposite of the $\overline{CTS}$ input. This bit is equivalent to bit 1 of HCR in loop-back mode.

Bit 3: TDCD. This bit indicates that the $\overline{DCD}$ pin has changed state after HSR was read by the CPU.

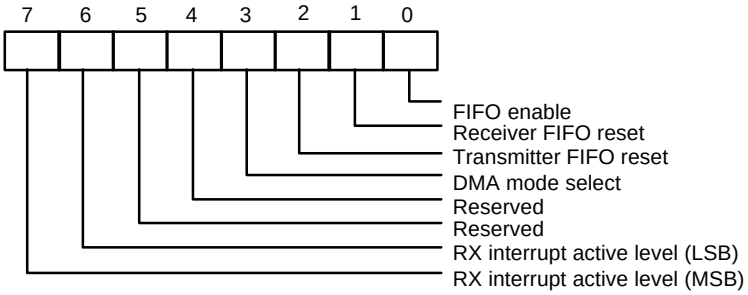
Bit 2: FERI. This bit indicates that the $\overline{RI}$ pin has changed from low to high state after HSR was read by the CPU.

Bit 1: TDSR. This bit indicates that the $\overline{DSR}$ pin has changed state after HSR was read by the CPU.

Bit 0: TCTS. This bit indicates that the $\overline{CTS}$ pin has changed state after HSR was read.

4.2.5 UART FIFO Control Register (UFR) (Write only)

This register is used to control the FIFO functions of the UART.



Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes, once there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify the CPU to read the data from the FIFO.

TABLE 4-3 FIFO TRIGGER LEVEL

Bit 7	Bit 6	RX FIFO Interrupt Active Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

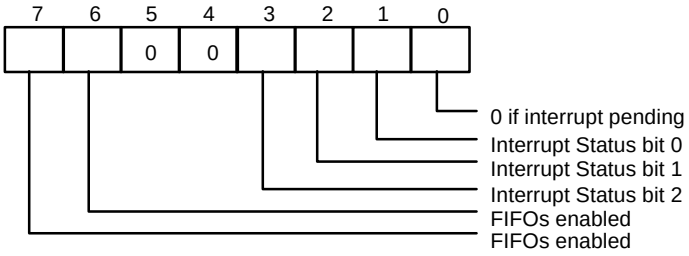
Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 1: Setting this bit to a logical 1 resets the RX FIFO counter logic to initial state. This bit will clear to a logical 0 by itself after being set to a logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the UART. This bit should be set to a logical 1 before other bits of UFR are programmed.

4.2.6 Interrupt Status Register (ISR) (Read only)

This register reflects the UART interrupt status, which is encoded by different interrupt sources into 3 bits.



Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logic 0.

Bit 3: In 16450 mode, this bit is 0. In 16550 mode, both bit 3 and 2 are set to a logical 1 when a time-out interrupt is pending.

Bit 2, 1: These two bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to a logical 0.

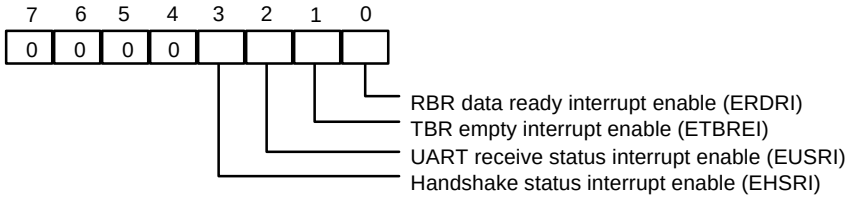
TABLE 4-4 INTERRUPT CONTROL FUNCTION

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	UART Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Timeout	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)
0	0	0	0	Fourth	Handshake status	1. TCTS = 1 2. TDSR = 1 3. FERI = 1 4. TDCD = 1	Read HSR

** Bit 3 of ISR is enabled when bit 0 of UFR is logical 1.

4.2.7 Interrupt Control Register (ICR) (Read/Write)

This 8-bit register allows the five types of controller interrupts to activate the interrupt output signal separately. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Control Register (ICR). A selected interrupt can be enabled via setting the appropriate bits of this register to a logical 1.



Bit 7-4: These four bits are always logic 0.

Bit 3: EHSRI. Setting this bit to a logical 1 enables the handshake status register interrupt.

Bit 2: EUSRI. Setting this bit to a logical 1 enables the UART status register interrupt.

Bit 1: ETBREI. Setting this bit to a logical 1 enables the TBR empty interrupt.

Bit 0: ERDRI. Setting this bit to a logical 1 enables the RBR data ready interrupt.

4.2.8 Programmable Baud Generator (BLL/BHL) (Read/Write)

Two 8-bit registers, BLL and BHL, compose a programmable baud generator that uses 24 MHz to generate a 1.8461 MHz frequency and divides it by a divisor from 1 to 2^{16}-1. The output frequency of the baud generator is the baud rate multiplied by 16, and this is the base frequency for the transmitter and receiver. The table in the next page illustrates the use of the baud generator with a frequency of 1.8461 MHz. In high-speed UART mode (refer to CR0C bit7 and CR0C bit6), the programmable baud generator directly uses 24 MHz and the same divisor as the normal speed divisor. In high-speed mode, the data transmission rate can be as high as 1.5M bps.

4.2.9 User-defined Register (UDR) (Read/Write)

This is a temporary register that can be accessed and defined by the user.

TABLE 4-5 BAUD RATE TABLE

BAUD RATE From different Pre-divider				
Pre-Div: 13 1.8461M Hz	Pre-Div:1.625 14.769M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage between desired and actual
50	400	650	**2304**	**
75	600	975	**1536**	**
110	880	1430	**1047**	0.18%
134.5	1076	1478.5	**857**	0.099%
150	1200	1950	**768**	**
300	2400	3900	**384**	**
600	4800	7800	**192**	**
1200	9600	15600	**96**	**
1800	14400	23400	**64**	**
2000	16000	26000	**58**	0.53%
2400	19200	31200	**48**	**
3600	28800	46800	**32**	**
4800	38400	62400	**24**	**
7200	57600	93600	**16**	**
9600	76800	124800	**12**	**
19200	153600	249600	**6**	**
38400	307200	499200	**3**	**
57600	460800	748800	**2**	**
115200	921600	1497600	**1**	**

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

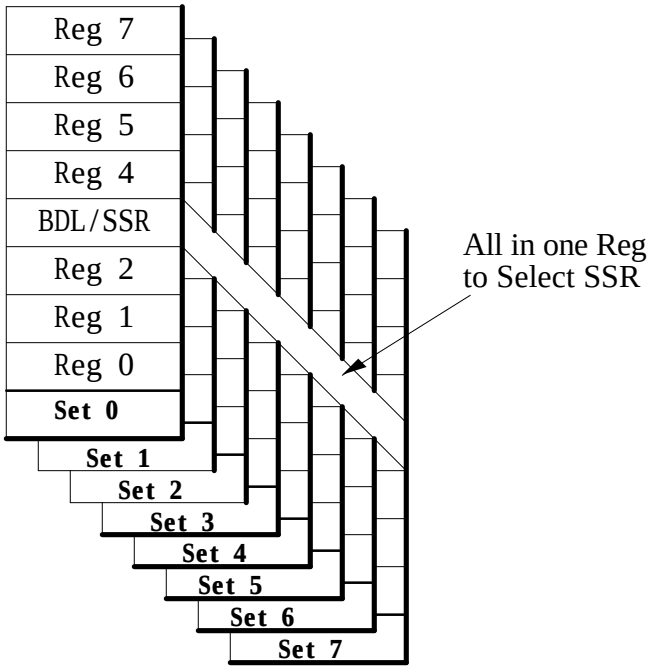
Note. Pre-Divisor is determined by CRF0 of UART A

5. INFRARED (IR) Port

The Infrared (IR) function provides a point-to-point (or multi-point to multi-point) wireless communication which can operate under various transmission protocols including IrDA 1.0 SIR, IrDA 1.1 MIR (1.152 Mbps), IrDA 1.1 FIR (4 Mbps), SHARP ASK-IR, and remote control (NEC, RC-5, advanced RC-5, and RECS-80 protocol).

5.1 IR Register Description

When bank select enable bit (ENBNKSEL, the bit 0 in CRF0 of logic device 6) is set, legacy IR will be switched to Advanced IR, and eight Register Sets can then be accessible. These Register Sets control enhanced IR, SIR, MIR, or FIR. Also, a superior traditional SIR function can be used with enhanced features such as 32-byte transmitter/receiver FIFOs, non-encoding IRQ identify status register, and automatic flow control. The MIR/FIR and remote control registers are also defined in these Register Sets. Structure of these Register Sets is as shown below.



*Set 0, 1 are legacy/Advanced UART Registers
*Set 2~7 are Advanced UART Registers

Each of these register sets has a common register, namely *Sets Select Register* (SSR), in order to switch to another register set. The summary description of these *Sets* is given below.

Set	Sets Description
0	Legacy/Advanced IR Control and Status Registers.
1	Legacy Baud Rate Divisor Register.
2	Advanced IR Control and Status Registers.
3	Version ID and Mapped Control Registers.
4	Transmitter/Receiver/Timer Counter Registers and IR Control Registers.
5	Flow Control and IR Control and Frame Status FIFO Registers.
6	IR Physical Layer Control Registers
7	Remote Control and IR front-end Module Selection Registers.

5.2 Set0-Legacy/Advanced IR Control and Status Registers

Address Offset	Register Name	Register Description
0	**RBR/TBR**	Receiver/Transmitter Buffer Registers
1	**ICR**	Interrupt Control Register
2	**ISR/UFR**	Interrupt Status or IR FIFO Control Register
3	**UCR/SSR**	IR Control or Sets Select Register
4	**HCR**	Handshake Control Register
5	**USR**	IR Status Register
6	**HSR**	Handshake Status Register
7	**UDR/ESCR**	User Defined Register

5.2.1 Set0.Reg0 - Receiver/Transmitter Buffer Registers (RBR/TBR) (Read/Write)

Receiver Buffer Register is read only and Transmitter Buffer Register is write only. When operating in the PIO mode, the port is used to Receive/Transmit 8-bit data.

When function as a legacy IR, this port only supports PIO mode. If set in the advanced IR mode and configured as MIR/FIR/Remote IR, this port also can support DMA transmission. Two DMA channels can be used simultaneously, one for TX DMA and the other for RX DMA. Therefore, single DMA channel is also supported when the bit of D_CHSW (DMA Channel Swap, in Set2.Reg2.Bit3) is set and the TX/RX DMA channel is swapped. Note that two DMA channels can be defined in configure register CR2A, which selects DMA channel or disables DMA channel. If only RX DMA channel is enabled while TX DMA channel is disabled, then the single DMA channel will be selected.

5.2.2 Set0.Reg1 - Interrupt Control Register (ICR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	0	0	0	0	0	EUSRI	ETBREI	ERDRI
Advanced IR	ETMRI	EFSFI	ETXTHI	EDMAI	0	EUSRI/ TXURI	ETBREI	ERBRI

The advanced IR functions including Advanced SIR/ASK-IR, MIR, FIR, or Remote IR are described below.

Bit 7: *Legacy IR Mode:*

Not used. A read will return 0.

Advanced IR Mode:

ETMRI - Enable Timer Interrupt

A write to 1 will enable timer interrupt.

Legacy IR Mode:

Bit6: *Legacy IR Mode:*

Not used. A read will return 0.

MIR, FIR mode:

EFSFI - Enable Frame Status FIFO Interrupt

A write to 1 will enable frame status FIFO interrupt.

Advanced SIR/ASK-IR, Remote IR:

Not used.

Bit 5: *Legacy IR Mode:*

Not used. A read will return 0.

Advanced SIR/ASK-IR, MIR, FIR, Remote IR:

ETXTHI - Enable Transmitter Threshold Interrupt

A write to 1 will enable transmitter threshold interrupt.

Legacy IR Mode:

Bit 4:

Not used. A read will return 0.

MIR, FIR, Remote IR:

EDMAI - Enable DMA Interrupt.

A write to 1 will enable DMA interrupt.

Bit 3: Reserved. A read will return 0.

Bit 2: *Legacy IR Mode:*

EUSRI - Enable USR (IR Status Register) Interrupt

A write to 1 will enable IR status register interrupt.

Advanced SIR/ASK-IR:

EUSRI - Enable USR (IR Status Register) Interrupt

A write to 1 will enable IR status register interrupt.

MIR, FIR, Remote Controller:

EHSRI/ETXURI - Enable USR Interrupt *or* Enable Transmitter Underrun Interrupt

A write to 1 will enable USR interrupt or enable transmitter underrun interrupt.

Bit 1: **ETBREI - Enable TBR (Transmitter Buffer Register) Empty Interrupt**

A write to 1 will enable the transmitter buffer register empty interrupt.

Bit 0: **ERBRI - Enable RBR (Receiver Buffer Register) Interrupt**

A write to 1 will enable receiver buffer register interrupt.

5.2.3 Set0.Reg2 - Interrupt Status Register/IR FIFO Control Register (ISR/UFR)

Interrupt Status Register (Read Only)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	FIFO Enable	FIFO Enable	0	0	IID2	IID1	IID0	IP
Advanced IR	TMR_I	FSF_I	TXTH_I	DMA_I	HS_I	USR_I/ FEND_I	TXEMP_I	RXTH_I
Reset Value	0	0	1	0	0	0	1	0

Legacy IR:

This register reflects the Legacy IR interrupt status, which is encoded by different interrupt sources into 3 bits.

Bit 7, 6: These two bits are set to a logical 1 when UFR bit 0 = 1.

Bit 5, 4: These two bits are always logical 0.

Bit 3: When not in FIFO mode, this bit is always 0. In FIFO mode, both bit 3 and 2 are set to logical 1 when a time-out interrupt is pending.

Bit 2, 1: These bits identify the priority level of the pending interrupt, as shown in the table below.

Bit 0: This bit is a logical 1 if there is no interrupt pending. If one of the interrupt sources has occurred, this bit will be set to logical 0.

TABLE: INTERRUPT CONTROL FUNCTION

ISR				INTERRUPT SET AND FUNCTION			
Bit 3	Bit 2	Bit 1	Bit 0	Interrupt priority	Interrupt Type	Interrupt Source	Clear Interrupt
0	0	0	1	-	-	No Interrupt pending	-
0	1	1	0	First	IR Receive Status	1. OER = 1 2. PBER =1 3. NSER = 1 4. SBD = 1	Read USR
0	1	0	0	Second	RBR Data Ready	1. RBR data ready 2. FIFO interrupt active level reached	1. Read RBR 2. Read RBR until FIFO data under active level
1	1	0	0	Second	FIFO Data Time-out	Data present in RX FIFO for 4 characters period of time since last access of RX FIFO.	Read RBR
0	0	1	0	Third	TBR Empty	TBR empty	1. Write data into TBR 2. Read ISR (if priority is third)

** Bit 3 of ISR is enabled when bit 0 of UFR is a logical 1.

Advanced IR:

Bit 7: **TMR_I - Timer Interrupt.**

Set to 1 when timer counts to logical 0. This bit is valid when: (1) the timer registers are defined in Set4.Reg0 and Set4.Reg1; (2) EN_TMR(Enable Timer, in Set4.Reg2.Bit0) is set to 1; (3) ENTMR_I (Enable Timer Interrupt, in Set0.Reg1.Bit7) is set to 1.

Bit 6: *MIR, FIR modes:*

FSF_I - Frame Status FIFO Interrupt.

Set to 1 when Frame Status FIFO is equal or larger than the threshold level *or* Frame Status FIFO time-out occurs. Cleared to 0 when Frame Status FIFO is below the threshold level.

Advanced SIR/ASK-IR, Remote IR modes: Not used.

Bit 5: **TXTH_I - Transmitter Threshold Interrupt.**

Set to 1 if the TBR (Transmitter Buffer Register) FIFO is below the threshold level. Cleared to 0 if the TBR (Transmitter Buffer Register) FIFO is above the threshold level.

Bit 4: *MIR, FIR, Remote IR Modes:*

DMA_I - DMA Interrupt.

Set to 1 if the DMA controller 8237A sends a TC (Terminal Count) to I/O device which might be a transmitter TC or a Receiver TC. Cleared to 0 when this register is read.

Bit 3: **HS_I - Handshake Status Interrupt.**

Set to 1 when the Handshake Status Register has a toggle. Cleared to 0 when Handshake Status Register (HSR) is read. Note that in all IR modes including SIR, ASK-IR, MIR, FIR, and Remote Control IR, this bit defaults to be inactive unless IR Handshake Status Enable (IRHS_EN) is set to 1.

Bit 2: *Advanced SIR/ASK-IR modes:*

USR_I - IR Status Interrupt.

Set to 1 when overrun error, parity error, stop bit error, or silent byte error is detected and registered in the IR Status Register (USR). Cleared to 0 when USR is read.

MIR, FIR modes:

FEND_I - Frame End Interrupt.

Set to 1 when (1) a frame has a grace end to be detected where the frame signal is defined in the physical layer of IrDA version 1.1; (2) abort signal or illegal signal has been detected during receiving valid data. Cleared to 0 when this register is read.

Remote Controller Mode: Not used.

Bit 1: **TXEMP_I - Transmitter Empty.**

Set to 1 when transmitter (or, say, FIFO + Transmitter) is empty. Cleared to 0 when this register is read.

Bit 0: **RXTH_I – Receiver Threshold Interrupt.**

Set to 1 when (1) the Receiver Buffer Register (RBR) is equal *or* larger than the threshold level; or (2) RBR time-out occurs if the receiver buffer register has valid data and is below the threshold level. Cleared to 0 when RBR is less than threshold level after reading RBR.

IR FIFO Control Register (UFR):

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Legacy IR	RXFTL1 (MSB)	RXFTL0 (LSB)	0	0	0	TXF_RST	RXF_RST	EN_FIFO
Advanced IR	RXFTL1 (MSB)	RXFTL0 (LSB)	TXFTL1 (MSB)	TXFTL0 (LSB)	0	TXF_RST	RXF_RST	EN_FIFO
Reset Value	0	0	0	0	0	0	0	0

Legacy IR:

This register is used to control FIFO functions of the IR.

Bit 6, 7: These two bits are used to set the active level for the receiver FIFO interrupt. For example, if the interrupt active level is set as 4 bytes and there are more than 4 data characters in the receiver FIFO, the interrupt will be activated to notify CPU to read the data from FIFO.

TABLE: FIFO TRIGGER LEVEL

Bit 7	Bit 6	RX FIFO Interrupt Active Level (Bytes)
0	0	01
0	1	04
1	0	08
1	1	14

Bit 4, 5: Reserved

Bit 3: When this bit is programmed to logic 1, the DMA mode will change from mode 0 to mode 1 if UFR bit 0 = 1.

Bit 2: Setting this bit to a logical 1 resets the TX FIFO counter logic to its initial state. This bit will be cleared to logical 0 by itself after being set to logical 1.

Bit 1: Setting this bit to logical 1 resets the RX FIFO counter logic to its initial state. This bit will be cleared to a logical 0 by itself after being set to logical 1.

Bit 0: This bit enables the 16550 (FIFO) mode of the IR. This bit should be set to logical 1 before other bits of UFR can be programmed.

Advanced IR:

Bit 7, 6: **RXFTL1, 0 – Receiver FIFO Threshold Level**

Its definition is the same as Legacy IR. RXTH_I becomes 1 when the Receiver FIFO Threshold Level is equal to or larger than the defined value shown as follow.

RXFTL1, 0 (Bit 7, 6)	**RX FIFO Threshold Level (**FIFO Size: ***16-byte*****)**	**RX FIFO Threshold Level (**FIFO Size: ***32-byte*****)**
00	1	1
01	4	4
10	8	16
11	14	26

Note that the FIFO Size is selectable in SET2.Reg4.

Bit 5, 4: TXFTL1, 0 - Transmitter FIFO Threshold Level

TXTH_I (Transmitter Threshold Level Interrupt) is set to 1 when the Transmitter Threshold Level is less than the programmed value shown below.

TXFTL1, 0 (Bit 5, 4)	**TX FIFO Threshold Level (**FIFO Size: ***16-byte*****)**	**TX FIFO Threshold Level (**FIFO Size: ***32-byte*****)**
00	1	1
01	3	7
10	9	17
11	13	25

Bit 3 ~0: Same as in Legacy IR Mode

5.2.4 Set0.Reg3 - IR Control Register/Set Select Register (UCR/SSR):

These two registers share the same address. In all Register Sets, *Set Select Register (SSR)* can be programmed to select a desired Set, but IR Control Register can only be programmed in Set 0 and Set 1. In other words, writing to Reg3 in Sets other than Set 0 and Set 1 will not affect IR Control Register. The mapping of entry Set and programming value is shown below.

SSR Bits									Selected
7	6	5	4	3	2	1	0	Hex Value	Set
0	×	×	×	×	×	×	×	¡ Đ	**Set 0**
1	Any combination except those used in SET 2~7							¡ Đ	**Set1**
1	1	1	0	0	0	0	0	**0xE0**	**Set 2**
1	1	1	0	0	1	0	0	**0xE4**	**Set 3**
1	1	1	0	1	0	0	0	**0xE8**	**Set 4**
1	1	1	1	1	1	0	0	**0xEC**	**Set 5**
1	1	1	1	0	0	0	0	**0xF0**	**Set 6**
1	1	1	1	0	1	0	0	**0xF4**	**Set 7**

5.2.5 Set0.Reg4 - Handshake Control Register (HCR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	0	0	0	XLOOP	EN_IRQ	0	0	0
Advanced IR	AD_MD2	AD_MD1	AD_MD0	SIR_PLS	TX_WT	EN_DMA	0	0
Reset Value	0	1	1	0	0	0	0	0

Legacy IR Register:

This register controls the pins of IR used for handshaking with peripherals such as modem, and controls the diagnostic mode of IR.

Bit 4: When this bit is set to logical 1, the legacy IR enters diagnostic mode by an internal loopback: IRTX is forced to logical 0, and IRRX is isolated from the communication link instead of the TSR.

Bit 3: The legacy IR interrupt output is enabled via setting this bit to logic 1.

Advanced IR Register:

Bit 7~5 *Advanced SIR/ASK-IR, MIR, FIR, Remote Controller Modes:*

AD_MD2~0 - Advanced IR/Infrared Mode Select.

These registers are active when Advanced IR Select (ADV_SL, in Set2.Reg2.Bit0) is set to 1. Operational mode selection is defined as follows. When backward operation occurs, these registers will be reset to 0 and fall back to legacy IR mode.

AD_MD2~0 (Bit 7, 6, 5)	**Selected Mode**
000	Reserved
001	Low speed **MIR** (0.576M bps)
010	Advanced **ASK-IR**
011	Advanced **SIR**
100	High Speed **MIR** (1.152M bps)
101	**FIR** (4M bps)
110	**Consumer IR**
111	Reserved

Bit 4: *MIR, FIR Modes:*

SIR_PLS - Send Infrared Pulse

Writing 1 to this bit will send a 2 ms long infrared pulse after physical frame end. This is to signal to SIR that the high speed infrared is still in. This bit will be auto cleared by hardware.

Other Modes: Not used.

Bit 3: *MIR, FIR modes:*

TX_WT - Transmission Waiting

If this bit is set to 1, the transmitter will wait for TX FIFO to reach threshold level or transmitter time-out before it begins to transmit data; this prevents short queues of data bytes from transmitting prematurely. This is to avoid Underrun.

Other Modes: Not used.

Bit 2: *MIR, FIR modes:*

EN_DMA - Enable DMA

Enable DMA function for transmitting or receiving. Before using this, the DMA channel should be selected first. If only RX DMA channel is set and TX DMA channel is disabled, then the single DMA channel is used. In the single channel system, the bit of D_CHSW (DMA channel swap, in Set 2.Reg2.Bit3) will determine if it is RX_DMA or TX_DMA channel.

Other modes: Not used.

Bit 1, 0: **RTS, DTR**

Functional definitions are the same as in legacy IR mode.

5.2.6 Set0.Reg5 - IR Status Register (USR)

Mode	B7	B6	B5	B4	B3	B2	B1	B0
Legacy IR	RFEI	TSRE	TBRE	SBD	NSER	PBER	OER	RDR
Advanced IR	LB_INFR	TSRE	TBRE	MX_LEX	PHY_ERR	CRC_ERR	OER	RDR
Reset Value	0	0	0	0	0	0	0	0

Legacy IR Register: These registers are defined the same as previous description.

Advanced IR Register:

Bit 7: *MIR, FIR Modes:*

LB_INFR - Last Byte In Frame End

Set to 1 when last byte of a frame is in the bottom of FIFO. This bit separates one frame from another when RX FIFO has more than one frame.

Bit 6, 5: Same as legacy IR description.

Bit 4: *MIR, FIR modes:*

MX_LEX - Maximum Frame Length Exceed

Set to 1 when the length of a frame from the receiver has exceeded the programmed frame length defined in SET4.Reg6 and Reg5. If this bit is set to 1, the receiver will not receive any data to RX FIFO.

Bit 3: *MIR, FIR modes:*

PHY_ERR - Physical Layer Error

Set to 1 when an illegal data symbol is received. The illegal data symbol is defined in physical layer of IrDA version 1.1. When this bit is set to 1, the decoder of receiver will be aborted and a frame end signal is set to 1.

Bit 2: *MIR, FIR Modes:*

CRC_ERR - CRC Error

Set to 1 when an attached CRC is erroneous.

Bit 1, 0: **OER - Overrun Error, RDR - RBR Data Ready**

Definitions are the same as legacy IR.

5.2.7Set0.Reg6 - Reserved

Set0.Reg7 - User Defined Register (UDR/AUDR)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Legacy IR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced IR	FLC_ACT	UNDRN	RX_BSY/ RX_IP	LST_FE/ RX_PD	S_FEND	0	LB_SF	RX_TO
Reset Value	0	0	0	0	0	0	0	0

Legacy IR Register:

This is a temporary register that can be accessed and defined by the user.

Advanced IR Register:

Bit 7 *MIR, FIR Modes:*

FLC_ACT - Flow Control Active

Set to 1 when the flow control occurs. Cleared to 0 when this register is read. Note that this will be affected by Set5.Reg2 which controls the SIR mode switches to MIR/FIR mode *or* MIR/FIR mode operated in DMA function switches to SIR mode.

Bit 6 *MIR, FIR Modes:*

UNDRN - Underrun

Set to 1 when transmitter is empty *and* S_FEND (bit 3 of this register) is not set in PIO mode or no TC (Terminal Count) in DMA mode. Cleared to 0 after a write to 1.

Bit 5 *MIR, FIR Modes:*

RX_BSY - Receiver Busy

Set to 1 when receiver is busy or active in process.

Remote IR mode:

RX_IP - Receiver in Process

Set to 1 when receiver is in process.

Bit 4: *MIR, FIR modes:*

LST_FE - Lost Frame End

Set to 1 when a frame end in a entire frame is lost. Cleared to 0 when this register is read.

Remote IR Modes:

RX_PD - Receiver Pulse Detected

Set to 1 when one or more remote pulses are detected. Cleared to 0 when this register is read.

Bit 3 *MIR, FIR Modes:*

S_FEND - Set a Frame End

Set to 1 when trying to terminate the frame, that is, the procedure od PIO command is

An Entire Frame = Write Frame Data (First) + Write S_FEND (Last)

This bit should be set to 1, if used in PIO mode, to avoid transmitter underrun. Note that setting S_FEND to 1 is equivalent to TC (Terminal Count) in DMA mode. Therefore, this bit should be set to 0 in DMA mode.

Bit 2: Reserved.

Bit 1: *MIR, FIR Modes:*

LB_SF - Last Byte Stay in FIFO

A 1 in this bit indicates one or more frame ends remain in receiver FIFO.

Bit 0: *MIR, FIR, Remote IR Modes:*

RX_TO - Receiver FIFO or Frame Status FIFO time-out

Set to 1 when receiver FIFO *or* frame status FIFO time-out occurs

5.3 Set1 - Legacy Baud Rate Divisor Register

Address Offset	Register Name	Register Description
0	**BLL**	Baud Rate Divisor Latch (Low Byte)
1	**BHL**	Baud Rate Divisor Latch (High Byte)
2	**ISR/UFR**	Interrupt Status *or* IR FIFO Control Register
3	**UCR/SSR**	IR Control *or* Sets Select Register
4	**HCR**	Handshake Control Register
5	**USR**	IR Status Register
6	**HSR**	Handshake Status Register
7	**UDR/ESCR**	User Defined Register

5.3.1 Set1.Reg0~1 - Baud Rate Divisor Latch (BLL/BHL)

These two registers of BLL and BHL are baud rate divisor latch in the legacy SIR/ASK-IR mode. Accessing these registers in Advanced IR mode will cause backward operation, that is, UART will fall back to legacy SIR mode and clear some register values as shown in the following table.

Set & Register	Advanced Mode DIS_BACK=×	Legacy Mode DIS_BACK=0
Set 0.Reg 4	Bit 7~5	-
Set 2.Reg 2	Bit 0, 5, 7	Bit 5, 7
Set 4.Reg 3	Bit 2, 3	-

Note that DIS_BACK=1 (Disable Backward operation) in legacy SIR/ASK-IR mode will not affect any register which is meaningful in legacy SIR/ASK-IR.

5.3.2 Set1.Reg 2~7

These registers are defined the same as Set 0 registers.

5.4 Set2 - Interrupt Status *or* IR FIFO Control Register (ISR/UFR)

These registers are only used in advanced modes.

Address Offset	Register Name	Register Description
0	**ABLL**	Advanced Baud Rate Divisor Latch (Low Byte)
1	**ABHL**	Advanced Baud Rate Divisor Latch (High Byte)
2	**ADCR1**	Advanced IR Control Register 1
3	**SSR**	Sets Select Register
4	**ADCR2**	Advanced IR Control Register 2
5	**Reserved**	-
6	**TXFDTH**	Transmitter FIFO Depth
7	**RXFDTH**	Receiver FIFO Depth

5.4.1 Reg0, 1 - Advanced Baud Rate Divisor Latch (ABLL/ABHL)

These two registers are the same as legacy IR baud rate divisor latch in SET 1.Reg0~1. In advanced SIR/ASK-IR mode, the user should program these registers to set baud rate. This is to prevent backward operations from occurring.

5.4.2 Reg2 - Advanced IR Control Register 1 (ADCR1)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced IR	BR_OUT	-	EN_LOUT	ALOOP	D_CHSW	DMATHL	DMA_F	ADV_SL
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **BR_OUT - Baud Rate Clock Output**

When written to 1, the programmed baud rate clock will be output to DTR pin. This bit is only used to test baud rate divisor.

Bit 6: **Reserved,** write 0.

Bit 5: **EN_LOUT - Enable Loopback Output**

A write to 1 will enable transmitter to output data to IRTX pin when loopback operation occurs. Internal data can be verified through an output pin by setting this bit.

Bit 4: **ALOOP - All Mode Loopback**

A write to 1 will enable loopback in all modes.

Bit 3: **D_CHSW - DMA TX/RX Channel Swap**

If only one DMA channel operates in MIR/FIR mode, then the DMA channel can be swapped.

D_CHSW	DMA Channel Selected
0	Receiver (Default)
1	Transmitter

A write to 1 will enable output data when ALOOP=1.

Bit 2: **DMATHL - DMA Threshold Level**

Set DMA threshold level as shown in the following table.

DMATHL	TX FIFO Threshold		RX FIFO Threshold
	16-Byte	32-Byte	(16/32-Byte)
0	13	13	4
1	23	7	10

Bit 1: **DMA_F - DMA Fairness**

DMA_F	Function Description
0	DMA request (DREQ) is forced inactive after 10.5us
1	No effect DMA request.

Bit 0: **ADV_SL - Advanced Mode Select**

A write to 1 selects advanced mode.

5.4.3 Reg3 - Sets Select Register (SSR)

Reading this register returns E0H. Writing a value selects Register Set.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Refault Value	1	1	1	0	0	0	0	0

5.4.4 Reg4 - Advanced IR Control Register 2 (ADCR2)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Advanced IR	DIS_BACK	-	PR_DIV1	PR_DIV0	RX_FSZ1	RX_FSZ0	TX_FSZ1	TXFSZ0
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **DIS_BACK - Disable Backward Operation**

A write to 1 disables backward legacy IR mode. When operating in legacy SIR/ASK-IR mode, this bit should be set to 1 to avoid backward operation.

Bit 6: **Reserved,** write 0.

Bit 5, 4: **PR_DIV1~0 - Pre-Divisor 1~0.**

These bits select pre-divisor for external input clock 24M Hz. The clock goes through the pre-divisor, then input to baud rate divisor of IR.

PR_DIV1~0	Pre-divisor	Max. Baud Rate
00	13.0	**115.2K** bps
01	1.625	**921.6K** bps
10	6.5	**230.4K** bps
11	1	**1.5M** bps

Bit 3, 2: **RX_FSZ1~0 - Receiver FIFO Size 1~0**

These bits setup receiver FIFO size when FIFO is enable.

RX_FSZ1~0	RX FIFO Size
00	**16**-Byte
01	**32**-Byte
1X	Reserved

Bit 1, 0: **TX_FSZ1~0 - Transmitter FIFO Size 1~0**

These bits setup transmitter FIFO size when FIFO is enable.

TX_FSZ1~0	TX FIFO Size
00	**16**-Byte
01	**32**-Byte
1X	Reserved

TABLE: SIR Baud Rate

BAUD RATE From different Pre-divider				
Pre-Div: 13 1.8461M Hz	Pre-Div:1.625 14.769M Hz	Pre-Div: 1.0 24M Hz	Decimal divisor used to generate 16X clock	Error Percentage between desired and actual
50	400	650	**2304**	**
75	600	975	**1536**	**
110	880	1430	**1047**	0.18%
134.5	1076	1478.5	**857**	0.099%
150	1200	1950	**768**	**
300	2400	3900	**384**	**
600	4800	7800	**192**	**
1200	9600	15600	**96**	**
1800	14400	23400	**64**	**
2000	16000	26000	**58**	0.53%
2400	19200	31200	**48**	**
3600	28800	46800	**32**	**
4800	38400	62400	**24**	**
7200	57600	93600	**16**	**
9600	76800	124800	**12**	**
19200	153600	249600	**6**	**
38400	307200	499200	**3**	**
57600	460800	748800	**2**	**
115200	921600	1497600	**1**	**

** The percentage error for all baud rates, except where indicated otherwise, is 0.16%.

5.4.5 Reg6 - Transmitter FIFO Depth (TXFDTH) (Read Only)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced IR	0	0	TXFD5	TXFD4	TXFD3	TXFD2	TXFD1	TXFD1
Reset Value	0	0	0	0	0	0	0	0

Bit 7~6: **Reserved,** Read 0.

Bit 5~0: Reading these bits returns the current transmitter FIFO depth, that is, the number of bytes left in the transmitter FIFO.

5.4.6 Reg7 - Receiver FIFO Depth (RXFDTH) (Read Only)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced IR	0	0	RXFD5	RXFD4	RXFD3	RXFD2	RXFD1	RXFD1
Reset Value	0	0	0	0	0	0	0	0

Bit 7~6: **Reserved,** Read 0.

Bit 5~0: Reading these bits returns the current receiver FIFO depth, that is, the number of bytes left in the receiver FIFO.

5.5 Set3 - Version ID *and* Mapped Control Registers

Address Offset	Register Name	Register Description
0	**AUID**	Advanced IR ID
1	**MP_UCR**	Mapped IR Control Register
2	**MP_UFR**	Mapped IR FIFO Control Register
3	**SSR**	Sets Select Register
4	**Reversed**	-
5	**Reserved**	-
6	**Reserved**	-
7	**Reserved**	-

5.5.1 Reg0 - Advanced IR ID (AUID)

This register is read only. It stores advanced IR version ID. Reading it returns 1XH.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	0	0	0	1	X	X	X	X

5.5.2 Reg1 - Mapped IR Control Register (MP_UCR)

This register is read only. Reading this register returns IR Control Register value of Set 0.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	0	0	0	0	0	0	0	0

5.5.3 Reg2 - Mapped IR FIFO Control Register (MP_UFR)

This register is read only. Reading this register returns IR FIFO Control Register (UFR) value of SET 0.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	0	0	0	0	0	0	0	0

5.5.4 Reg3 - Sets Select Register (SSR)

Reading this register returns E4H. Writing a value selects a Register Set.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	0	0	1	0	0

5.6 Set4 - TX/RX/Timer counter registers *and* IR control registers.

Address Offset	Register Name	Register Description
0	**TMRL**	Timer Value Low Byte
1	**TMRH**	Timer Value High Byte
2	**IR_MSL**	Infrared Mode Select
3	**SSR**	Sets Select Register
4	**TFRLL**	Transmitter Frame Length Low Byte
5	**TFRLH**	Transmitter Frame Length High Byte
6	**RFRLL**	Receiver Frame Length Low Byte
7	**RFRLH**	Receiver Frame Length High Byte

5.6.1 Set4.Reg0, 1 - Timer Value Register (TMRL/TMRH)

This is a 12-bit timer whose resolution is 1ms, that is, the maximum programmable time is 2^{12}-1 ms. The timer is a down-counter and starts counting down when EN_TMR (Enable Timer) of Set4.Reg2 is set to 1. When the timer counts down to *zero* and EN_TMR=1, the TMR_I is set to 1 and a new initial value will be loaded into counter.

5.6.2 Set4.Reg2 - Infrared Mode Select (IR_MSL)

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Advanced IR	-	-	-	-	IR_MSL1	IR_MSL0	TMR_TST	EN_TMR
Reset Value	0	0	0	0	0	0	0	0

Bit 7~4: **Reserved**, write to 0.

Bit 3, 2: **IR_MSL1, 0 - Infrared Mode Select**

Select legacy IR, SIR, or ASK-IR mode. Note that in legacy SIR/ASK-IR user should set DIS_BACK=1 to avoid backward when programming baud rate.

IR_MSL1, 0	Operation Mode Selected
00	Legacy **IR**
01	CIR
10	Legacy **ASK-IR**
11	Legacy **SIR**

Bit 1: **TMR_TST - Timer Test**

When set to 1, reading the TMRL/TMRH returns the programmed values of TMRL/TMRH instead of the value of down counter. This bit is for testing timer register.

Bit 0: **EN_TMR - Enable Timer**

A write to 1 will enable the timer.

5.6.3 Set4.Reg3 - Set Select Register (SSR)

Reading this register returns E8H. Writing this register selects Register Set.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	1	1	0	0	0

5.6.4 Set4.Reg4, 5 - Transmitter Frame Length (TFRLL/TFRLH)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TFRLL	bit 7	bit 6	bit 5	bit 4	bit3	bit 2	bit 1	bit 0
Reset Value	0	0	0	0	0	0	0	0
TFRLH	-	-	-	bit 12	bit 11	bit 10	bit 9	bit 8
Reset Value	-	-	-	0	0	0	0	0

These are combined to be a 13-bit register. Writing these registers programs the transmitter frame length of a package. These registers are only valid when APM=1 (automatic package mode, Set5.Reg4.bit5). When APM=1, the physical layer will split data stream to a programmed frame length if the transmitted data is larger than the programmed frame length. When these registers are read, they will return the number of bytes which is not transmitted from a frame length programmed.

5.6.5 Set4.Reg6, 7 - Receiver Frame Length (RFRLL/RFRLH)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFRLL	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Reset Value	0	0	0	0	0	0	0	0
RFRLH	-	-	-	bit 12	bit 11	bit 10	bit 9	bit 8
Reset Value	-	-	-	0	0	0	0	0

These are combined to be a 13-bit register and up counter. The length of receiver frame will be limited to the programmed frame length. If the received frame length is larger than the programmed receiver frame length, the bit of MX_LEX (Maximum Length Exceed) will be set to 1. Simultaneously, the receiver will not receive any more data to RX FIFO until the next start flag of the next frame, which is defined in the physical layer IrDA 1.1. Reading these registers returns the number of received data bytes of a frame from the receiver.

5.7 Set 5 - Flow control *and* IR control *and* Frame Status FIFO registers

Address Offset	Register Name	Register Description
0	FCBLL	Flow Control Baud Rate Divisor Latch Register (Low Byte)
1	FCBHL	Flow Control Baud Rate Divisor Latch Register (High Byte)
2	FC_MD	Flow Control Mode Operation
3	SSR	Sets Select Register
4	IRCFG1	Infrared Configure Register
5	FS_FO	Frame Status FIFO Register
6	RFRLFL	Receiver Frame Length FIFO Low Byte
7	RFRLFH	Receiver Frame Length FIFO High Byte

5.7.1 Set5.Reg0, 1 - Flow Control Baud Rate Divisor Latch Register (FCDLL/ FCDHL)

If flow control is enforced when UART switches mode from MIR/FIR to SIR, then the pre-programmed baud rate of FCBLL/FCBHL are loaded into advanced baud rate divisor latch (ADBLL/ADBHL).

5.7.2 Set5.Reg2 - Flow Control Mode Operation (FC_MD)

These registers control flow control mode operation as shown in the following table.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FC_MD	FC_MD2	FC_MD1	FC_MD0	-	FC_DSW	EN_FD	EN_BRFC	EN_FC

Reset Value	0	0	0	0	0	0	0	0

Bit 7~5 **FC_MD2 - Flow Control Mode**

When flow control is enforced, these bits will be loaded into AD_MD2~0 of advanced HSR (Handshake Status Register). These three bits are defined as same as AD_MD2~0.

Bit 4: **Reserved**, write 0.

Bit 3: **FC_DSW - Flow Control DMA Channel Swap**

A write to 1 allows user to swap DMA channel for transmitter or receiver when flow control is enforced.

FC_DSW	Next Mode After Flow Control Occurred
0	Receiver Channel
1	Transmitter Channel

Bit 2: **EN_FD - Enable Flow DMA Control**

A write to 1 enables UART to use DMA channel when flow control is enforced.

Bit 1: **EN_BRFC - Enable Baud Rate Flow Control**

A write to 1 enables FC_BLL/FC_BHL (Flow Control Baud Rate Divider Latch, in Set5.Reg1~0) to be loaded into advanced baud rate divisor latch (ADBLL/ADBHL, in Set2.Reg1~0).

Bit 0: **EN_FC - Enable Flow Control**

A write to 1 enables flow control function and bit 7~1 of this register.

5.7.3 Set5.Reg3 - Sets Select Register (SSR)

Writing this register selects Register Set. Reading this register returns ECH.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	0	1	1	0	0

5.7.4 Set5.Reg4 - Infrared Configure Register 1 (IRCFG1)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRCFG1	-	FSF_TH	FEND_M	AUX_RX	-	-	IRHSSL	IR_FULL
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved**, write 0.

Bit 6: **FSF_TH - Frame Status FIFO Threshold**

Set this bit to determine the frame status FIFO threshold level and to generate the FSF_I. The threshold level values are defined as follows.

FSF_TH	Status FIFO Threshold Level
0	2
1	4

Bit 5: **FEND_MD - Frame End Mode**

A write to 1 enables hardware to split data stream into equal length frame automatically as defined in Set4.Reg4 and Set4.Reg5, i.e., TFRLL/TFRLH.

Bit 4: **AUX_RX - Auxiliary Receiver Pin**

A write to 1 selects IRRX input pin. (Refer to Set7.Reg7.Bit5)

Bit 3~2: **Reserved**, write 0.

Bit 1: **IRHSSL - Infrared Handshake Status Select**

When set to 0, the HSR (Handshake Status Register) operates the same as defined in IR mode. A write to 1 will disable HSR, and reading HSR returns 30H.

Bit 0: **IR_FULL - Infrared Full Duplex Operation**

When set to 0, IR module operates in half duplex. A write to 1 makes IR module operate in full duplex.

5.7.5 Set5.Reg5 - Frame Status FIFO Register (FS_FO)

This register shows the bottom byte of frame status FIFO.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FS_FO	FSFDR	LST_FR	-	MX_LEX	PHY_ERR	CRC_ERR	RX_OV	FSF_OV
Reset Value	0	0	0	0	0	0	0	0

Bit 7: **FSFDR - Frame Status FIFO Data Ready**

Indicates that a data byte is valid in frame status FIFO bottom.

Bit 6: **LST_FR - Lost Frame**

Set to 1 when one or more frames have been lost.

Bit 5: **Reserved**.

Bit 4: **MX_LEX - Maximum Frame Length Exceed**

Set to 1 when incoming data exceeds programmed maximum frame length defined in Set4.Reg6 and Set4.Reg7. This bit is in frame status FIFO bottom and is valid only when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 3: **PHY_ERR - Physical Error**

When receiving data, any physical layer error as defined in IrDA 1.1 will set this bit to 1. This bit is in frame status FIFO bottom and is valid only when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 2: **CRC_ERR - CRC Error**

Set to 1 when a bad CRC is received in a frame. This CRC belongs to physical layer as defined in IrDA 1.1. This bit is in frame status FIFO bottom and is valid only when FSFDR=1 (Frame Status FIFO Data Ready).

Bit 1: **RX_OV - Received Data Overrun**

Set to 1 when receiver FIFO overruns.

Bit 0: **FSF_OV - Frame Status FIFO Overrun**

Set to 1 When frame status FIFO overruns.

5.7.6 Set5.Reg6, 7 - Receiver Frame Length FIFO (RFLFL/RFLFH) or Lost Frame Number (LST_NU)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFLFL/ LST_NU	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset Value	0	0	0	0	0	0	0	0
RFLFH	-	-	-	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset Value	0	0	0	0	0	0	0	0

Receiver Frame Length FIFO (RFLFL/RFLFH):

These are combined to be a 13-bit register. Reading these registers returns received byte count for the frame. When read, the register of *RFLFH* will pop-up another frame status and frame length if FSFDR=1 (Set5.Reg4.Bit7).

Lost Frame Number (LST_NU):

When LST_FR=1 (Set5.Reg4.Bit6), Reg6 stands for LST_NU which is a 8-bit register holding the number of frames lost in succession.

5.8 Set6 - IR Physical Layer Control Registers

Address Offset	Register Name	Register Description
0	**IR_CFG2**	Infrared Configure Register 2
1	**MIR_PW**	MIR (1.152M bps or 0.576M bps) Pulse Width
2	**SIR_PW**	SIR Pulse Width
3	**SSR**	Sets Select Register
4	**HIR_FNU**	High Speed Infrared Flag Number
5	**IR_ID1**	IR ID Register 1
6	IR_ID2	IR ID Register 2
7	HIR_SL	High Speed infrared Select Register

5.8.1 Set6.Reg0 - Infrared Configure Register 2 (IR_CFG2)

This register controls ASK-IR, MIR, FIR operations.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IR_CFG2	SHMD_N	SHDM_N	FIR_CRC	MIR_CRC	-	INV_CRC	DIS_CRC	-
Reset Value	0	0	1	0	0	0	0	0

Bit 7: **SHMD_N - ASK-IR Modulation Disable**

SHMD_N	Modulation Mode
0	IRTX modulate 500K Hz Square Wave
1	Re-rout IRTX

Bit 6: **SHDM_N - ASK-IR Demodulation Disable**

SHDM_N	Demodulation Mode
0	Demodulation 500K Hz
1	Re-rout IRRX

Bit 5: **FIR_CRC - FIR (4M bps) CRC Type**

FIR_CRC	CRC Type
0	16-bit CRC
1	32-bit CRC

Note that the 16/32-bit CRC are defined in IrDA 1.1 physical layer.

Bit 4: **MIR_CRC - MIR (1.152M/0.576M bps) CRC Type**

MIR_CRC	CRC Type
0	16-bit CRC
1	32-bit CRC

Bit 2: **INV_CRC - Inverting CRC**

When set to 1, the CRC is inversely output in physical layer.

Bit 1: **DIS_CRC - Disable CRC**

When set to 1, the transmitter does not transmit CRC in physical layer.

Bit 0: **Reserved**, write 1.

5.8.2 Set6.Reg1 - MIR (1.152M/0.576M bps) Pulse Width

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MIR_PW	-	-	-	M_PW4	M_PW3	M_PW2	M_PW1	M_PW0
Reset Value	0	0	0	0	1	0	1	0

This 5-bit register sets MIR output pulse width.

M_PW4~0	MIR Pulse Width (1.152M bps)	MIR Output Width (0.576M bps)
00000	**0** ns	**0** ns
00001	**20.83** ns	**41.66** ns
00010	**41.66** (==20.83*2) ns	**83.32** (==41.66*2) ns
...	**...**	**...**
k_{10}	**20.83*** k_{10} ns	**41.66*** k_{10} ns
...	**...**	**...**
11111	**645** ns	**1290** ns

5.8.3 Set6.Reg2 - SIR Pulse Width

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SIR_PW	-	-	-	S_PW4	S_PW3	S_PW2	S_PW1	S_PW0
Reset Value	0	0	0	0	0	0	0	0

This 5-bit register sets SIR output pulse width.

S_PW4~0	SIR Output Pulse Width
00000	**3/16 bit time** of IR
01101	**1.6** us
Others	**1.6** us

5.8.4 Set6.Reg3 - Set Select Register

Select Register Set by writing a set number to this register. Reading this register returns F0H.

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	SSR7	SSR6	SSR5	SSR4	SSR3	SSR2	SRR1	SRR0
Default Value	1	1	1	1	0	0	0	0

5.8.5 Set6.Reg4 - High Speed Infrared Beginning Flag Number (HIR_FNU)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HIR_FNU	M_FG3	M_FG2	M_FG1	M_FG0	F_FL3	F_FL2	F_FL1	F_FL0
Reset Value	0	0	1	0	1	0	1	0

Bit 7~4: **M_FG3~0 - MIR beginning Flag Number**

These bits define the number of transmitter *Start Flag* of MIR. Note that the number of MIR start flag should be equal or more than *two* which is defined in IrDA 1.1 physical layer. The default value is 2.

M_FG3~0	Beginning Flag Number	M_FG3~0	Beginning Flag Number
0000	Reserved	**1000**	10
0001	1	**1001**	12
0010	**2** (Default)	**1010**	16
0011	3	**1011**	20
0100	4	**1100**	24
0101	5	**1101**	28
0110	6	**1110**	32
0111	8	**1111**	Reserved

Bit 3~0: **F_FG3~0 - FIR Beginning Flag Number**

These bits define the number of transmitter *Preamble Flag* in FIR. Note that the number of FIR start flag should be equal to *sixteen* which is defined in IrDA 1.1 physical layer. The default value is 16.

M_FG3~0	Beginning Flag Number	M_FG3~0	Beginning Flag Number
0000	Reserved	**1000**	10
0001	1	**1001**	12
0010	2	**1010**	**16** (Default)
0011	3	**1011**	20
0100	4	**1100**	24
0101	5	**1101**	28
0110	6	**1110**	32
0111	8	**1111**	Reserved

5.8.6 Set6.Reg5 – Winbond infrared ID Register 1

Bit 7~0: **Winbond infrared ID1. Default value is 0x5C. Ready only.**

5.8.7 Set6.Reg6 – Winbond infrared ID Register 2

Bit 7~0: **Winbond infrared ID2. Default value is 0XA3. Ready only.**

5.8.8 Set6.Reg7 – High Speed infrared ID Select Register

Bit 7-4: **Reserve.**

Bit 3-2: **IRSEL0_IRRXH Pin Function select**

Bit 3-2	IRSEL0_IRRXH Pin function
00	IRRXH FUNCTION
01	IRSEL0 FUNCTION(Default value)

Bit 1-0: **Reserve.**

5.9 Set7 - Remote control and IR module selection registers

Address Offset	Register Name	Register Description
0	**RIR_RXC**	Remote Infrared Receiver Control
1	**RIR_TXC**	Remote Infrared Transmitter Control
2	**RIR_CFG**	Remote Infrared Config Register
3	**SSR**	Sets Select Register
4	**IRM_SL1**	Infrared Module (Front End) Select 1
5	**IRM_SL2**	Infrared Module Select 2
6	**IRM_SL3**	Infrared Module Select 3
7	**IRM_CR**	Infrared Module Control Register

5.9.1 Set7.Reg0 - Remote Infrared Receiver Control (RIR_RXC)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIR_RXC	RX_FR2	RX_FR1	RX_FR0	RX_FSL4	RX_FSL3	RX_FSL2	RX_FSL1	RX_FSL0
Default Value	0	0	1	0	1	0	0	1

This register defines frequency range of receiver of remote IR.

Bit 7~5: **RX_FR2~0 - Receiver Frequency Range 2~0.**

These bits select the input frequency range of the receiver. It is implemented through a band pass filter, i.e., only the input signals whose frequency lies in the range defined in this register will be received.

Bit 4~0: **RX_FSL4~0 - Receiver Frequency Select 4~0.**

Selects the operation frequency of receiver.

Table: Low Frequency range select of receiver.

	RX_FR2~0 (Low Frequency)					
	001		010		011	
RX_FSL4~0	Min.	Max.	Min.	Max.	Min.	Max.
00010	26.1	29.6	24.7	31.7	23.4	34.2
00011	28.2	32.0	26.7	34.3	25.3	36.9
00100	29.4	33.3	27.8	35.7	26.3	38.4
00101	30.0	34.0	28.4	36.5	26.9	39.3
00110	31.4	35.6	29.6	38.1	28.1	41.0
00111	32.1	36.4	30.3	39.0	28.7	42.0
01000	32.8	37.2	31.0	39.8	29.4	42.9
01001	***33.6****	***38.1****	31.7	40.8	30.1	44.0
01011	34.4	39.0	32.5	41.8	30.8	45.0
01100	36.2	41.0	34.2	44.0	32.4	47.3
01101	37.2	42.1	35.1	45.1	33.2	48.6
01111	38.2	43.2	36.0	46.3	34.1	49.9
10000	40.3	45.7	38.1	49.0	36.1	52n.7
10010	41.5	47.1	39.2	50.4	37.2	54.3
10011	42.8	48.5	40.4	51.9	38.3	56.0
10101	44.1	50.0	41.7	53.6	39.5	57.7
10111	45.5	51.6	43.0	55.3	40.7	59.6
11010	48.7	55.2	46.0	59.1	43.6	63.7
11011	50.4	57.1	47.6	61.2	45.1	65.9
11101	54.3	61.5	51.3	65.9	48.6	71.0

Note that those unassigned combinations are reserved.

Table: High Frequency range select of receiver

	RX_FR2~0 (High Frequency)	
	001	
RX_FSL4~0	Min.	Max.
00011	355.6	457.1
01000	380.1	489.8
01011	410.3	527.4

Note that those unassigned combinations are reserved.

Table: SHARP ASK-IR receiver frequency range select.

RX_FSL4~0 (SHARP ASK-IR)						
RX_FR2~0	001	010	011	100	101	110

-	***480.0****	***533.3****	457.1	564.7	436.4	600.0	417.4	640.0	400.0	685.6	384.0	738.5

Note that those unassigned combinations are reserved.

5.9.2 Set7.Reg1 - Remote Infrared Transmitter Control (RIR_TXC)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIR_TXC	TX_PW2	TX_PW1	TX_PW0	TX_FSL4	TX_FSL3	TX_FSL2	TX_FSL1	TX_FSL0
Default Value	0	1	1	0	1	0	0	1

This Register defines the transmitter frequency and pulse width of remote IR.

Bit 7~5: **TX_PW2~0 - Transmitter Pulse Width 2~ 0.**

Select the transmission pulse width.

TX_PW2~0	Low Frequency	High Frequency
010	6 ms	0.7 ms
011	7 ms	0.8 ms
100	9 ms	0.9 ms
101	10.6 ms	1.0 ms

Note that those unassigned combinations are reserved.

Bit 4~0: **TX_FSL4~0 - Transmitter Frequency Select 4~0.**

Select the transmission frequency.

Table: Low frequency selected.

TX_FSL4~0	Low Frequency
00011	30K Hz
00100	31K HZ
...	...
11101	56K Hz

Note that those unassigned combinations are reserved.

Table: High frequency selected.

TX_FSL4~0	High Frequency
00011	400K Hz
01000	450K Hz
01011	480K Hz

Note that those unassigned combinations are reserved.

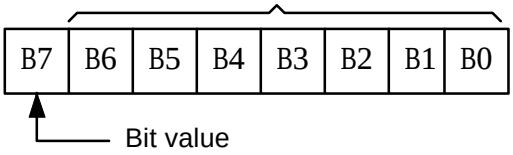
5.9.3 Set7.Reg2 - Remote Infrared Config Register (RIR_CFG)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RIR_CFG	P_PNB	SMP_M	RXCFS	-	TX_CFS	RX_DM	TX_MM1	TX_MM0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **P_PNB: Programming Pulse Number Coding.**

Write a 1 to select programming pulse number coding. The code format is defined as follows.

(Number of bits) - 1



If the bit value is set to 0, the high pulse will be transmitted/received. If the bit value is set to 1, then no energy will be transmitted/received.

Bit 6: **SMP_M - Sampling Mode.**

To select receiver sampling mode.

When set to 0 then uses T-period sampling, that the T-period is programmed IR baud rate.

When set to 1, programmed baud rate will be used to do oversampling.

Bit 5: **RXCFS - Receiver Carry Frequency Select**

RXCFS	Selected Frequency
0	30K ~ 56K Hz
1	400K ~ 480K Hz

Bit 4: **Reserved,** write 0.

Bit 3: **TX_CFS - Transmitter Carry Frequency Select.**

Select low speed or high speed transmitter carry frequency.

TX_FCS	Selected Frequency
0	30K ~ 56K Hz
1	400K ~ 480K Hz

Bit 2: **RX_DM - Receiver Demodulation Mode.**

RX_DM	Demodulation Mode
0	Enable internal decoder
1	Disable internal decoder

Bit 1~0: **TX_MM1~0 - Transmitter Modulation Mode 1~0**

TX_MM1~0	TX Modulation Mode
00	Continuously send pulse for logic 0
01	**8 pulses** for logic 0 and no pulse for logic 1.
10	**6 pulses** for logic 0 and no pulse for logic 1
11	Reserved.

5.9.4 Set7.Reg3 - Sets Select Register (SSR)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SSR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Default Value	1	1	1	1	0	1	0	0

Reading this register returns F4H. Select Register Set by writing a set number to this register.

5.9.5 Set7.Reg4 - Infrared Module (Front End) Select 1 (IRM_SL1)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_SL1	IR_MSP	SIR_SL2	SIR_SL1	SIR_SL0	-	AIR_SL2	AIR_SL1	AIR_SL0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **IR_MSP - IR Mode Select Pulse**

When set to 1, the transmitter (IRTX) will send a 64 ms pulse to setup a special IR front-end operational mode. When IR front-end module uses *mode select pin (MD)* and *transmitter IR pulse (IRTX)* to switch between high speed IR (such as FIR or MIR) and low speed IR (SIR or ASK-IR), this bit should be used.

Bit 6~4: **SIR_SL2~0 - SIR (Serial IR) mode select.**

These bits are used to program the operational mode of the SIR front-end module. These values of SIR_SL2~0 will be automatically loaded to pins of IR_SL2~0, respectively, when (1) AM_FMT=1 (Automatic Format, in Set7.Reg7.Bit7); (2) the mode of Advanced IR is set to SIR (AD_MD2~0, in Set0.Reg4.Bit7~0).

Bit 3: **Reserved,** write 0.

Bit 2~0: **AIR_SL2~0 - ASK-IR Mode Select.**

These bits setup the operational mode of ASK-IR front-end module when AM_FMT=1 and AD_MD2~0 are configured to ASK-IR mode. These values will be automatically loaded to IR_SL2~0, respectively.

5.9.6 Set7.Reg5 - Infrared Module (Front End) Select 2 (IRM_SL2)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_SL2	-	FIR_SL2	FIR_SL1	FIR_SL0	-	MIR_SL2	MIR_SL1	MIR_SL0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved,** write 0.

Bit 6~4: **FIR_SL2~0 - FIR mode select.**

These bits setup the operational mode of FIR front-end module when AM_FMT=1 and AD_MD2~0 are configured to FIR mode. These values will be automatically loaded to IR_SL2~0, respectively.

Bit 3: **Reserved,** write 0.

Bit 2~0: **MIR_SL2~0 - MIR Mode Select.**

These bits setup the MIR operational mode when AM_FMT=1 *and* AD_MD2~0 are configured to MIR mode. These values will be automatically loaded to IR_SL2~0, respectively.

5.9.7 Set7.Reg6 - Infrared Module (Front End) Select 3 (IRM_SL3)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_SL3	-	LRC_SL2	LRC_SL1	LRC_SL0	-	HRC_SL2	HRC_SL1	HRC_SL0
Default Value	0	0	0	0	0	0	0	0

Bit 7: **Reserved,** write 0.

Bit 6~4: **LRC_SL2~0 - Low Speed Remote IR mode select.**

These bits setup the operational mode of *low speed* remote IR front-end module when AM_FMT=1 and AD_MD2~0 are configured to Remote IR mode. These values will be automatically loaded to IR_SL2~0, respectively.

Bit 3: **Reserved,** write 0.

Bit 2~0: **HRC_SL2~0 - High Speed Remote IR Mode Select.**

These bits setup the operational mode of *high speed* remote IR front-end module when AM_FMT=1 and .AD_MD2~0 are configured to Remote IR mode. These values will be automatically loaded to IR_SL2~0, respectively.

5.9.8 Set7.Reg7 - Infrared Module Control Register (IRM_CR)

Reg.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRM_CR	AM_FMT	IRX_MSL	IRSL0D	RXINV	TXINV	-	-	-
Default Value	0	0	0	0	0	0	0	0

Bit 7: **AM_FMT - Automatic Format**

A write to 1 will enable automatic format IR front-end module. These bits will affect the output of IR_SL2~0 which is referred by IR front-end module selection (Set7.Reg4~6)

Bit 6: **IRX_MSL - IR Receiver Module Select**

Select the receiver input path from the IR front end module if IR module has a separated high speed and low speed receiver path. If the IR module has only one receiving path, then this bit should be set to 0.

IRX_MSL	Receiver Pin selected
0	IRRX (Low/High Speed)
1	IRRXH (High Speed)

Bit 5: **IRSL0D - Direction of IRSL0 Pin**

Select function for IRRXH or IRSL0 because they share common pin and have different input/output direction.

IRSL0_D	Function
0	IRRXH (I/P)
1	IRSL0 (O/P)

Table: IR receiver input pin selection

IRSL0D	IRX_MSL	AUX_RX	High Speed IR	Selected IR Pin
0	0	0	X	**IRRX**
0	0	1	X	**IRRXH**
0	1	X	0	**IRRX**
0	1	X	1	**IRRXH**
1	0	0	X	**IRRX**
1	0	1	X	Reserved
1	1	X	0	**IRRX**
1	1	X	1	Reserved

Note: that (1) AUX_RX is defined in Set5.Reg4.Bit4, (2) high speed IR includes MIR (1.152M or 0.576M bps) and FIR (4M bps), (3) IRRX is the input of the low speed or high speed IR receiver, IRRXH is the input of the high speed IR receiver.

Bit 4: **RXINV - Receiving Signal Invert**

A write to 1 will Invert the receiving signal.

Bit 3: **TXINV - Transmitting Signal Invert**

A write to 1 will Invert the transmitting signal.

Bit 2~0: **Reserved,** write 0.

6. PARALLEL PORT

6.1 Printer Interface Logic

The parallel port of the W83L517D makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL level. The W83L517D supports an IBM XT/AT compatible parallel port (SPP), bi-directional parallel port (BPP), Enhanced Parallel Port (EPP), Extended Capabilities Parallel Port (ECP), Extension FDD mode (EXTFDD), Extension 2FDD mode (EXT2FDD) on the parallel port. Refer to the configuration registers for more information on disabling, power-down, and on selecting the mode of operation. Table 6-1 shows the pin definitions for different modes of the parallel port.

TABLE 6-1-1 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

HOST CONNECTOR	Pin Number of W83627HF	PIN ATTRIBUTE	SPP	EPP	ECP
1	36	O	nSTB	nWrite	nSTB, HostClk[2]
2-9	31-26, 24-23	I/O	PD<0:7>	PD<0:7>	PD<0:7>
10	22	I	nACK	Intr	nACK, PeriphClk[2]
11	21	I	BUSY	nWait	BUSY, PeriphAck[2]
12	19	I	PE	PE	PEerror, nAckReverse[2]
13	18	I	SLCT	Select	SLCT, Xflag[2]
14	35	O	nAFD	nDStrb	nAFD, HostAck[2]
15	34	I	nERR	nError	nFault[1], nPeriphRequest[2]
16	33	O	nINIT	nInit	nINIT[1], nReverseRqst[2]
17	32	O	nSLIN	nAStrb	nSLIN[1] , ECPMode[2]

Notes:

n<name > : Active Low

1. Compatible Mode

2. High Speed Mode

3. For more information, refer to the IEEE 1284 standard.

TABLE 6-1-2 PARALLEL PORT CONNECTOR AND PIN DEFINITIONS

Host Connector	Pin Number of W83627HF	Pin Attribute	SPP	Pin Attribute	EXT2FDD	Pin Attribute	EXTFDD
1	36	O	nSTB	---	---	---	---
2	31	I/O	PD0	I	INDEX2#	I	INDEX2#
3	30	I/O	PD1	I	TRAK02#	I	TRAK02#
4	29	I/O	PD2	I	WP2#	I	WP2#
5	28	I/O	PD3	I	RDATA2#	I	RDATA2#
6	27	I/O	PD4	I	DSKCHG2#	I	DSKCHG2#
7	26	I/O	PD5	---	---	---	---
8	24	I/O	PD6	OD	MOA2#	---	---
9	23	I/O	PD7	OD	DSA2#	---	---
10	22	I	nACK	OD	DSB2#	OD	DSB2#
11	21	I	BUSY	OD	MOB2#	OD	MOB2#
12	19	I	PE	OD	WD2#	OD	WD2#
13	18	I	SLCT	OD	WE2#	OD	WE2#
14	35	O	nAFD	OD	RWC2#	OD	RWC2#
15	34	I	nERR	OD	HEAD2#	OD	HEAD2#
16	33	O	nINIT	OD	DIR2#	OD	DIR2#
17	32	O	nSLIN	OD	STEP2#	OD	STEP2#

6.2 Enhanced Parallel Port (EPP)

TABLE 6-2 PRINTER MODE AND EPP REGISTER ADDRESS

A2	A1	A0	REGISTER	NOTE
0	0	0	Data port (R/W)	1
0	0	1	Printer status buffer (Read)	1
0	1	0	Printer control latch (Write)	1
0	1	0	Printer control swapper (Read)	1
0	1	1	EPP address port (R/W)	2
1	0	0	EPP data port 0 (R/W)	2
1	0	1	EPP data port 1 (R/W)	2
1	1	0	EPP data port 2 (R/W)	2
1	1	1	EPP data port 2 (R/W)	2

Notes:

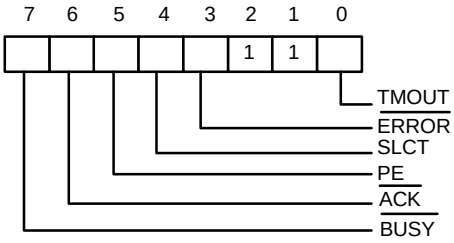
1. These registers are available in all modes.
2. These registers are available only in EPP mode.

6.2.1 Data Swapper

The system microprocessor can read the contents of the printer's data latch by reading the data swapper.

6.2.2 Printer Status Buffer

The system microprocessor can read the printer status by reading the address of the printer status buffer. The bit definitions are as follows:



Bit 7: This signal is active during data entry, when the printer is off-line during printing, when the print head is changing position, or during an error state. When this signal is active, the printer is busy and cannot accept data.

Bit 6: This bit represents the current state of the printer's ACK# signal. A 0 means the printer has received a character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before BUSY# stops.

Bit 5: Logical 1 means the printer has detected the end of paper.

Bit 4: Logical 1 means the printer is selected.

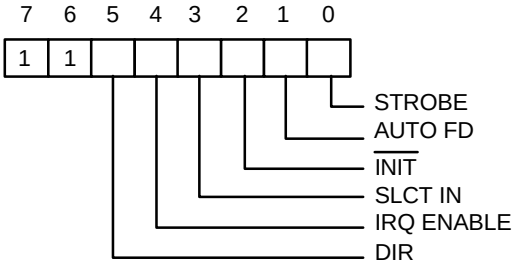
Bit 3: Logical 0 means the printer has encountered an error condition.

Bit 1, 2: These two bits are not implemented and are logic one during a read of the status register.

Bit 0: This bit is valid in EPP mode only. It indicates that a 10 μS time-out has occurred on the EPP bus. A logic 0 means that no time-out error has occurred; a logic 1 means that a time-out error has been detected. Writing a logic 1 to this bit will clear the time-out status bit; writing a logic 0 has no effect.

6.2.3 Printer Control Latch and Printer Control Swapper

The system microprocessor can read the contents of the printer control latch by reading the printer control swapper. Bit definitions are as follows:



Bit 7, 6: These two bits are a logic one during a read. They can be written.

Bit 5: Direction control bit

When this bit is a logic 1, the parallel port is in input mode (read); when it is a logic 0, the parallel port is in output mode (write). This bit can be read and written. In SPP mode, this bit is invalid and fixed at zero.

Bit 4: A 1 in this position allows an interrupt to occur when ACK# changes from low to high.

Bit 3: A 1 in this bit position selects the printer.

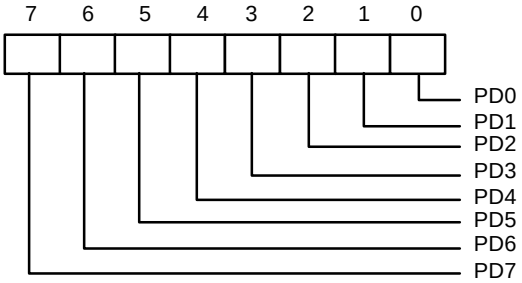
Bit 2: A 0 starts the printer (50 microsecond pulse, minimum).

Bit 1: A 1 causes the printer to line-feed after a line is printed.

Bit 0: A 0.5 microsecond minimum high active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microseconds before and after the strobe pulse.

6.2.4 EPP Address Port

The address port is available only in EPP mode. Bit definitions are as follows:

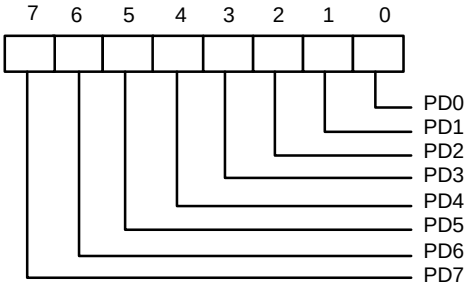


The contents of DB0-DB7 are buffered (non-inverting) and output to ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP address write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

PD0-PD7 ports are read during a read operation. The leading edge of IOR# causes an EPP address read cycle to be performed and the data to be output to the host CPU.

6.2.5 EPP Data Port 0-3

These four registers are available only in EPP mode. Bit definitions of each data port are as follows:



When accesses are made to any EPP data port, the contents of DB0-DB7 are buffered (non-inverting) and output to the ports PD0-PD7 during a write operation. The leading edge of IOW# causes an EPP data write cycle to be performed, and the trailing edge of IOW# latches the data for the duration of the EPP write cycle.

During a read operation, ports PD0-PD7 are read, and the leading edge of IOR# causes an EPP read cycle to be performed and the data to be output to the host CPU.

6.2.6 Bit Map of Parallel Port and EPP Registers

REGISTER	7	6	5	4	3	2	1	0
Data Port (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Status Buffer (Read)	BUSY#	ACK#	PE	SLCT	ERROF#	1	1	TMOUT
Control Swapper (Read)	1	1	1	IRQEN	SLIN	INIT#	AUTOFD#	STROBE#
Control Latch (Write)	1	1	DIR	IRQ	SLIN	INIT#	AUTOFD#	STROBE#
EPP Address Port R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 0 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 1 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 2 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EPP Data Port 3 (R/W)	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

6.2.7 EPP Pin Descriptions

EPP NAME	TYPE	EPP DESCRIPTION
nWrite	O	Denotes an address or data read or write operation.
PD<0:7>	I/O	Bi-directional EPP address and data bus.
Intr	I	Used by peripheral device to interrupt the host.
nWait	I	Inactive to acknowledge that data transfer is completed. Active to indicate that the device is ready for the next transfer.
PE	I	Paper end; same as SPP mode.
Select	I	Printer selected status; same as SPP mode.
nDStrb	O	This signal is active low. It denotes a data read or write operation.
nError	I	Error; same as SPP mode.
NInits	O	This signal is active low. When it is active, the EPP device is reset to its initial operating mode.
nAStrb	O	This signal is active low. It denotes an address read or write operation.

6.2.8 EPP Operation

When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. The PDx bus is in the standard or bi-directional mode when no EPP read, write, or address cycle is currently being executed. In this condition all output signals are set by the SPP Control Port and the direction is controlled by DIR of the Control Port.

A watchdog timer is required to prevent system lockup. The timer indicates that more than 10 μS have elapsed from the start of the EPP cycle to the time WAIT# is deasserted. The current EPP cycle is aborted when a time-out occurs. The time-out condition is indicated in Status bit 0.

6.2.8.1 EPP Operation

The EPP operates on a two-phase cycle. First, the host selects the register within the device for subsequent operations. Second, the host performs a series of read and/or write byte operations to the selected register. Four operations are supported on the EPP: Address Write, Data Write, Address Read, and Data Read. All operations on the EPP device are performed asynchronously.

6.2.8.2 EPP Version 1.9 Operation

The EPP read/write operation can be completed under the following conditions:

a. If the nWait is active low, when the read cycle (nWrite inactive high, nDStrb/nAStrb active low) or write cycle (nWrite active low, nDStrb/nAStrb active low) starts, the read/write cycle proceeds normally and will be completed when nWait goes inactive high.

b. If nWait is inactive high, the read/write cycle will not start. It must wait until nWait changes to active low, at which time it will start as described above.

6.2.8.3 EPP Version 1.7 Operation

The EPP read/write cycle can start without checking whether nWait is active or inactive. Once the read/write cycle starts, however, it will not terminate until nWait changes from active low to inactive high.

6.3 Extended Capabilities Parallel (ECP) Port

This port is software and hardware compatible with existing parallel ports, so it may be used as a standard printer mode if ECP is not required. It provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward (host to peripheral) and reverse (peripheral to host) directions.

Small FIFOs are used in both forward and reverse directions to improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes. The ECP port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The ECP port supports run-length-encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Hardware support for compression is optional.

For more information about the ECP Protocol, refer to the Extended Capabilities Port Protocol and ISA Interface Standard.

6.3.1 ECP Register and Mode Definitions

NAME	ADDRESS	I/O	ECP MODES	FUNCTION
data	Base+000h	R/W	000-001	Data Register
ecpAFifo	Base+000h	R/W	011	ECP FIFO (Address)
dsr	Base+001h	R	All	Status Register
dcr	Base+002h	R/W	All	Control Register
cFifo	Base+400h	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base+400h	R/W	011	ECP FIFO (DATA)
tFifo	Base+400h	R/W	110	Test FIFO
cnfgA	Base+400h	R	111	Configuration Register A
cnfgB	Base+401h	R/W	111	Configuration Register B
ecr	Base+402h	R/W	All	Extended Control Register

Note: The base addresses are specified by CR23, which are determined by configuration register or hardware setting.

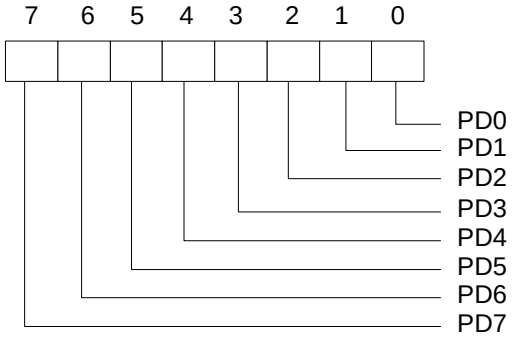
MODE	DESCRIPTION
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the CR9 and CR0 to select ECP/EPP mode)
101	Reserved
110	Test mode
111	Configuration mode

Note: The mode selection bits are bit 7-5 of the Extended Control Register.

6.3.2 Data and ecpAFifo Port

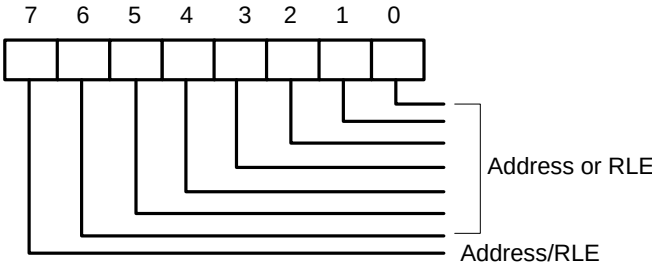
Modes 000 (SPP) and 001 (PS/2) (Data Port)

During a write operation, the Data Register latches the contents of the data bus on the rising edge of the input. The contents of this register are output to the PD0-PD7 ports. During a read operation, ports PD0-PD7 are read and output to the host. The bit definitions are as follows:



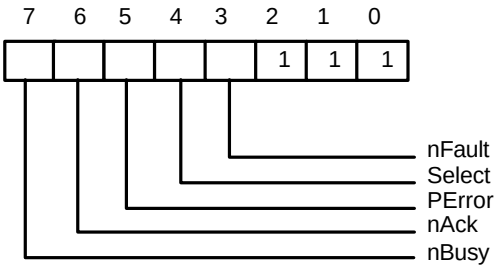
Mode 011 (ECP FIFO-Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is defined only for the forward direction. The bit definitions are as follows:



6.3.3 Device Status Register (DSR)

These bits are at low level during a read of the Printer Status Register. The bits of this status register are defined as follows:



Bit 7: This bit reflects the complement of the Busy input.

Bit 6: This bit reflects the nAck input.

Bit 5: This bit reflects the PError input.

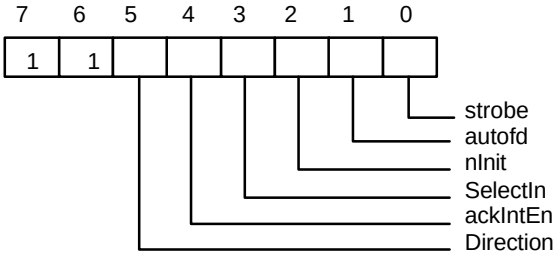
Bit 4: This bit reflects the Select input.

Bit 3: This bit reflects the nFault input.

Bit 2-0: These three bits are not implemented and are always logic one during a read.

6.3.4 Device Control Register (DCR)

The bit definitions are as follows:



Bit 6, 7: These two bits are logic one during a read and cannot be written.

Bit 5: This bit has no effect and the direction is always out if mode = 000 or mode = 010. Direction is valid in all other modes.

0 the parallel port is in output mode.

1 the parallel port is in input mode.

Bit 4: Interrupt request enable. When this bit is set to a high level, it may be used to enable interrupt requests from the parallel port to the CPU due to a low to high transition on the ACK# input.

Bit 3: This bit is inverted and output to the SLIN# output.

0 The printer is not selected.

1 The printer is selected.

Bit 2: This bit is output to the INIT# output.

Bit 1: This bit is inverted and output to the AFD# output.

Bit 0: This bit is inverted and output to the STB# output.

6.3.5 cFifo (Parallel Port Data FIFO) Mode = 010

This mode is defined only for the forward direction. The standard parallel port's protocol is used by a hardware handshake to the peripheral to transmit bytes written or DMAed from the system to this FIFO. Transfers to the FIFO are byte aligned.

6.3.6 ecpDFifo (ECP Data FIFO) Mode = 011

When the direction bit is 0, bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

When the direction bit is 1, data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

6.3.7 tFifo (Test FIFO Mode) Mode = 110

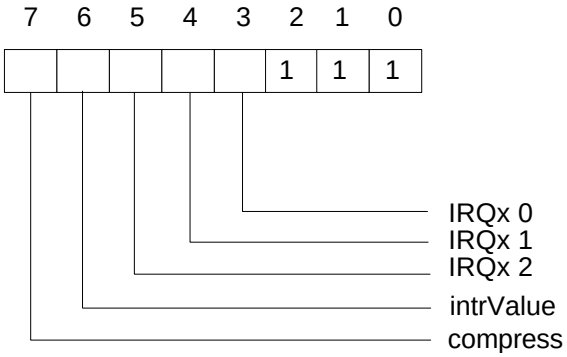
Data bytes may be read, written, or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the parallel port lines. However, data in the tFIFO may be displayed on the parallel port data lines.

6.3.8 cnfgA (Configuration Register A) Mode = 111

This register is a read-only register. When it is read, 10H is returned. This indicates to the system that this is an 8-bit implementation.

6.3.9 cnfgB (Configuration Register B) Mode = 111

The bit definitions are as follows:



Bit 7: This bit is read-only. It is at low level during a read. This means that this chip does not support hardware RLE compression.

Bit 6: Returns the value on the ISA IRQ line to determine possible conflicts.

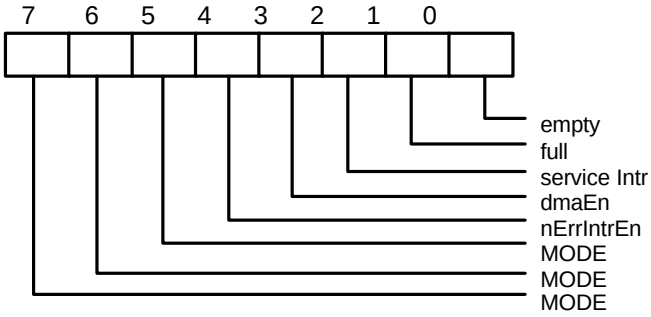
Bit 5-3: Reflect the IRQ resource assigned for ECP port.

cnfgB[5:3]	IRQ resource
000	reflect other IRQ resources selected by PnP register (default)
001	IRQ7
010	IRQ9
011	IRQ10
100	IRQ11
101	IRQ14
110	IRQ15
111	IRQ5

Bit 2-0: These five bits are at high level during a read and can be written.

6.3.10 ECR (Extended Control Register) Mode = all

This register controls the extended ECP parallel port functions. The bit definitions are follows:



Bit 7-5: These bits are read/write and select the mode.

000	Standard Parallel Port mode. The FIFO is reset in this mode.
001	PS/2 Parallel Port mode. This is the same as 000 except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register.
010	Parallel Port FIFO mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data are automatically transmitted using the standard parallel port protocol. This mode is useful only when direction is 0.
011	ECP Parallel Port Mode. When the direction is 0 (forward direction), bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and auto transmitted to the peripheral using ECP Protocol. When the direction is 1 (reverse direction), bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo.
100	Selects EPP Mode. In this mode, EPP is activated if the EPP mode is selected.
101	Reserved.
110	Test Mode. The FIFO may be written and read in this mode, but the data will not be transmitted on the parallel port.

111 Configuration Mode. The confgA and confgB registers are accessible at 0x400 and 0x401 in this mode.

Bit 4: Read/Write (Valid only in ECP Mode)

1 Disables the interrupt generated on the asserting edge of nFault.

0 Enables an interrupt pulse on the high to low edge of nFault. If nFault is asserted (interrupt) an interrupt will be generated and this bit is written from a 1 to 0.

Bit 3: Read/Write

1 Enables DMA.

0 Disables DMA unconditionally.

Bit 2: Read/Write

1 Disables DMA and all of the service interrupts.

0 Enables one of the following cases of interrupts. When one of the service interrupts has occurred, the serviceIntr bit is set to a 1 by hardware. This bit must be reset to 0 to re-enable the interrupts. Writing a 1 to this bit will not cause an interrupt.

(a) dmaEn = 1: During DMA this bit is set to a 1 when terminal count is reached.

(b) dmaEn = 0 direction = 0: This bit is set to 1 whenever there are writeIntr Threshold or more bytes free in the FIFO.

(c) dmaEn = 0 direction = 1: This bit is set to 1 whenever there are readIntr Threshold or more valid bytes to be read from the FIFO.

Bit 1: Read only

0 The FIFO has at least 1 free byte.

1 The FIFO cannot accept another byte or the FIFO is completely full.

Bit 0: Read only

0 The FIFO contains at least 1 byte of data.

1 The FIFO is completely empty.

6.3.11 Bit Map of ECP Port Registers

	D7	D6	D5	D4	D3	D2	D1	D0	Note
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
Dsr	nBusy	nAck	PError	Select	nFault	1	1	1	1
Dcr	1	1	Directio	ackIntEn	SelectIn	nInit	autofd	strobe	1
Cfifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
Tfifo	Test FIFO								2
CnfgA	0	0	0	1	0	0	0	0	
CnfgB	compress	intrValue	1	1	1	1	1	1	
Ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Notes:
1. These registers are available in all modes.
2. All FIFOs use one common 16-byte FIFO.

6.3.12 ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe (HostClk)	O	The nStrobe registers data or address into the slave on the asserting edge during write operations. This signal handshakes with Busy.
PD<7:0>	I/O	These signals contains address or data or RLE data.
nAck (PeriphClk)	I	This signal indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
Busy (PeriphAck)	I	This signal deasserts to indicate that the peripheral can accept data. It indicates whether the data lines contain ECP command information or data in the reverse direction. When in reverse direction, normal data are transferred when Busy (PeriphAck) is high and an 8-bit command is transferred when it is low.
PError (nAckReverse)	I	This signal is used to acknowledge a change in the direction of the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select (Xflag)	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when it is asserted. This signal indicates whether the data lines contain ECP address or data in the forward direction. When in forward direction, normal data are transferred when nAutoFd (HostAck) is high and an 8-bit command is transferred when it is low.
nFault (nPeriphRequest)	I	Generates an error interrupt when it is asserted. This signal is valid only in the forward direction. The peripheral is permitted (but not required) to drive this pin low to request a reverse transfer during ECP Mode.
nInit (nReverseRequest)	O	This signal sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction.
nSelectIn (ECPMode)	O	This signal is always deasserted in ECP mode.

6.3.13 ECP Operation

The host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol before ECP operation. After negotiation, it is necessary to initialize some of the port bits. The following are required:

(a) Set direction = 0, enabling the drivers.

(b) Set strobe = 0, causing the nStrobe signal to default to the deasserted state.

(c) Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.

(d) Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo, respectively.

6.3.13.1 Mode Switching

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (mode 011 or 010).

If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can be changed only in mode 001.

When in extended forward mode, the software should wait for the FIFO to be empty before switching back to mode 000 or 001. In ECP reverse mode the software waits for all the data to be read from the FIFO before changing back to mode 000 or 001.

6.3.13.2 Command/Data

ECP mode allows the transfer of normal 8-bit data or 8-bit commands. In the forward direction, normal data are transferred when HostAck is high and an 8-bit command is transferred when HostAck is low. The most significant bits of the command indicate whether it is a run-length count (for compression) or a channel address.

In the reverse direction, normal data are transferred when PeriphAck is high and an 8-bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero.

6.3.13.3 Data Compression

The W83627HF supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Note that the odd (RLE) compression in hardware is not supported. In order to transfer data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

6.3.14 FIFO Operation

The FIFO threshold is set in configuration register 5. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode, as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. After a reset, the FIFO is disabled.

6.3.15 DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo, or CFifo. The DMA uses the standard PC DMA services. The ECP requests DMA transfers from the host by activating the PDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, which will disable the DMA.

6.3.16 Programmed I/O (NON-DMA) Mode

The ECP or parallel port FIFOs can also be operated using interrupt driven programmed I/O. Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. The host must set the direction, state, dmaEn = 0 and serviceIntr = 0 in the programmed I/O transfers.

The ECP requests programmed I/O transfers from the host by activating the IRQ pin. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

6.4 Extension FDD Mode (EXTFDD)

In this mode, the W83627HF changes the printer interface pins to FDC input/output pins, allowing the user to install a second floppy disk drive (FDD B) through the DB-25 printer connector. The pin assignments for the FDC input/output pins are shown in Table 6-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins MOB# and DSB# will be forced to inactive state.

(2) Pins DSKCHG#, RDATA#, WP#, TRAK0#, INDEX# will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXTFDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

6.5 Extension 2FDD Mode (EXT2FDD)

In this mode, the W83627HF changes the printer interface pins to FDC input/output pins, allowing the user to install two external floppy disk drives through the DB-25 printer connector to replace internal floppy disk drives A and B. The pin assignments for the FDC input/output pins are shown in Table6-1.

After the printer interface is set to EXTFDD mode, the following occur:

(1) Pins MOA#, DSA#, MOB#, and DSB# will be forced to inactive state.

(2) Pins DSKCHG#, RDATA#, WP#, TRAK0#, and INDEX# will be logically ORed with pins PD4-PD0 to serve as input signals to the FDC.

(3) Pins PD4-PD0 each will have an internal resistor of about 1K ohm to serve as pull-up resistor for FDD open drain/collector output.

(4) If the parallel port is set to EXT2FDD mode after the system has booted DOS or another operating system, a warm reset is needed to enable the system to recognize the extension floppy drive.

7. General Purpose I/O

W83L517D provides 38 input/output ports that can be individually configured to perform a simple basic I/O function or a pre-defined alternate function. Those 38 GP I/O ports are divided into five groups, each group contains 6,8,8,8,8 ports from group 1 to group 5. The first group is configured through control registers in logical device 7, the second group in logical device 8,the third ,the fourth,and the fifth group in logical device 9. Users can configure each individual port to be an input or output port by programming respective bit in selection register (CRF0: 0 = output, 1 = input). Invert port value by setting inversion register (CRF2: 0 = non-inverse, 1 = inverse). Port value is read/written through data register (CRF1). Table 7.1 and 7.2 gives more details on GPIO's assignment. In addition, GPIO1 is designed to be functional even in power loss condition (VCC or VSB is off). Figure 7.1 shows the GP I/O port's structure. Right after Power-on reset, those ports default to perform basic input function except ports in GPIO1 which maintains its previous settings until a battery loss condition.

Table 7.1

SELECTION Bit 0 = output 1 = input	INVERSION bit 0 = non inverSE 1 = inverSE	basic i/o operations
0	0	Basic non-inverting output
0	1	Basic inverting output
1	0	Basic non-inverting input
1	1	Basic inverting input

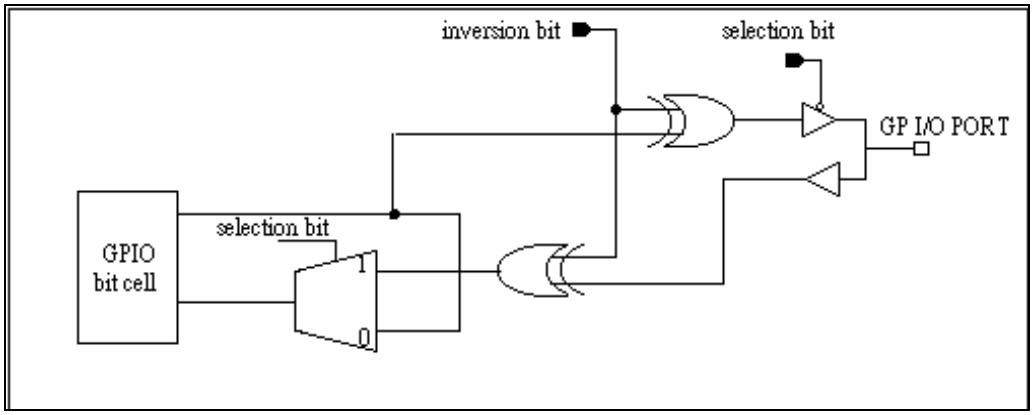
Table 7.2

GPIO port data register	register bit ASSIGNMENT	GP i/o port
GP1	BIT 0	GP10
	BIT 1	GP11
	BIT 2	GP12
	BIT 3	GP13
	BIT 4	GP14
	BIT 5	GP15
GP2	BIT 0	GP20
	BIT 1	GP21
	BIT 2	GP22
	BIT 3	GP23
	BIT 4	GP24
	BIT 5	GP25
	BIT 6	GP26
	BIT 7	GP27
GP3	BIT 0	GP30
	BIT 1	GP31
	BIT 2	GP32
	BIT 3	GP33
	BIT 4	GP34
	BIT 5	GP35
	BIT 6	GP36
	BIT 7	GP37

Table 7.2, continued

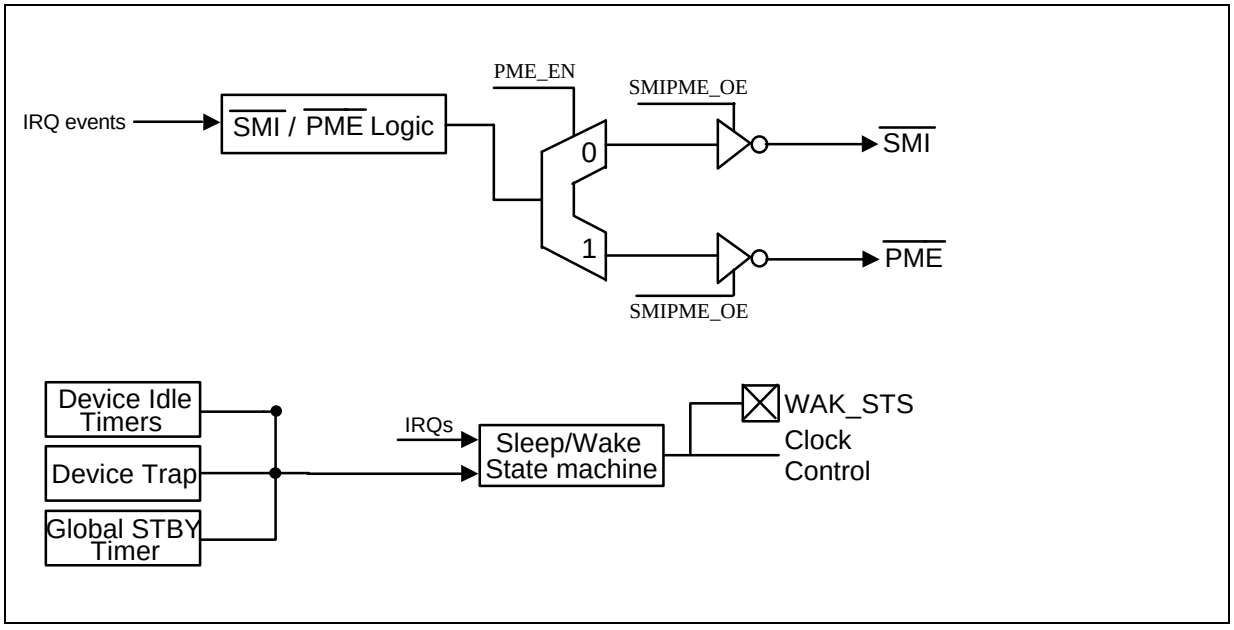
GPIO port data register	register bit ASSIGNMENT	GP i/o port
GP4	BIT 0	GP40
	BIT 1	GP41
	BIT 2	GP42
	BIT 3	GP43
	BIT 4	GP44
	BIT 5	GP45
	BIT 6	GP46
	BIT 7	GP47
GP5	BIT 0	GP50
	BIT 1	GP51
	BIT 2	GP52
	BIT 3	GP53
	BIT 4	GP54
	BIT 5	GP55
	BIT 6	GP56
	BIT 7	GP57

Figure 7.1



8. ACPI Registers Features

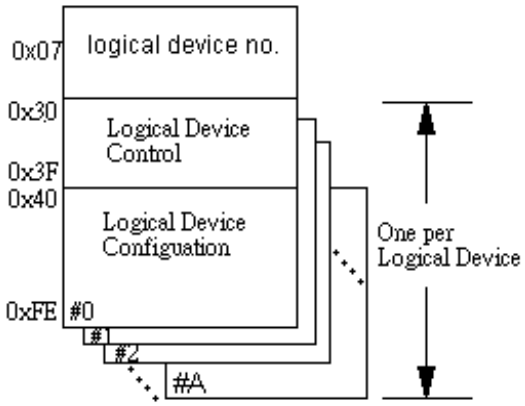
W83L517D supports both ACPI and legacy power managements. The switch logic of the power management block generates an $\overline{SMI}$ interrupt in the legacy mode and an $\overline{PME}$ interrupt in the ACPI mode. The new ACPI feature routes $\overline{SMI}$/$\overline{PME}$ logic output either to $\overline{SMI}$ or to $\overline{PME}$. The $\overline{SMI}$/$\overline{PME}$ logic routes to $\overline{SMI}$ only when both PME_EN = 0 and SMIPME_OE = 1. Similarly, the $\overline{SMI}$/$\overline{PME}$ logic routes to $\overline{PME}$ only when both PME_EN = 1 and SMIPME_OE = 1.



9. CONFIGURATION REGISTER

9.1 Plug and Play Configuration

The W83L517D uses Compatible PNP protocol to access configuration registers for setting up different types of configurations. In W83L517D, there are eleven Logical Devices (from Logical Device 0 to Logical Device B with the exception of logical device 4 for backward compatibility) which correspond to eleven individual functions: FDC (logical device 0), PRT (logical device 1), UART1 (logical device 2), FIR (Fast IR, logical device 6), GPIO1 (logical device 7), GPIO2(logical device 8),GPIO3 ~GPIO5(logical device 9), and ACPI ((logical device A). Each Logical Device has its own configuration registers (above CR30). Host can access those registers by writing an appropriate logical device number into logical device select register at CR07.



9.2 Compatible PnP

9.2.1 Extended Function Registers

In Compatible PnP, there are two ways to enter Extended Function and read or write the configuration registers. HEFRAS (CR26 bit 6) can be used to select one out of these two methods of entering the Extended Function mode as follows:

HEFRAS	address and value
0	write 87h to the location 2Eh twice
1	write 87h to the location 4Eh twice

After Power-on reset, the value on RTSA# (pin 49) is latched by HEFRAS of CR26. In Compatible PnP, a specific value (87h) must be written twice to the Extended Functions Enable Register (I/O port address 2Eh or 4Eh). Secondly, an index value (02h, 07h-FFh) must be written to the Extended Functions Index Register (I/O port address 2Eh or 4Eh same as Extended Functions Enable Register) to identify which configuration register is to be accessed. The designer can then access the desired configuration register through the Extended Functions Data Register (I/O port address 2Fh or 4Fh).

After programming of the configuration register is finished, an additional value (AAh) should be written to EFERs to exit the Extended Function mode to prevent unintentional access to those configuration registers. The designer can also set bit 5 of CR26 (LOCKREG) to high to protect the configuration registers against accidental accesses.

The configuration registers can be reset to their default or hardware settings only by a cold reset (pin MR = 1). A warm reset will not affect the configuration registers.

9.2.2 Extended Functions Enable Registers (EFERs)

After a power-on reset, the W83L517D enters the default operating mode. Before the W83L517D enters the extended function mode, a specific value must be programmed into the Extended Function Enable Register (EFER) so that the extended function register can be accessed. The Extended Function Enable Registers are write-only registers. On a PC/AT system, their port addresses are 2Eh or 4Eh (as described in previous section).

9.2.3 Extended Function Index Registers (EFIRs), Extended Function Data Registers(EFDRs)

After the extended function mode is entered, the Extended Function Index Register (EFIR) must be loaded with an index value (02h, 07h-FEh) to access Configuration Register 0 (CR0), Configuration Register 7 (CR07) to Configuration Register FE (CRFE), and so forth through the Extended Function Data Register (EFDR). The EFIRs are write-only registers with port address 2Eh or 4Eh (as described in section 12.2.1) on PC/AT systems; the EFDRs are read/write registers with port address 2Fh or 4Fh (as described in section 9.2.1) on PC/AT systems.

9.3 Configuration Sequence

To program W83L517D configuration registers, the following configuration sequence must be followed:

(1). Enter the extended function mode

(2). Configure the configuration registers

(3). Exit the extended function mode

9.3.1 Terminology

I/F : Interface.

Default : The default value of the register after power-on.

'XXXXb' : Indicates the value in binary notation.

'XXXXh' : Indicates the value in hexadecimal notation.

'XsXXb' : The 's' indicates the bit value is setting by power-on strapping.

9.3.2 Enter the extended function mode

To place the chip into the extended function mode, two successive wrtites of 0x87 must be applied to Extended Function Enable Registers (EFERs, i.e. 2Eh or 4Eh).

9.3.3 Configure the configuration registers

The chip selects the logical device and activates the desired logical devices through Extended Function Index Register (EFIR) and Extended Function Data Register(EFDR). EFIR is located at the same address as EFER, and EFDR is located at address (EFIR+1).
First, write the Logical Device Number (i.e.,0x07h) to the EFIR and then write the number of the desired logical device to the EFDR. If accessing the Chip(Global) Control Registers, this step is not required.
Secondly, write the address of the desired configuration register within the logical device to the EFIR and then write (or read) the desired configuration register through EFDR.

9.3.4 Exit the extended function mode

To exit the extended function mode, one write of 0xAAh to EFER is required. Once the chip exits the extended function mode, it is in the normal running mode and is ready to enter the configuration mode.

9.3.5 Software programming example

The following example is written in Intel 8086 assembly language. It assumes that the EFER is located at 2Eh, so EFIR is located at 2Eh and EFDR is located at 2Fh. If HEFRAS (CR26 bit 6) is set, 4Eh can be directly replaced by 4Eh and 2Fh replaced by 4Fh.

```
;--------------------------------------------------------------------------------
; Enter the extended function mode ,interruptible double-write    |
;--------------------------------------------------------------------------------
MOV    DX,2EH
MOV    AL,87H
OUT    DX,AL
OUT    DX,AL
;--------------------------------------------------------------------------
; Configure logical device 1, configuration register CRF0   |
;--------------------------------------------------------------------------
MOV    DX,2EH
MOV    AL,07H
OUT    DX,AL           ; point to Logical Device Number Reg.
MOV    DX,2FH
MOV    AL,01H
OUT    DX,AL           ; select logical device 1
;
MOV    DX,2EH
MOV    AL,F0H
OUT    DX,AL           ; select CRF0
MOV    DX,2FH
MOV    AL,3CH
OUT    DX,AL           ; update CRF0 with value 3CH
;-----------------------------------------
; Exit extended function mode     |
;-----------------------------------------
MOV    DX,2EH
MOV    AL,AAH
OUT    DX,AL
```

9.4 Chip (Global) Control Register

CR02 (Default 0x00h)

Bit 7 - 1: Reserved.

Bit 0: SWRST --> Soft Reset.

CR07

The register is used to switch each logical device when write the number of logical device to EFDRs.

Bit 7 - 0: LDNB7 - LDNB0 --> Logical Device Number Bit 7 - 0

CR20 (Default 0x61h)

Bit 7 - 0: DEVIDB7 - DEBIDB0 --> Device ID Bit 7 - Bit 0 = 0x 61 (read only).

CR21 (Default 0x0X)

Bit 7 - 0: DEVREVB7 - DEBREVB0 --> Device Rev = 0x 0**X** (read only).

X : Version change number .(Bit 3~0).

CR22 (Default 0xFFh)

Bit 7~ 5: Reserved.

Bit 4: Flash I/F Power down

= 0 Power down

= 1 No Power down

Bit 3: FIRPWD

= 0 Power down

= 1 No Power down

Bit 2: URAPWD

= 0 Power down

= 1 No Power down

Bit 1: PRTPWD

= 0 Power down

= 1 No Power down

Bit 0: FDCPWD

= 0 Power down

= 1 No Power down

CR23 (Default 0x00h)

Bit 7: GPIO 5X Output Mode Selection.

= 0. When on inactive situation, each signal of GPIO 5X will be open-drain.

= 1. When on inactive situation, each signal of GPIO 5X will be 5V CMOS structure.

Bit 6: GPIO 4X Output Mode Selection.

= 0. Each signal of GPIO 4X will be open-drain.

= 1. Each signal of GPIO 4X will be 5V CMOS structure.

Bit 5: GPIO 3X Output Mode Selection.

= 0. When on inactive situation, each signal of GPIO 3X will be open-drain.

= 1. When on inactive situation, each signal of GPIO 3X will be 5V CMOS structure.

Bit 4: GPIO 2X Output Mode Selection.

= 0. When on inactive situation, each signal of GPIO 2X will be open-drain.

= 1. When on inactive situation, each signal of GPIO 2X will be 5V CMOS structure.

Bit 3: GPIO 1X Output Mode Selection.

= 0. When on inactive situation, each signal of GPIO 1X will be open-drain.

= 1. When on inactive situation, each signal of GPIO 1X will be 5V CMOS structure.

Bit 2: Flash ROM I/F Address Segment (000F0000h – 000FFFFFh) Enable.

= 0 Enable (Default).

= 1 Disable.

Bit 1: Flash ROM I/F Address Segment (000E0000h – 000EFFFFh) Enable.

= 0 Enable (Default).

= 1 Disable.

Bit 0: IPD (Immediate Power Down). When set to 1, it will put the whole chip into power down mode immediately.

CR24 (Default ss00,00ssb)

Bit 7 : Keyboard address decoder control

= 0 Enable keyboard address (interface: KBCS# and MCCS#) decoder and IRQ1 , IRQ12 pass to SERIRQ.

= 1 Disable keyboard interface.

The corresponding power-on setting pin is PENKBC# (pin 52)

Bit 6: CLKSEL(Enable 48Mhz)

= 0 The clock input on Pin 1 should be 24 MHz.

= 1 The clock input on Pin 1 should be 48 MHz.

The corresponding power-on setting pin is PEN48 (pin 61).

Bit[5:4]: ROM size select

= 00 1Mb

01 2Mb

10 4Mb

11 Reserved

Bit3:MEMW# Select (PIN97)

= 0 MEMW# of flash interface is Disabled.

= 1 MEMW# of flash interface is Enabled.

Bit2: Reserved.

Bit1 : Enable Flash ROM Interface

= 0 Flash ROM Interface is enabled after hardware reset

= 1 Flash ROM Interface is disabled after hardware reset

This bit is read only, and set/reset by power-on setting pin. The corresponding power-on setting pin is PENROM#(pin 69)

Bit 0: PNPCSV

= 0 The Compatible PnP address select registers have default values.

= 1 The Compatible PnP address select registers have no default value.

The corresponding power-on setting pin is PNPCSV# (pin 43).

CR25 (Default 0x00h)

Bit 7 ~ 4: Reserved

Bit 3: FIRTRI

When write to “1” ,FIR interface is set to tri-state and reduce the power consumption of chip.

Bit 2: URATRI

When write to “1”, UART interface is set to tri-state and reduce the power consumption of chip.

Bit 1: PRTTRI

When write to “1”, PRT interface is set to tri-state and reduce the power consumption of chip.

Bit 0: FDCTRI.

When write to “1”,FDC interface is set to tri-state and reduce the power consumption of chip.

CR26 (Default 0s00,000b)

Bit 7: Reserved

Bit 6: HEFRAS

These two bits define how to enable Configuration mode. The corresponding power-on setting pin is RTSA# (pin 42).

HEFRAS Address and Value

= 0 Write 87h to the location 2E twice.

= 1 Write 87h to the location 4Etwice.

Bit 5: LOCKREG

= 0 Enable R/W Configuration Registers.

= 1 Disable R/W Configuration Registers.

Bit 4: Reserved.

Bit 3: DSFDLGRQ

= 0 Enable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is effective on selecting IRQ

= 1 Disable FDC legacy mode on IRQ and DRQ selection, then DO register bit 3 is not effective on selecting IRQ

Bit 2: DSPRLGRQ

= 0 Enable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is effective on selecting IRQ

= 1 Disable PRT legacy mode on IRQ and DRQ selection, then DCR bit 4 is not effective on selecting IRQ

Bit 1: DSUALGRQ

= 0 Enable UART A legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART A legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

Bit 0: DSUBLGRQ

= 0 Enable UART B legacy mode IRQ selecting, then MCR bit 3 is effective on selecting IRQ

= 1 Disable UART B legacy mode IRQ selecting, then MCR bit 3 is not effective on selecting IRQ

CR28 (Default 0000,0sssb)

Bit 7 : PRT_NFDD#

= 0 Enable PRT_NFDD# Function.(Default)

= 1 Disable PRT_NFDD# Function.

Bit 6 - 3: Reserved.

Bit 2 - 0: PRTMODS2 - PRTMODS0

= 0xx Parallel Port Mode

= 100 Reserved

= 101 External FDC Mode

= 110 Reserved

= 111 External two FDC Mode

When bit 7 = 0 , the bit 2 is controlled by Pin PRT_NFDD#.

CR29 (GPIO10,GP11 Select ,Default 0sss,s000b)

Bit 7: Reserved.

Bit [6:5] : Pin 5 Func. Select

= 00 GP11

= 01 WDTO

= 10 RTCCS#

= 11 IRQIN1

Bit[4:3] : Pin 4 Func. Select

= 00 GP10

= 01 PLED

= 10 P80CS#

= 11 IRQIN0

Bit2~0: Reserved

CR2A (GPIO1 ~ 5& FlashROM Interface Selected, Default ssss,ssssb)

Bit 7~5 : Reserved

Bit 4 : (PIN 81 ~ 84 ,PIN 86 ~ 89)

= 0 GPIO 5X

= 1 Flash I/F (XA11 ~ XA18)

Bit 3 : (PIN 73 ~80)

= 0 GPIO 4X

= 1 Flash I/F (XA3 ~ XA10)

Bit 2 : (PIN 57 ~ 59, PIN 61 ~ 64 , PIN 66)

= 0 GPIO 3X

= 1 Flash I/F (XD7 ~ XD0)

Bit 1 : (PIN 71 ~72)

= 0 GPIO 2X

= 1 or CR24 bit7 =0 the Pin 71 ~ 72 is Flash I/F (XA1 ~ XA0)

Bit 0: (PIN 67 ~ 70)

= 0 GPIO1X

= 1 Flash I/F(MEMR#, MEMW#, ROMCS#, XA0)

This bits is set to 1 if Pin 45 is set to 0 during RESET Period.

CR2B (POWER DOWN CONTROL

Default s000,0000b)

Bit 7 :

= 0 Normal operation

= 1 Enable Power down mode (Active with

bit[2..0] are all set to “1”)

Bit 6 –3 : Reserved

Bit 2 : Enable Flash interface Power-down

= 0 Normal operation

= 1 Flash interface is in power-down mode if CR2B bit 7 =1 or PDCTL# = 0)

Bit 1 : Enable SERIRQ interface Power-down

= 0 Normal operation

= 1 SERIRQ interface is in power-down mode if CR2B bit 7 =1 or PDCTL# = 0)

Bit 0 : Enable FDC,UR, FIR ,PRT interface Power-down

= 0 Normal operation

= 1 FDC, UR, FIR, PRT interface is in power-down mode if CR2B bit 7 =1 or PDCTL# = 0

CR2C , CR2D , CR2E FOR WINBOND TEST Reserved.

CR2C (Default 0x10h)

bit 7 – 5 : Reserved

bit 4-0 : Fresh interface Cycle time control .

9.5 Logical Device 0 (FDC)

CR30 (Default 0x01h if PNPCSV = 0 during POR, 0x00h otherwise)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03, 0xF0h if PNPCSV = 0 during POR, Default 0x00h, 0x00h otherwise)

These two registers select FDC I/O base address [0x100:0xFF8] on 8 byte boundary.

CR70 (Default 0x06 if PNPCSV = 0 during POR, 0x00h otherwise)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for FDC.

CR74 (Default 0x02 if PNPCSV = 0 during POR, 0x04h otherwise)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for FDC.

= 0x00h DMA0

= 0x01h DMA1

= 0x02h DMA2

= 0x03h DMA3

= 0x04h - 0x07h No DMA active

CRF0 (Default 0x0Eh)

FDD Mode Register

Bit 7: FIPURDWN

This bit controls the internal pull-up resistors of the FDC input pins RDATA, INDEX, TRAK0, DSKCHG, and WP.

= 0 The internal pull-up resistors of FDC are turned on.(Default)

= 1 The internal pull-up resistors of FDC are turned off.

Bit 6: INTVERTZ,This bit determines the polarity of all FDD interface signals.

= 0 FDD interface signals are active low.

= 1 FDD interface signals are active high.

Bit 5: DRV2EN (PS2 mode only)

When this bit is a logic 0, indicates a second drive is installed and is reflected in status register A.

Bit 4: Swap Drive 0, 1 Mode

= 0 No Swap (Default)

= 1 Drive and Motor select 0 and 1 are swapped.

Bit 3 - 2 Interface Mode

= 11b AT Mode (Default)

= 10b (Reserved)

= 01b PS/2

= 00b Model 30

Bit 1: FDC DMA Mode

= 0 Burst Mode is enabled

= 1 Non-Burst Mode (Default)

Bit 0: Floppy Mode

= 0 Normal Floppy Mode (Default)

= 1 Enhanced 3-mode FDD

CRF1 (Default 0x00h)

Bit 7 - 6: Boot Floppy

= 00b FDD A

= 01b FDD B

= 10b FDD C

= 11b FDD D

Bit 5, 4: Media ID1, Media ID0. These bits will be reflected on FDC's Tape Drive Register bit 7, 6.

Bit 3 - 2: Density Select

= 00b Normal (Default)

= 01b Normal

= 10b 1 (Forced to logic 1)

= 11b 0 (Forced to logic 0)

Bit 1: DISFDDWR

= 0 Enable FDD write.

= 1 Disable FDD write(forces pins WE, WD stay high).

Bit 0: SWWP

= 0 Normal, use WP to determine whether the FDD is write protected or not.

= 1 FDD is always write-protected.

CRF2 (Default 0xFFh)

Bit 7 - 6: FDD D Drive Type
Bit 5 - 4: FDD C Drive Type
Bit 3 - 2: FDD B Drive Type
Bit 1 - 0: FDD A Drive Type

CRF4 (Default 0x00h)

FDD0 Selection:
Bit 7: Reserved.
Bit 6: Precomp. Disable.
= 1 Disable FDC Precompensation.
= 0 Enable FDC Precompensation.
Bit 5: Reserved.
Bit 4 - 3: DRTS1, DRTS0: Data Rate Table select (Refer to TABLE A).
= 00b Select Regular drives and 2.88 format
= 01b 3-mode drive
= 10b 2 Meg Tape
= 11b Reserved
Bit 2: Reserved.
Bit 1:0: DTYPE0, DTYPE1: Drive Type select (Refer to TABLE B).

CRF5 (Default 0x00h)

FDD1 Selection: Same as FDD0 of CRF4.

TABLE A

Drive Rate Table Select		Data Rate		Selected Data Rate		SELDEN
DRTS1	DRTS0	DRATE1	DRATE0	MFM	FM	
0	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	300K	150K	0
		1	0	250K	125K	0
0	1	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	500K	250K	0
		1	0	250K	125K	0
1	0	1	1	1Meg	---	1
		0	0	500K	250K	1
		0	1	2Meg	---	0
		1	0	250K	125K	0

TABLE B

DTYPE0	DTYPE1	DRVDEN0(pin 2)	DRVDEN1(pin 3)	DRIVE TYPE
0	0	SELDEN	DRATE0	4/2/1 MB 3.5”“ 2/1 MB 5.25” 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	$\overline{\text{SELDEN}}$	DRATE0	
1	1	DRATE0	DRATE1	

9.6 Logical Device 1 (Parallel Port)

CR30 (Default 0x01 if PNPCSV = 0 during POR, 0x00h otherwise)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03h, 0x78h if PNPCSV = 0 during POR, default 0x00h, 0x00h otherwise)

These two registers select Parallel Port I/O base address.

[0x100h: 0xFFCh] on 4 byte boundary (EPP not supported) or

[0x100h: 0xFF8h] on 8 byte boundary (all modes supported, EPP is only available when the base address is on 8 byte boundary).

CR70 (Default 0x07h if PNPCSV = 0 during POR, 0x00h otherwise)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for Parallel Port.

CR74 (Default 0x04h)

Bit 7 - 3: Reserved.

Bit 2 - 0: These bits select DRQ resource for Parallel Port.

0x00h = DMA0

0x01h = DMA1

0x02h = DMA2

0x03h = DMA3

0x04h - 0x07h = No DMA active

CRF0 (Default 0x3Fh)

Bit 7: Reserved.

Bit 6 - 3: ECP FIFO Threshold.

Bit 2 - 0: Parallel Port Mode (CR28 PRTMODS2 = 0)

= 100b Printer Mode (Default)

= 000b Standard and Bi-direction (SPP) mode

= 001b EPP - 1.9 and SPP mode

= 101b EPP - 1.7 and SPP mode

= 010b ECP mode

= 011b ECP and EPP - 1.9 mode

= 111b ECP and EPP - 1.7 mode.

9.7 Logical Device 2 (UART A)

CR30 (Default 0x01h if PNPCSV = 0 during POR, 0x00h otherwise)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x03h, 0xF8h if PNPCSV = 0 during POR, 0x00h, 0x00h otherwise)

These two registers select Serial Port 1 I/O base address [0x100h:0xFF8h] on 8 byte boundary.

CR70 (Default 0x04h if PNPCSV = 0 during POR, 0x00h otherwise)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resource for Serial Port 1.

CRF0 (Default 0x00h)

Bit 7 - 2: Reserved.

Bit 1 - 0: SUACLKB1, SUACLKB0

= 00b UART A clock source is 1.8462 Mhz (24MHz/13)

= 01b UART A clock source is 2 Mhz (24MHz/12)

= 10b UART A clock source is 24 Mhz (24MHz/1)

= 11b UART A clock source is 14.769 Mhz (24mhz/1.625)

9.8 Logical Device 6 (FIR)

CR30 (Default 0x00h)

Bit 7 - 1: Reserved.

Bit 0:

= 1 Activates the logical device.

= 0 Logical device is inactive.

CR60, CR 61 (Default 0x00h, 0x00h)

These two registers select IR I/O base address [0x100h : 0xFF8h] on 8 byte boundary.

CR70 (Default 0x00h)

Bit 7 - 4: Reserved.

Bit [3:0]: These bits select IRQ resource for IR

CR74 (Default 0x04h)

Bit 7-3 : Reserved.

Bit 2-0 : These bits select DRQ resource for RX of FIR.

= 0x00h DMA0

= 0x01h DMA1

= 0x02h DMA2

= 0x03h DMA3

= 0x04h - 0x07h No DMA active

CR75 (Default 0x04h)

Bit 7-3 : Reserved.

Bit 2-0 : These bits select DRQ resource for TX of FIR.

= 0x00h DMA0

= 0x01h DMA1

= 0x02h DMA2

= 0x03h DMA3

= 0x04h - 0x07h No DMA active

CRF0 (Default 0x00h)

Bit 7 - 4: Reserved.

Bit 3: RXW4C

= 0 No reception delay when SIR is changed from TX mode to RX mode.

= 1 Reception delays 4 characters-time (40 bit-time) when SIR is changed from TX mode to RX mode.

Bit 2: TXW4C

= 0 No transmission delay when SIR is changed from RX mode to TX mode.

= 1 Transmission delays 4 characters-time (40 bit-time) when SIR is changed from RX mode to TX mode.

Bit 1 : APEDCRC

= 0 No append hardware CRC value as data in FIR/MIR mode.

= 1 Append hardware CRC value as data in FIR/MIR mode.

Bit 0 : ENBNKSEL; Bank select enable

= 0 Disable IR Bank selection.

= 1 Enable IR Bank selection.

9.9 Logical Device 7 (GPIO Port 1)

CR30 (Default 0x00h)

Bit 7 - 1: Reserved.

Bit 0: = 1 GPIO1 port is Activate

= 0 GPIO1 port is inactive.

CR62, CR 63 (Default 0x00h, 0x00h)

These two registers select the GPIO1 base address [0x100h : 0xFFFh] on 4byte boundary.

IO address : CRF1 base address

IO address + 1 : CRF3 base address

IO address + 2 : CRF4 base address

IO address + 3 : CRF5 base address

CR70 (Default 0x09 if PNPCSV = 0 during POR, default 0x00 otherwise when the port is active)

Bit [7:4]: These bits select IRQ resource for IRQIN1.

Bit [3:0]: These bits select IRQ resource for IRQIN0.

CRF0 (GPIO1 selection register. Default 0xFFh)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GPIO1 data register. Default 0x00h when the port is active)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP5 inversion register. Default 0x00h when the port is active)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (PLED mode register. Default 0x00h)

Bit 7 ~ 3 : Reserved .

Bit 2: select WDTO count mode.

= 0 second

= 1 minute

Bit 1 ~ 0: select PLED mode

= 00b Power LED pin is tri-stated.

= 01b Power LED pin is droved low.

= 10b Power LED pin is a 1Hz toggle pulse with 50 duty cycle.

= 11b Power LED pin is a 1/4Hz toggle pulse with 50 duty cycle.

CRF4 (Default 0x00h)

Watch Dog Timer Time-out value. Writing a non-zero value to this register causes the counter to load the value to Watch Dog Counter and start counting down. Reading this register returns current value in Watch Dog Counter instead of Watch Dog Timer Time-out value.

Bit 7 - 0:

= 0x00h Time-out Disable

= 0x01h Time-out occurs after 1 second/minute

= 0x02h Time-out occurs after 2 second/minutes

= 0x03h Time-out occurs after 3 second/minutes

.....

= 0xFFh Time-out occurs after 255 second/minutes

CRF5 (Default 0x00h)

Bit 7 ~ 6 : Reserved .

Bit 5: Force Watch Dog Timer Time-out, Write only*

= 1 Force Watch Dog Timer time-out event; this bit is self-clearing.

Bit 4: Watch Dog Timer Status, R/W

= 1 Watch Dog Timer time-out occurred.

= 0 Watch Dog Timer counting

Bit 3 -0: These bits select IRQ resource for Watch Dog. Setting of 2 selects SMI.

Logical Device 8 (GPIO Port 2)

CR30 (Default 0x00h)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activate GPIO2

= 0 GPIO2 is inactive.

CR62, CR 63 (Default 0x00h, 0x00h)

These two registers select the GPIO1 base address [0x100:0xFFF] on 1 byte boundary

IO address : CRF1 base address

CRF0 (GP10-GP17 I/O selection register. Default 0xFFh)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP10-GP17 data register. Default 0x00h when the port is active, otherwise 0xFF)

If a port is programmed to be an output port, then its respective bit can be read/written

If a port is programmed to be an input port, then its respective bit can only be read

CRF2 (GP10-GP17 inversion register. Default 0x00h when the port is active, otherwise 0xFF)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

Logical Device 9 (GPIO Port 3 ~ GPIO Port 5)

CR30 (Default 0x00h)

Bit 7 ~ 3: Reserved.

Bit 2: = 1 Activate GPIO5.
= 0 GPIO5 is inactive

Bit 1: = 1 Activate GPIO4.
= 0 GPIO4 is inactive

Bit 0: = 1 Activate GPIO3.
= 0 GPIO3 is inactive.

CR60,61(Default 0x00h,0x00h).

These two registers select the GP 3,4,5 base address(0x100h : FFFh) ON 3 bytes boundary.

IO address : CRF1 base address

IO address + 1 : CRF3 base address

IO address + 2 : CRF7 base address

CRF0 (GP3 I/O selection register. Default 0xFFh)

When set to a '1', respective GPIO port is programmed as an input port.

When set to a '0', respective GPIO port is programmed as an output port.

CRF1 (GP3 data register. Default 0x00h when the port is active, otherwise 0xFFh)

If a port is programmed to be an output port, then its respective bit can be read/written.

If a port is programmed to be an input port, then its respective bit can only be read.

CRF2 (GP3 inversion register. Default 0x00h when the port is active, otherwise 0xFFh)

When set to a '1', the incoming/outgoing port value is inverted.

When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF3 (GP4 I/O selection register. Default 0xFFh)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF4 (GP4 data register. Default 0x00h when the port is active, otherwise 0xFFh)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF5 (GP4 inversion register. Default 0x00h when the port is active, otherwise 0xFFh)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

CRF6 (GP5 I/O selection register. Default 0xFFh)

When set to a '1', respective GPIO port is programmed as an input port.
When set to a '0', respective GPIO port is programmed as an output port.

CRF7 (GP5 data register. Default 0x00h when the port is active, otherwise 0xFFh)

If a port is programmed to be an output port, then its respective bit can be read/written.
If a port is programmed to be an input port, then its respective bit can only be read.

CRF8 (GP5 inversion register. Default 0x00h when the port is active, otherwise 0xFFh)

When set to a '1', the incoming/outgoing port value is inverted.
When set to a '0', the incoming/outgoing port value is the same as in data register.

9.10 Logical Device A (ACPI)

CR30 (Default 0x00h)

Bit 7 - 1: Reserved.

Bit 0: = 1 Activates the logical device.

= 0 Logical device is inactive.

CR70 (Default 0x00h)

Bit 7 - 4: Reserved.

Bit 3 - 0: These bits select IRQ resources for $\overline{SMI}$ / $\overline{PME}$

CRE0 (Default 0x00h)

Bit7 : ENCIRWAKEUP. Enable CIR to wake-up system .

= 0 Disable CIR wake up function

= 1 Enable CIR wake up function

Bit 5 : CIR_STS. This bit is cleared by reading 1 this register.

= 0 Disable

= 1 Enable

Bit6, 4 ~ 0 : Reserved

CRE 1 (Default 0x00) CIR wake up index register

The range of CIR wake up index register is 0x20 ~ px2F .

CRE 2 CIR wake up data register

This register holds the value of wake up key register indicated by CRE1. This register can be read/written.

CRE5 (Default 0x00)

Bit 7 : Reserved

Bit 6 ~ 0 :Compared Code Length . When the compared codes are storage in the data register, these data length should be written to this register.

CRE6 (Default 0x00)

Bit 7 - 6: Reserved.

Bit 5 - 0: CIR Baud Rate Divisor. The clock base of CIR is 32khz, so that the baud rate is 32khz divided by (CIR Baud Rate Divisor + 1).

CRE7 (Default 0x00)

Bit 7 - 3: Reserved.

Bit 2:Reset CIR Power-On function. After using CIR power-on, the software should write logical 1 to restart CIR power-on function.

Bit 1: Invert RX Data.

= 1 Inverting RX Data.

= 0 Not inverting RX Data.

Bit 0: Enable Demodulation.

= 1 Enable received signal to demodulate.

= 0 Disable received signal to demodulate.

CRF0 (Default 0x00)

Bit 7: CHIPPME. Chip level auto power management enable.

= 0 disable the auto power management functions

= 1 enable the auto power management functions.

Bit 6: CIRPME. Consumer IR port auto power management enable.

= 0 disable the auto power management functions

= 1 enable the auto power management functions.

Bit 5: MIDIPME. MIDI port auto power management enable.

= 0 disable the auto power management functions

= 1 enable the auto power management functions.

Bit 4: Reserved. Return zero when read.

Bit 3: PRTPME. Printer port auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

Bit 2: FDCPME. FDC auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

Bit 1: URAPME. UART A auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

Bit 0: URBPME. UART B auto power management enable.

= 0 disable the auto power management functions.

= 1 enable the auto power management functions.

CRF1 (Default 0x00)

Bit 7: WAK_STS. This bit is set when the chip is in the sleeping state and an enabled resume event occurs. Upon setting this bit, the sleeping/working state machine will transition the system to the working state. This bit is only set by hardware and is cleared by writing a 1

to this bit position or by the sleeping/working state machine automatically when the global standby timer expires.

= 0 the chip is in the sleeping state.

= 1 the chip is in the working state.

Bit 6 - 5: Devices' trap status.

Bit 4: Reserved. Return zero when read.

Bit 3 - 0: Devices' trap status.

CRF3 (Default 0x00)

Bit 7 ~ 4: Reserved. Return zero when read.

Bit 3 ~ 0: Device's IRQ status.

These bits indicate the IRQ status of the individual device respectively. The device's IRQ status bit is set by their source device and is cleared by writing a 1. Writing a 0 has no effect.

Bit 3: PRTIRQSTS. printer port IRQ status.

Bit 2: FDCIRQSTS. FDC IRQ status.

Bit 1: URAIRQSTS. UART A IRQ status.

Bit 0: URBIRQSTS. FIR IRQ status.

CRF4 (Default 0x00)

Bit 7 ~ 4: Reserved. Return zero when read.

Bit 3 ~ 0: These bits indicate the IRQ status of the individual GPIO function or logical device respectively. The status bit is set by their source function or device and is cleared by writing a1. Writing a 0 has no effect.

Bit 2: WDTIRQSTS. Watch dog timer IRQ status.

Bit 1~0: Reserved

CRF9 (Default 0x00)

Bit 7 - 3: Reserved. Return zero when read.

Bit 2: PME_EN: Select the power management events to be either an $\overline{PME}$ or $\overline{SMI}$ interrupt for the IRQ events. Note that: this bit is valid only when SMIPME_OE = 1.

= 0 the power management events will generate an $\overline{SMI}$ event.

= 1 the power management events will generate an $\overline{PME}$ event.

Bit 1: FSLEEP: This bit selects the fast expiry time of individual devices.

= 0 1 S

= 1 8 mS.

Bit 0: SMIPME_OE: This is the $\overline{SMI}$ and $\overline{PME}$ output enable bit.

= 0 neither $\overline{SMI}$ nor $\overline{PME}$ will be generated. Only the IRQ status bit is set.

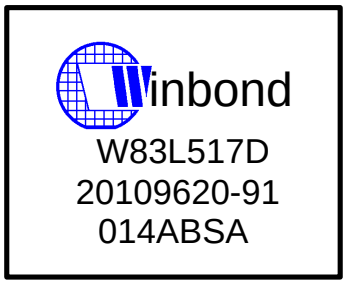
= 1 an $\overline{SMI}$ or $\overline{PME}$ event will be generated.

10. ORDERING INSTRUCTION

PART NO.	PACKAGE	REMARKS
W83L517D	100-pin LQFP	

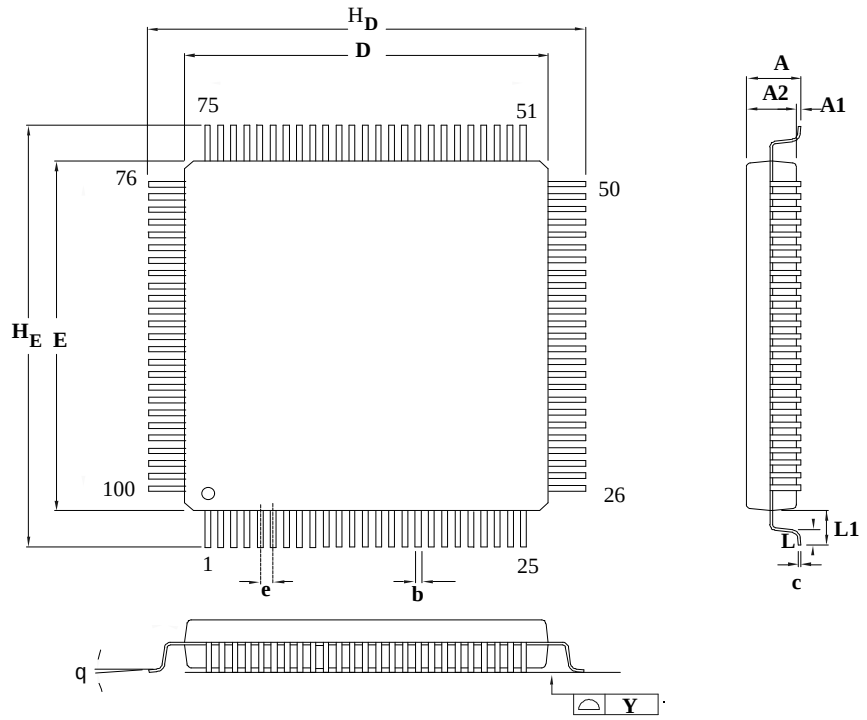
11. HOW TO READ THE TOP MARKING

Example: The top marking of W83L517D



1st line: Winbond logo
2nd line: the type number: W83L517D
3rd line: the tracking code 20109620-91
20109620-91: wafer production series lot number
4th line: the tracking code 014 A B SA
014: packages made in '2000, week 14
A: assembly house ID; A means ASE, S means SPIL.... etc.
B: IC revision; A means version A, B means version B
SA: for internal use

12. PACKAGE DIMENSIONS



Controlling Dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A1	0.002	—	—	0.05	—	—
A2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.007	0.009	0.011	0.17	0.22	0.27
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.556	13.90	14.00	14.10
E	0.547	0.551	0.556	13.90	14.00	14.10
e	—	0.020	—	—	0.50	—
H_D	0.622	0.630	0.638	15.80	16.00	16.20
H_E	0.622	0.630	0.638	15.80	16.00	16.20
L	0.018	0.024	0.030	0.45	0.60	0.75
L1	—	0.039	—	—	1.00	—
y	—	—	0.004	—	—	0.10
q	0°	—	7°	0°	—	7°

Winbond Electronics Corp.

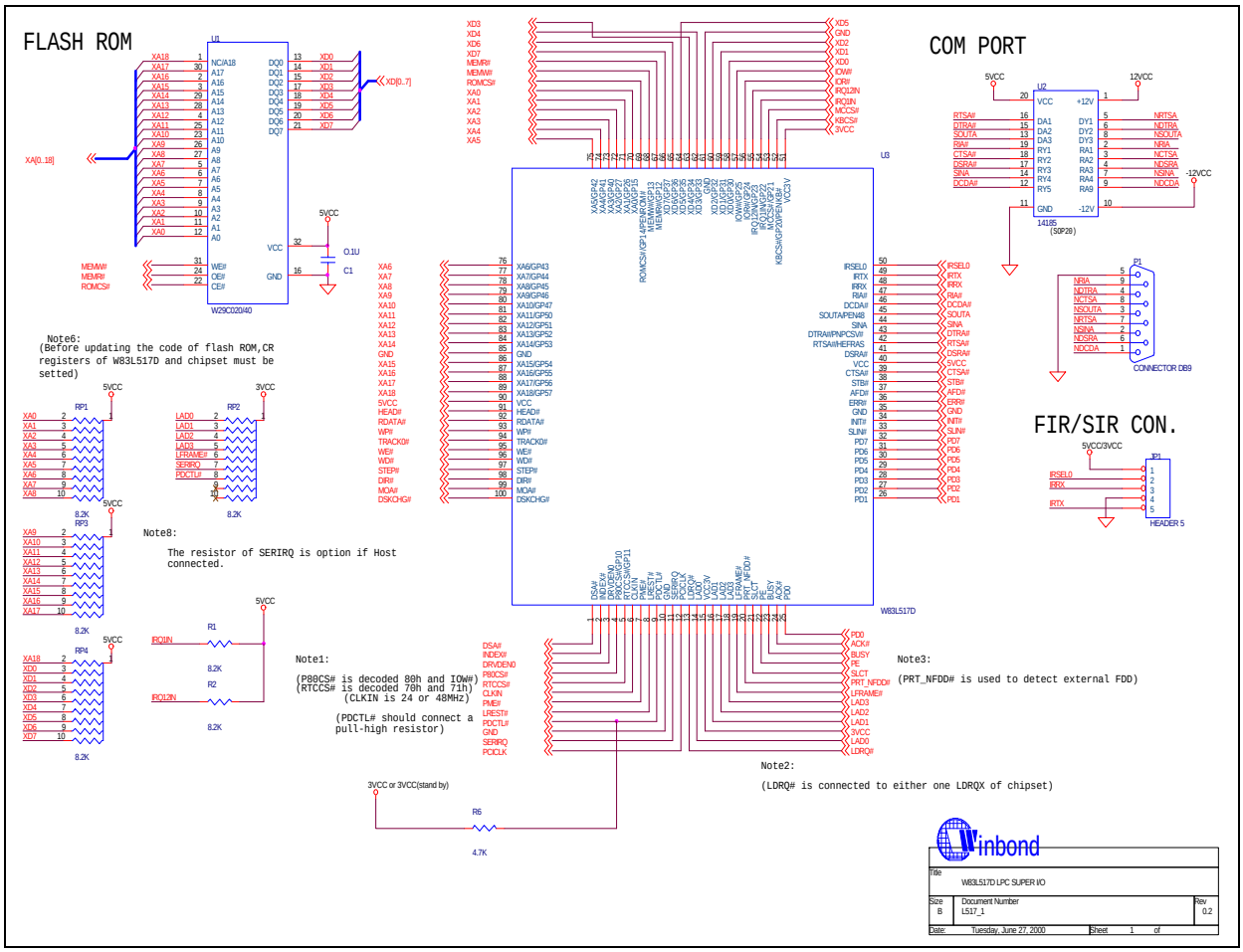
Headquarters
No. 4, Creation Rd. III
Science-Based Industrial Park
Hsinchu, Taiwan
TEL: 886-35-770066
FAX: 886-35-789467
www: http://www.winbond.com.tw/

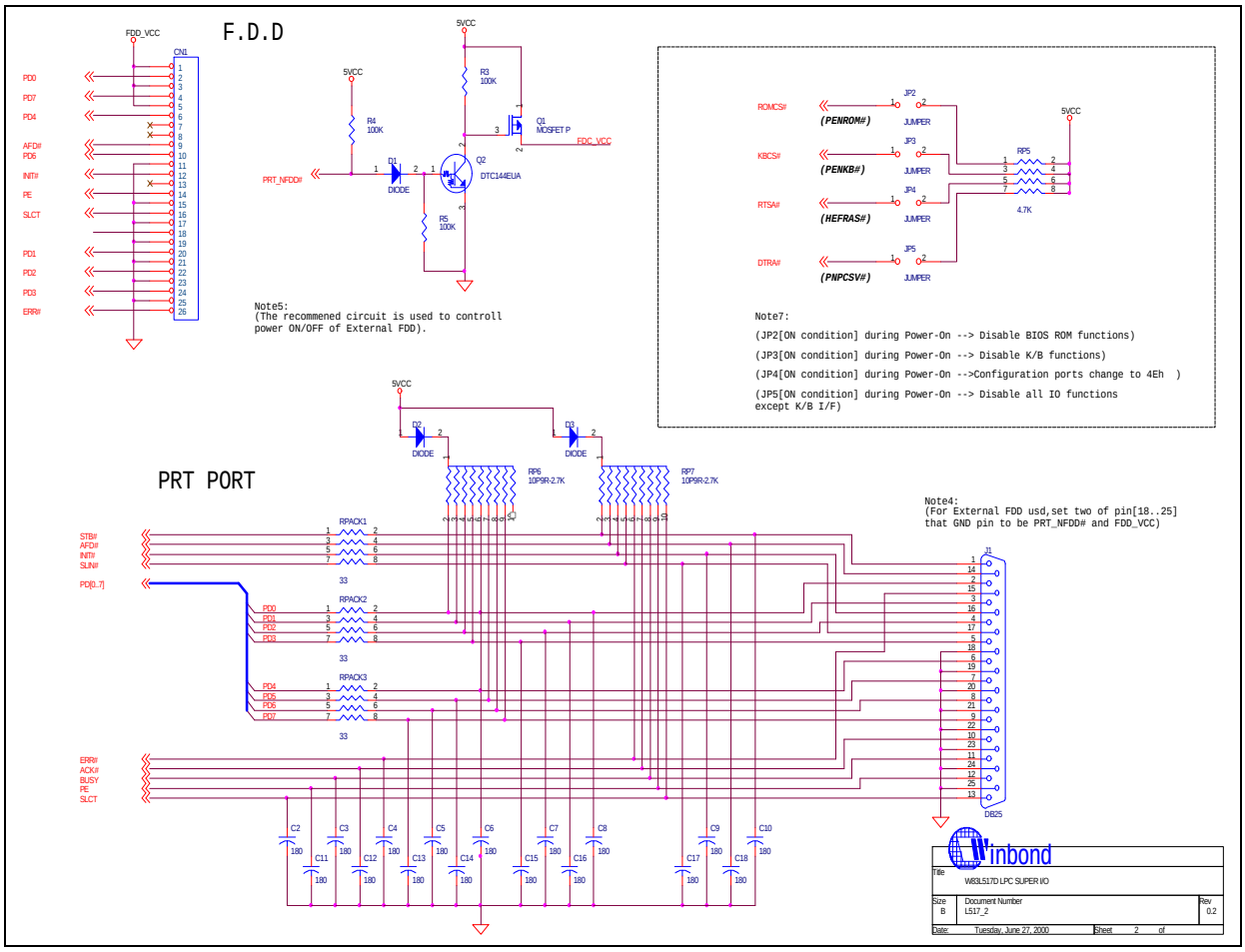
Taipei Office
11F, No. 115, Sec. 3, Min-Sheng East Rd.
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502
TLX: 16485 WINTPE

Winbond Electronics (H.K.) Ltd.
Rm. 803, World Trade Square, Tower II
123 Hoi Bun Rd., Kwun Tong
Kowloon, Hong Kong
TEL: 852-27516023-7
FAX: 852-27552064

Winbond Electronics (North America) Corp.
2730 Orchard Parkway
San Jose, CA 95134 U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

13 Recommended Circuit




F.D.D
FDD_VCC
CN1
PD0
PD7
PD4
AFD#
PD6
INIT#
PE
SLCT
PD1
PD2
PD3
ERR#
5VCC
R3
100K
R4
100K
Q1
MOSFET P
FDC_VCC
PRT_NFDD#
D1
DIODE
Q2
DTC144EUA
R5
100K
Note5:
(The recommened circuit is used to controll
power ON/OFF of External FDD).
ROMCS#
(PENROM#)
JP2
JUMPER
KBCS#
(PENKB#)
JP3
JUMPER
RTSA#
(HEFRAS#)
JP4
JUMPER
DTRA#
(PNPCSV#)
JP5
JUMPER
RP5
4.7K
Note7:
(JP2[ON condition] during Power-On --> Disable BIOS ROM functions)
(JP3[ON condition] during Power-On --> Disable K/B functions)
(JP4[ON condition] during Power-On -->Configuration ports change to 4Eh)
(JP5[ON condition] during Power-On --> Disable all IO functions
except K/B I/F)
PRT PORT
D2
DIODE
D3
DIODE
RP6
10P9R-2.7K
RP7
10P9R-2.7K
Note4:
(For External FDD usd,set two of pin[18..25]
that GND pin to be PRT_NFDD# and FDD_VCC)
STB#
AFD#
INIT#
SLIN#
PD[0..7]
RPACK1
RPACK2
RPACK3
33
ERR#
ACK#
BUSY
PE
SLCT
J1
DB25
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
180
Winbond
Title
W83L517D LPC SUPER I/O
Size
B
Document Number
L517_2
Rev
0.2
Date:
Tuesday, June 27, 2000
Sheet
2
of