W86L387D

Winbond Host Interface
Memory Stick™ Bridge

W86L387D Data Sheet Revision History

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Winbond Electronics Corp.

PRELIMINARY

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PRELIMINARY

1. GENERAL DESCRIPTION

The W86L387D is a Memory Stick™ host interface bridge used between host microprocessor and Memory Stick™. The data width of host microprocessor can be 8-bit or 16-bit. W86L387D can support synchronous or asynchronous type of host interface. It also supports DMA or Interrupt type of transfer mode to improve data transfer performance between host microprocessor and Memory Stick™. W86L387D is fit for most of IA devices, such as PDA, Cellular Phone, DSC, and MP3 player.

2. FEATURES

- Compliant with Sony Memory Stick™ spec. Version 1.3
- Support two types of host microprocessor interface access--synchronous and asynchronous mode
- DMA and Interrupt transfer mode supported
- Host microprocessor data bus can be 8-bit or 16-bit
- Built-in crystal driver circuit, support external oscillator or crystal clock input
- Extra 8 programmable GPIO supported
- Wide range of clock input up to 20Mhz
- 3.3V opereation
- 48-pin LQFP package

Ordering Information

Part Number	Package Type	Production Flow
W86L387D	48-PIN LQFP	Commercial, 0°C to +70°C

3. PIN CONFIGURATION

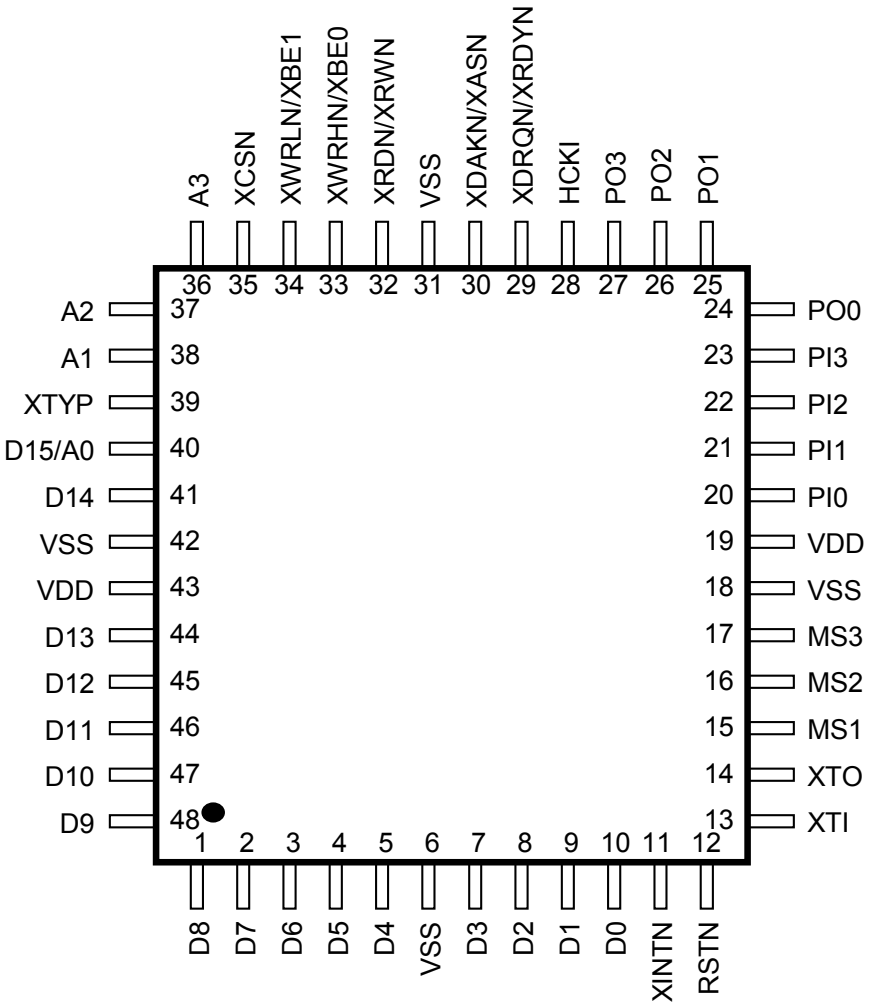


Fig.3-1 W86L387D Pin Assignment.

4. PIN DESCRIPTIONS

Pin	Name	Type	Description
MS Interface:			
15	MS1	DO	Memory stick connect pin #1
16	MS2	DO/DI	Memory stick connect pin #2
17	MS3	DO	Memory stick connect pin #3
Crystal Driver:			
13	XTI	DI	From 3.58MHz to 20MHz Clock driver input signal, can be used as external clock input.
14	XTO	DO	Clock driver output signal.
Host Interface:			
28	HCKI	DI	Host clock input. Only used in Type2.
35	XCSN	DI	Chip select input pin, active low.
36:38	A[3:1]	DI	Address input pins.
40	D15/A0	DI/DO	Data bus D15 pin, D[15:8] is the high byte of the data bus, D15 also used as A0 when 8-bit Host data size. In 8-bit mode, internal register high byte (D15:8) will accessed at data bus [7:0] when A0 = 1, low byte (D7:0) will accessed at data bus [7:0] when A0 = 0.
41	D14	DI/DO	Data bus D14 pin.
44:48	D[13:9]	DI/DO	Data bus [13:9] pins.
1:5	D[8:4]	DI/DO	Data bus [8:4] pins, D[7:0] is the low byte of the data bus.
7:10	D[3:0]	DI/DO	Data bus [3:0] pins.
33	XWRHN/ XBE0	DI	Type 1: High byte (D15 to D8) write control pin, active low. Type 2: High byte (D15 to D8) data valid pin, active low.
34	XWRLN/ XBE1	DI	Type 1: Low byte (D7 to D0) write control pin, active low. Type 2: Low byte (D7 to D0) data valid pin, active low.

4. Pin Descriptions, continued

Pin	Name	Type	Description
32	XRDN/ XRWN	DI	Type 1: Read control pin, active low. Type 2: Read write control pin, 1: read 0: write
11	XINTN	DO	Interrupt request pin, active low.
30	XDAKN/ XASN	**DI**	Type 1: DMA transfer acknowledge pin, active low. Type 2: Bus access cycle start pin, active low.
29	XDRQN/ XRDYN	DO	Type 1: DMA transfer request pin, active low. Type 2: Bus cycle complete pin, active low.
39	XTYP	DI	Host interface type 2 select pin, 0 : type 1 mode. 1 : type 2 mode.
GP I/O Port:			
23:20	PI[3:0]	DI	4-bit parallel port input signal.
27:24	PO[3:0]	DO	4-bit parallel port output signal.
Other:			
12	RSTN	DI	Reset input, hardware reset input, active low.
Power:			
19,43	VDD x2	DP	Power supply 3.3V (2 pins).
6,18, 31,42	VSS x4	DP	Ground (4 pins).

Type: DP is Power, DI is Digital Input, DO is Digital Output.

5. BLOCK DIAGRAM

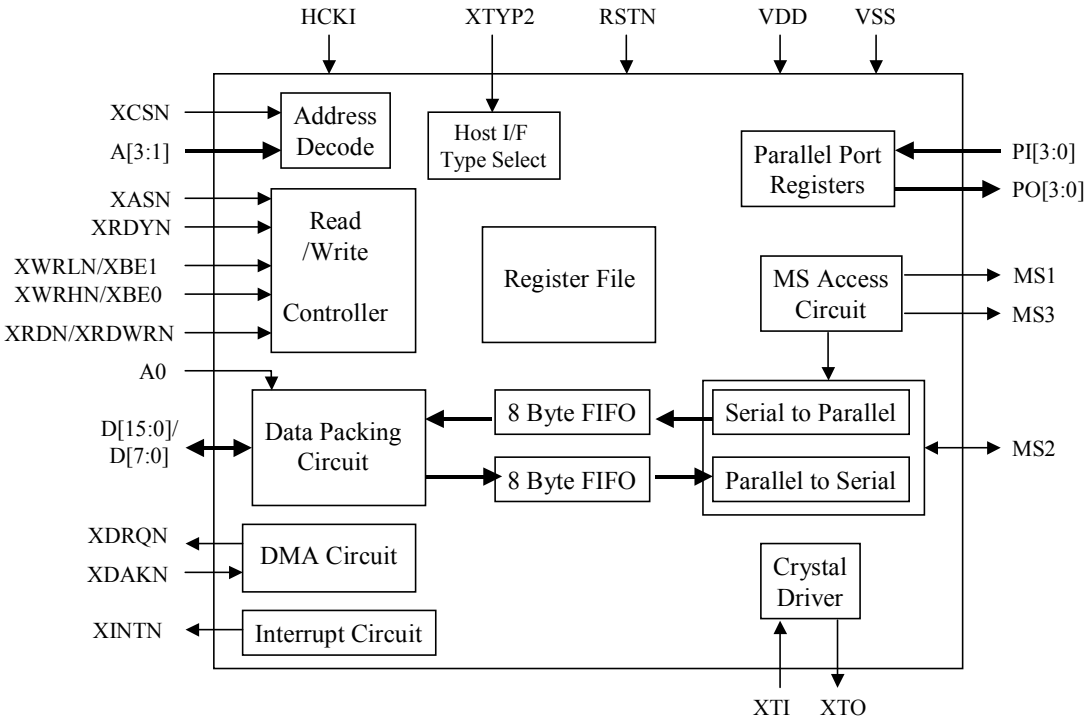


Fig. 5-1 Block Diagram of W86L387D

6. REGISTERS

6.1 Register Map

The register in the W86L387D is consisted of command, status, control, received/transmit data buffer, interrupt, DMA and parallel port registers and READY register in Host interface type 2, these registers are listed as follows:

Addr	Register Name	Content (note 2)															
A[3:1]	(note 1)	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
000	Command Reg. (R/W)	PID code				Data size											
		0	0	0	0	-	-	0	0	0	0	0	0	0	0	0	0
001	Status Reg. (RO)	Status								-	-	-	-	-	-	-	-
		0	0	-	-	1	0	1	0								
001	Control Reg. (R/W)	-	-	-	-	-	-	-	-	Control							
										0	0	0	0	0	1	0	1
010	Receive Data Buffer (R/O)	Receive data buffer															
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
010	Transmit Data Buffer (WO)	Transmit data buffer															
		X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
011	Interrupt Status Reg. (RO)	Interrupt status								-	-	-	-	-	-	-	-
		1	0	0	0	-	-	0	0								
011	Interrupt Control Reg. (R/W)	-	-	-	-	-	-	-	-	Interrupt control							
										0	0	0	-	-	-	-	-
100	Parallel Port Data Reg. ([15:12]RO, [11:8]R/W)	PI[3:0]				PO[3:0]				-	-	-	-	-	-	-	-
		X	X	X	X	X	X	X	X								
100	Parallel Port Control Reg. (R/W)	-	-	-	-	-	-	-	-	PIEN[3:0]				POEN[3:0]			
										0	0	0	0	0	0	0	0
101	Ready Control Reg. (R/W)	F	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
		0															
111	Data Size Reg. (R/W)	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	8-bit
										0	0	0	0	0	0	0	0

Note 1: R/W means the register can be read and write.

RO means the register is read only.

WO means the register is write only.

Note 2: The data bit in the content is the initial value during hardware reset.

0: the bit value is 0.

1: the bit value is 1.

X: the bit value is unknown.

-: Undefined bit in the register and the value will read 0.

7. FUNCTIONAL DESCRIPTION

7.1 Host Interface

The Host interface type may be type 1 or type 2 and the data size of the data bus may be 16-bit or 8-bit.

Host Interface Type 1:

The Host interface type 1 is selected when XTYP pin is low. The data size of the CPU data bus may be 16-bit or 8-bit. Figure 7-1 shows the timing of 16-bit CPU read and write in type 1, figure 7-2 and 7-3 show the timing of CPU 8-bit data bus read and write in type 1.

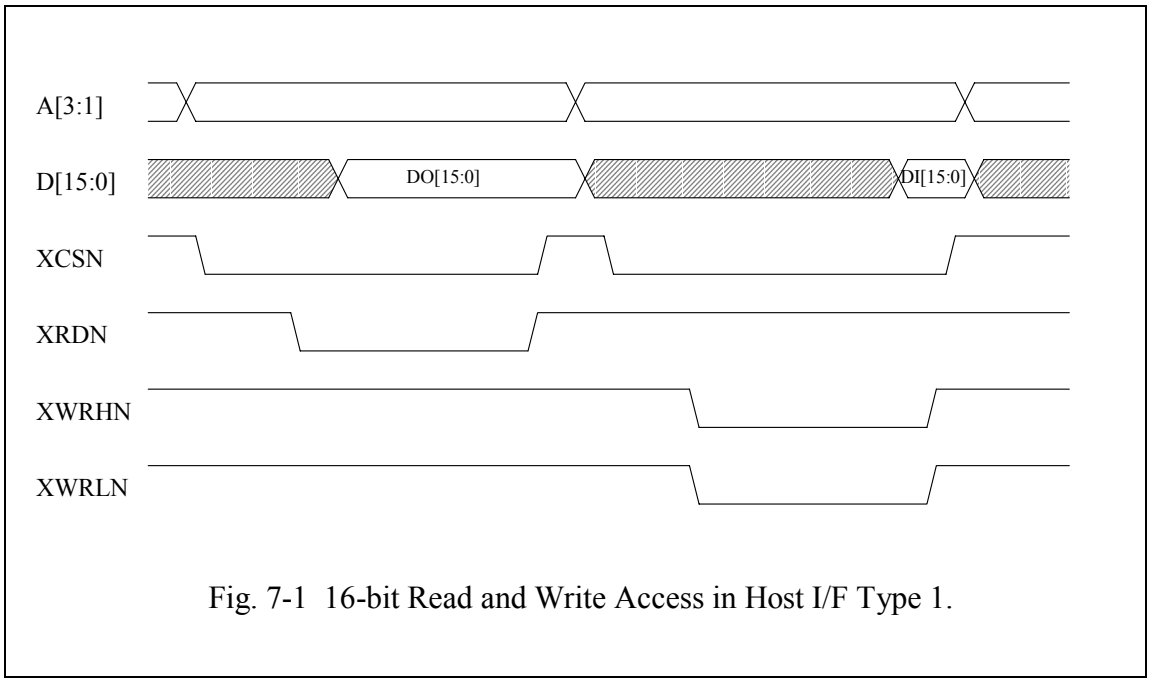


Fig. 7-1 16-bit Read and Write Access in Host I/F Type 1.

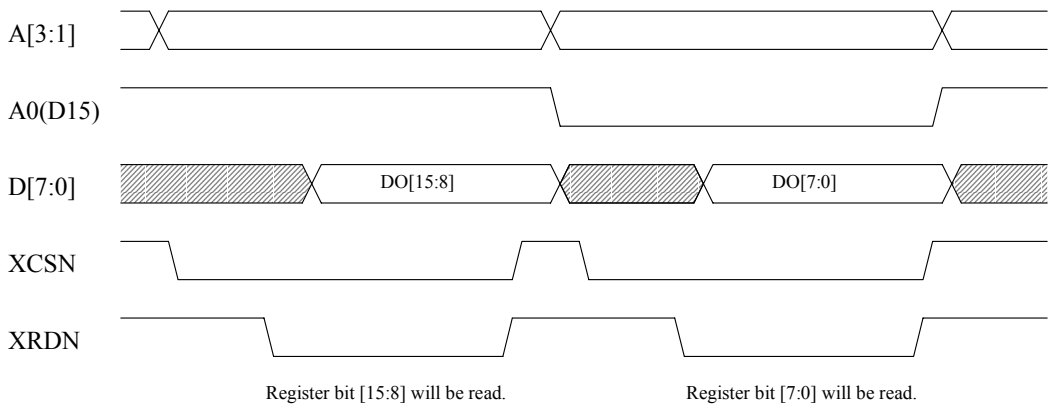


Fig. 7-2 CPU 8-bit Data Bus Read Access in Host I/F Type 1.

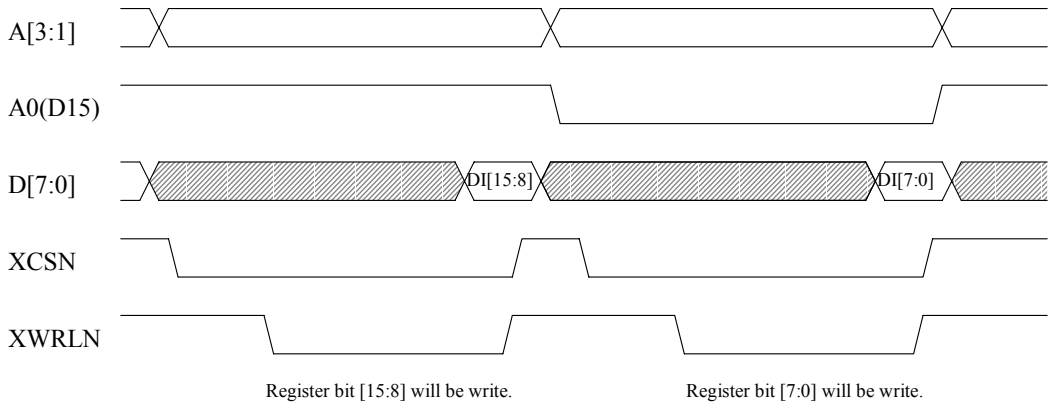


Fig. 7-3 CPU 8-bit Data Bus Write Access in Host I/F Type 1.

The data is located at bit [7:0] when the data size of Host CPU is 8-bit, the address bit 0 (A0) = 1 is to access the register data bit [15:8], A0 = 0 to access data bit [7:0].

Host Interface Type 2:

The Host interface type 2 is selected when XTYP pin is high. The data size of the CPU data bus may be 16-bit or 8-bit and the access cycle may be in 3-cycle or 3-cycle. Figure 7-4 shows the timing of 16-bit CPU read write in type 2 and the access cycle is 3-cycle access, figure 7-5 shows the timing of 16-bit CPU read write in type 2 and the access cycle is 2-cycle access.

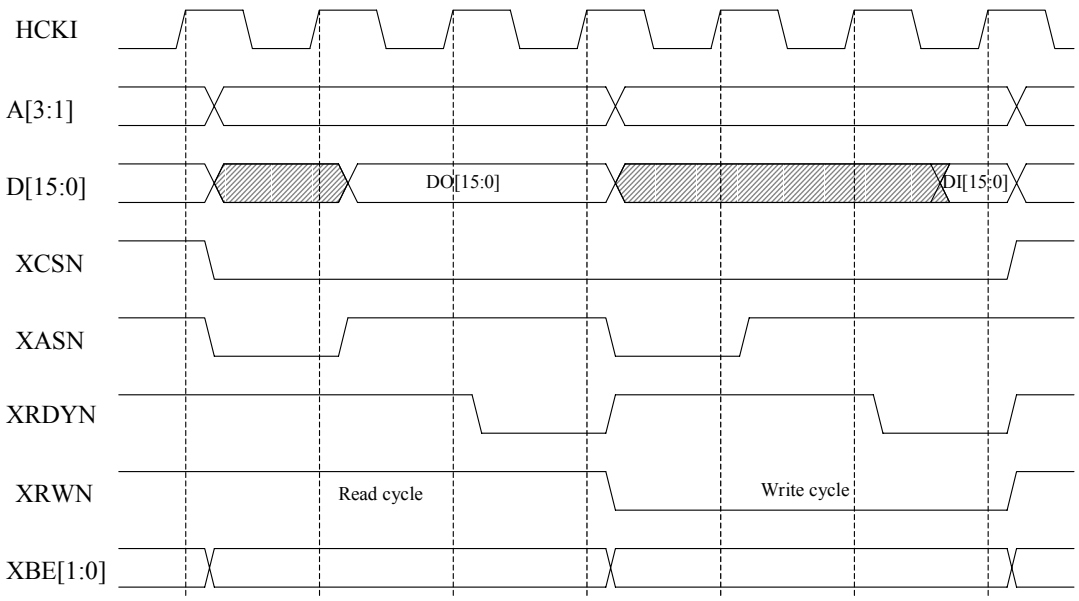


Fig. 7-4 16-bit Read and Write Access in Host I/F Type 2, 3-Cycle Access.

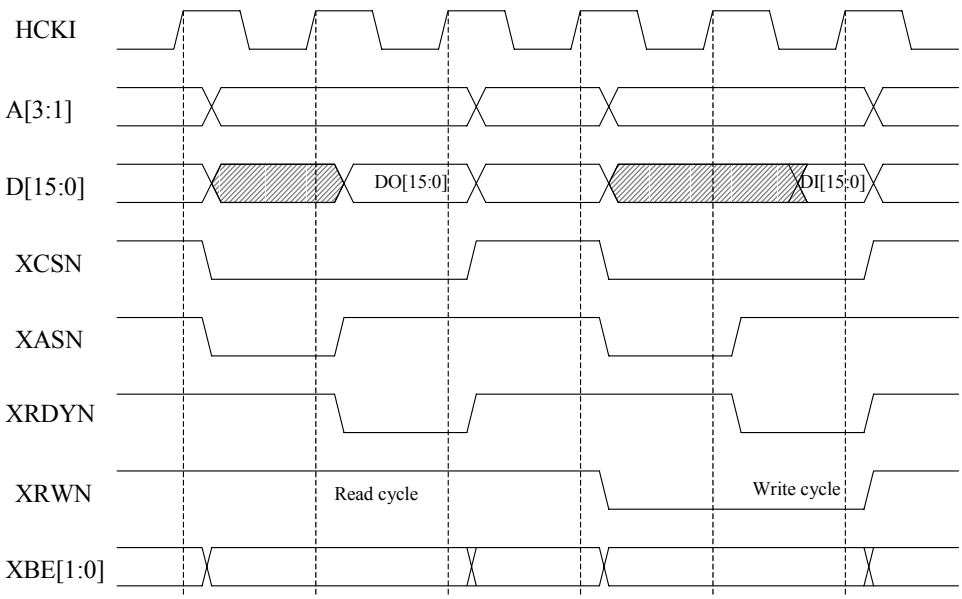


Fig. 7-5 16-bit Read and Write Access in Host I/F Type 2, 2-Cycle Access.

7.2 DMA Access

DMA request XDRQN is used to notify the Host that the Host should write data to the transmit data buffer or read data from the receive data buffer in data write to the card or data read from the card.

During data transmit to the card, the XDRQN will active if the data write command has been transfer to the card and the transmit data buffer have not enough data to transmit to the card. The XDRQN will not active if the transmit data buffer have enough data to transmit to the card.

During data receive from the card, the XDRQN will active if the data read command has been transfer to the card and the data have been received in the receive data buffer. The XDRQN will not active if the data read command has been executed completely and the receive data buffer is read out.

There are two types of DMA acknowledge waveform, the first type is configured if DAKEN = low, XDAKN is ignore and XDRQN will inactive after each access receive or transmit data buffer, the XDRQN will re-active after four clock later. Figure 7-6 shows the waveform of DMA access receive data buffer in DAKN = low. The second type is configured if DAKEN = high, XDAKN is used to count the transfer count of the data buffer, XDRQN will hold at active state until the data has been transferred completely. Figure 7-7 is the waveform of DMA access transmit data buffer in DAKN = high.

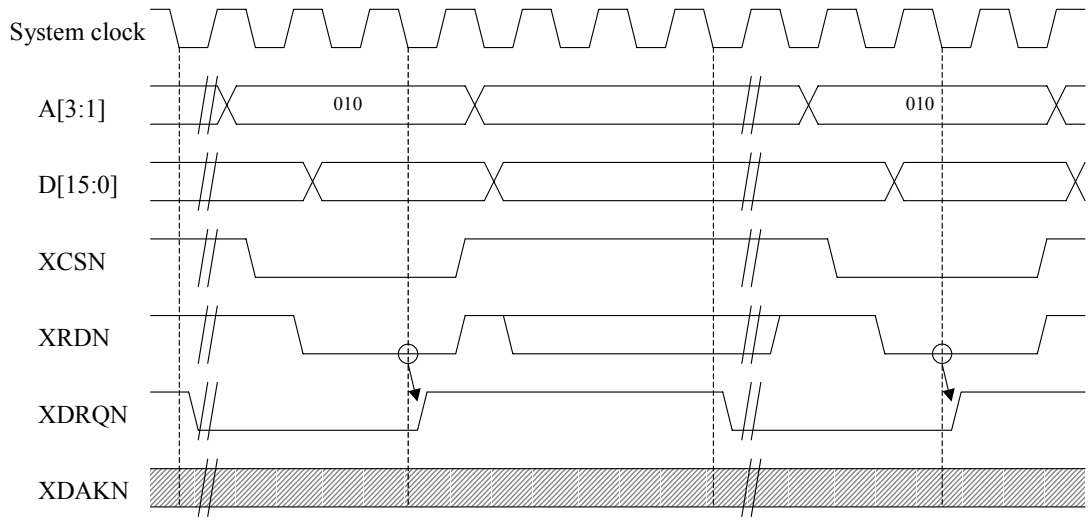


Fig. 7-6 DMA Access Receive Data Buffer (DAKEN = low).

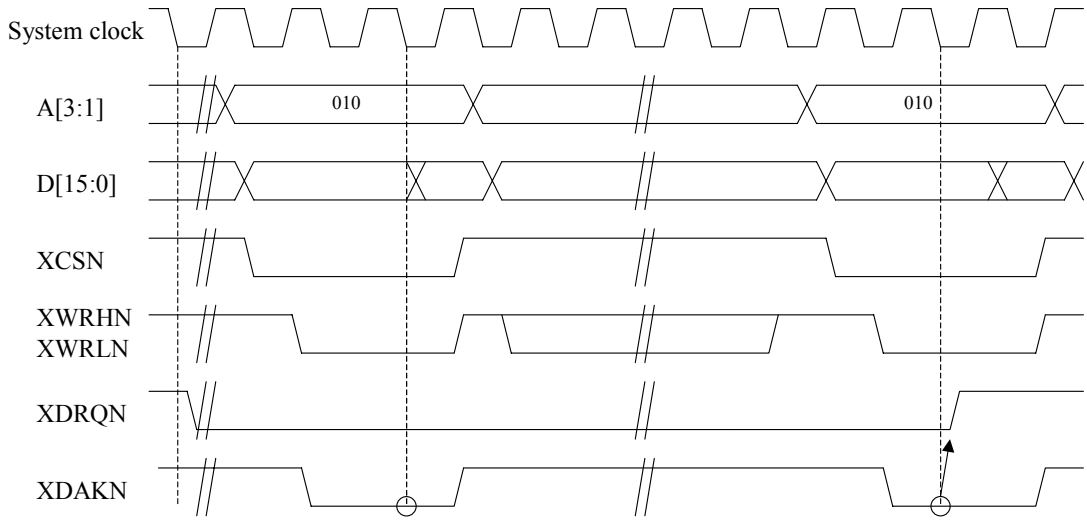


Fig. 7-7 DMA Access Transmit Data Buffer (DAKEN = high).

8. ELECTRICAL CHARACTERISTICS

8.1 Maximum Ratings*

	Parameter	Symbol	Rating	Units
1	Supply Voltage with respect to V_{VSS}	V_{VDD}	-0.3 to 6	V
2	Current at any pin other than supplies		0 to 10	mA
3	Storage Temperature	T_{st}	-65 to 150	℃

* Exceeding these values may cause permanent damage.

8.2 Recommended Operating Conditions

	Characteristics	Symbol	Rating	Unit
1	Operation Voltage (referenced to VSS pin).	V_{VDD}	3.0 to 3.6	V
2	Operation Voltage (referenced to VSS pin) (Note)	V_{VDD}	2.7to 3.0	V
3	Clock Frequency at XTI pin	f_{XTL}	20	MHz
4	Operation Temperature	T_{op}	0 to 70	℃

Note: Clock frequency not guaranteed up to 20MHz.

8.3 Power Supply Characteristics

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Test
1	Standby Supply Current	Power Supply	I_Q		2	10	uA	Test 1
2	Operating Supply Current	(V_{VDD} = 3.3V)	I_{VDD}		4.7	6	mA	Test 2
3	Operating Supply Current		I_{VDD}		3.5		mA	Test 3

‡: Typical figure are at V_{DIVDD} = 3.3V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Test 1: All input pins are V_{VDD} or V_{VSS}, configured as power down mode, output without loading and no clock input on the XTI and HCKI pins.

Test 2: 20 MHz external clock input on the XTI pin, output without loading.

Test 3: 20 MHz crystal connected at XTI and XTO pins, output without loading.

8.4. Digital Characteristics

	Parameter	Condition	Symbol	Min	Typ‡	Max	Units	Notes
1	Output High Voltage	2mA load	V_{OH}	0.9			VDD	1
2	Output Low Voltage	2mA sink	V_{OL}			0.1	VDD	1
3	Output High Voltage at CLK output	3mA load	V_{OH}	0.9			VDD	
4	Output Low Voltage at CLK output	3mA sink	V_{OL}			0.1	VDD	
5	High Level Input Voltage		V_{IH}	0.7			VDD	
6	Low Level Input Voltage		V_{IL}			0.3	VDD	
7	Input Current		Iin			1	uA	
8	Input Capacitance		Cin		10		pF	

‡: Typical figure are at V_{DVDD} = 3.3V and temperature = 25 ℃ and are for design aid only, not guaranteed and not subject to production testing.

Notes:

1: All output pins except CLK output.

8.5. Timing Characteristics

	Parameter	Symbol	Min	Typ	Max	Units	Notes
Clock (figure 8-1)							
1	XTI	fXTI	1	-	20	MHz	1
2	XTI high pulse width	$tXTI_{wh}$	10	-	-	nS	1
3	XTI low pulse width	$tXTI_{wl}$	10	-	-	nS	1
4	XTI rise time	$tXTI_{r}$	-	-	5	nS	1
5	XTI fall time	$tXTI_{f}$	-	-	5	nS	1
5	XTO delay time	$tXTO_{d}$	-	-	5	nS	2
6	XTI crystal driver	fXTI	3.58	-	20	MHz	3
7	HCLK frequency	fHCLK	1	-	30	MHz	
8	HCLK high pulse width	$tHCLK_{wh}$	10	-	-	nS	
9	HCLK low pulse width	$tHCLK_{wl}$	10	-	-	nS	
10	HCLK rise time	$tHCLK_{l}$	-	-	5	nS	
11	HCLK fall time	$tHCLK_{f}$	-	-	5	nS	

8.5. Timing Characteristics,continued

	Parameter	Symbol	Min	Typ	Max	Units	Notes
Reset							
1	RSTN	tRST	4	-	-	cycle	
Host Interface at Type 1 (figure 8-2, 8-3)							
1	Access time	t_{acc}	100	-	-	nS	4
2	Address setup time	tA_{su}	10	-	-	nS	
3	Address hold time	tA_{h}	5	-	-	nS	
4	D[15:0] output delay time	tD_{od}	-	-	30	nS	5,6
5	D[15:0] output hold time	tD_{oh}	10	-	-	nS	5,7
6	D[15:0] input setup time	tD_{su}	10	-	-	nS	8
7	D[15:0] input hold time	tD_{h}	5	-	-	nS	9
8	DMA request delay time	$tDRQ_{d}$	-	-	20	nS	2
9	DMA request hold time	$tDRQ_{h}$	5	-	-	nS	2
Host Interface at Type 2 (figure 8-4)							
1	Input signals setup time	$tIF2_{su}$	10	-	-	nS	10
2	Input signals hold time	$tIF2_{h}$	5	-	-	nS	10
3	Address setup time	$tA2_{su}$	10	-	-	nS	
4	Address hold time	$tA2_{h}$	5	-	-	nS	
5	XRDYN delay time	$tRDY_{d}$	-	-	20	nS	2
6	XRDYN hold time	$tRDY_{h}$	5	-	-	nS	2
7	D[15:0] output delay time	tD_{od}	-	-	30	nS	5
8	D[15:0] output hold time	tD_{oh}	10	-	-	nS	5
9	D[15:0] input setup time	tD_{su}	10	-	-	nS	
10	D[15:0] input hold time	tD_{h}	5	-	-	nS	
Interrupt (figure 8-3)							
1	Interrupt delay time	$tINT_{d}$	-	-	20	nS	
Serial Interface Signals (figure 8-5)							
1	MS1 output delay	$tMS1_{d}$	0	-	5	nS	2
2	MS2 output delay time	$tMS2_{d}$	-	-	30	nS	2
3	MS2 input setup time	$tMS2_{su}$	10	-	-	nS	
4	MS2 input hold time	$tMS2_{h}$	5	-	-	nS	

Note 1: External clock input.

Note 2: 20 pF output loading.

Note 3: Crystal driver.

Note 4: Minimum active pulse width of (XCSN and XRDN) or (XCSN and XWRHN and XWRLN).

Note 5: 40 pF output loading.

Note 6: From the last active signal of XCSN or XRDN.

Note 7: From the first in-active signal of XCSN or XRDN.

Note 8: To the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].

Note 9: From the first in-active signal of XCSN, XWRHN or XWRLN, XWRHN or XWRLN related to the D[15:8] or D[7:0].

Note 10: XCSN, XASN, XRWN and XBE[1:0] signals.

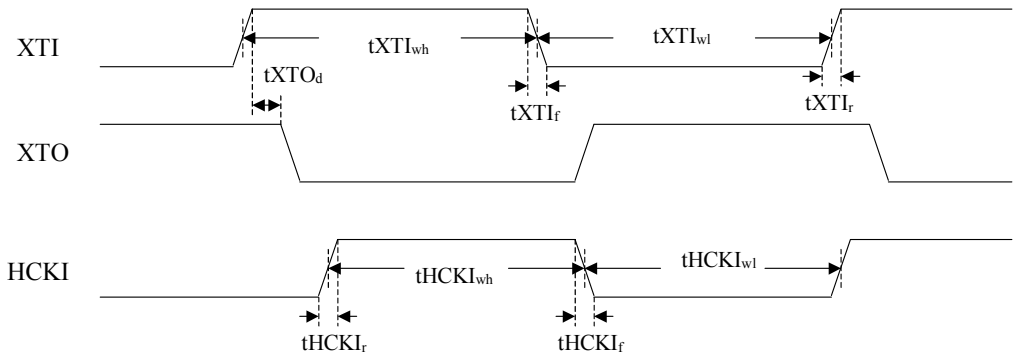


Fig. 8-1 Timing Characteristic of XTI, XTO and HCKI.

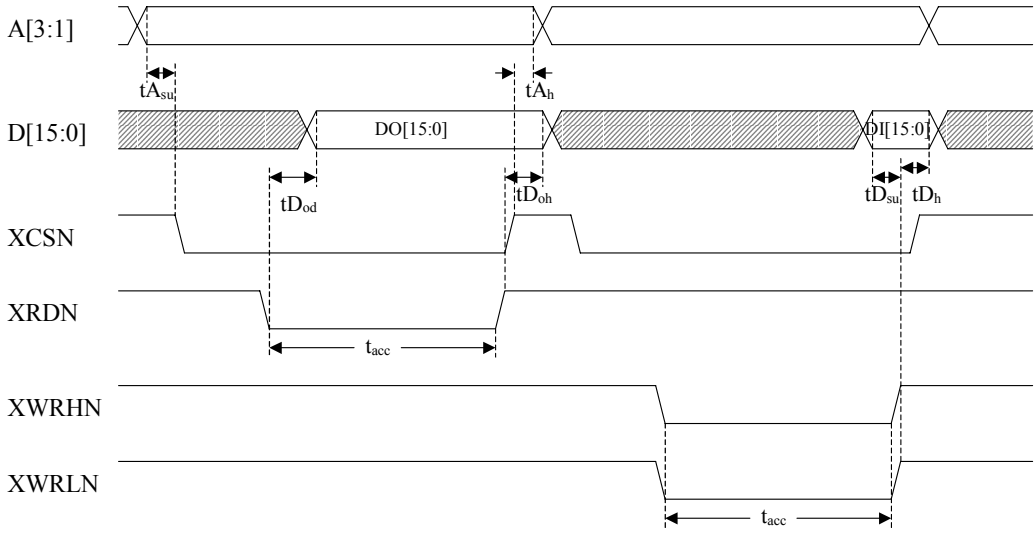


Fig. 8-2 Host Access Timing Characteristic in Host I/F Type 1.

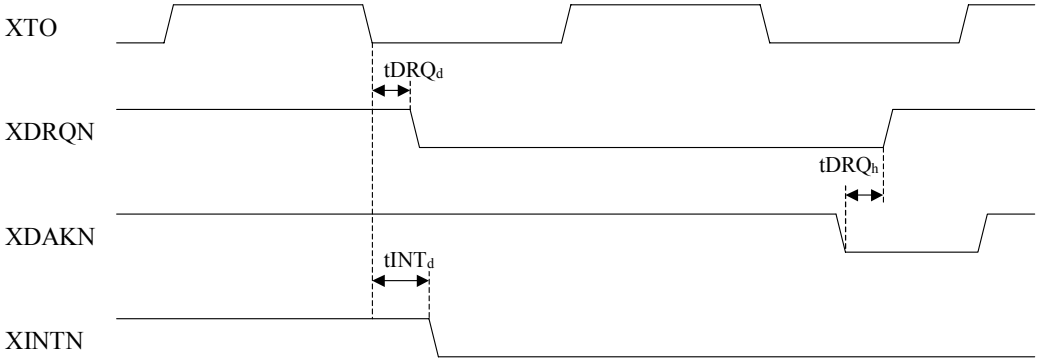


Fig. 8-3 DMA and Interrupt Timing Characteristic.

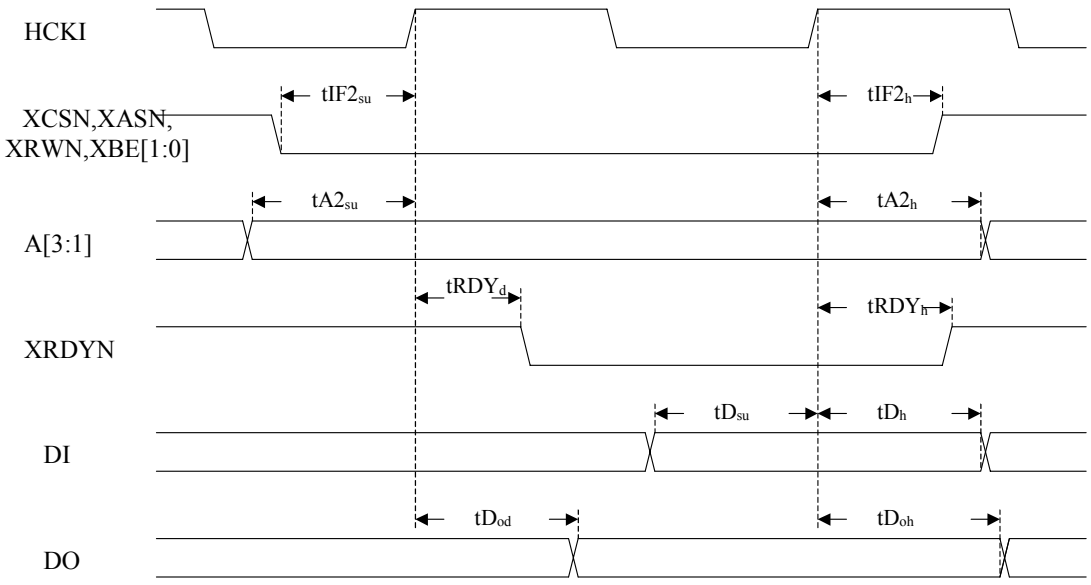


Fig. 8-4 Host Interface Type 2 Timing Characteristic.

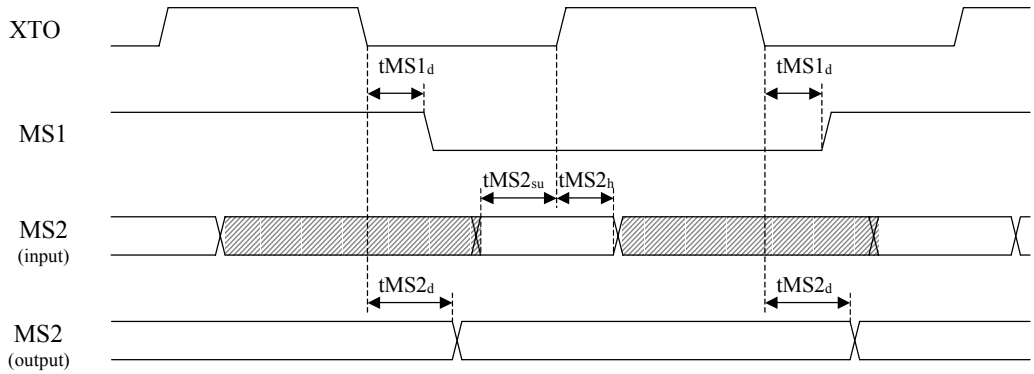
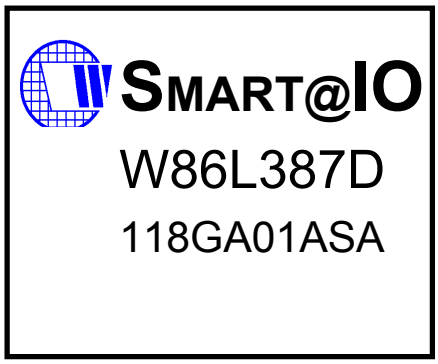


Fig. 8-5 Serial Interface Timing Characteristic.

9. HOW TO READ THE TOP MARKING

The top marking of W86L387D



1st line: Winbond logo and SMART@IO Mark

2nd line: Part number of W86L387D

3rd line: Tracking code 118 G A 01A SA

118: packages made in '01, week 18

G: assembly house ID; A means ASE, O means OSE, G means GR

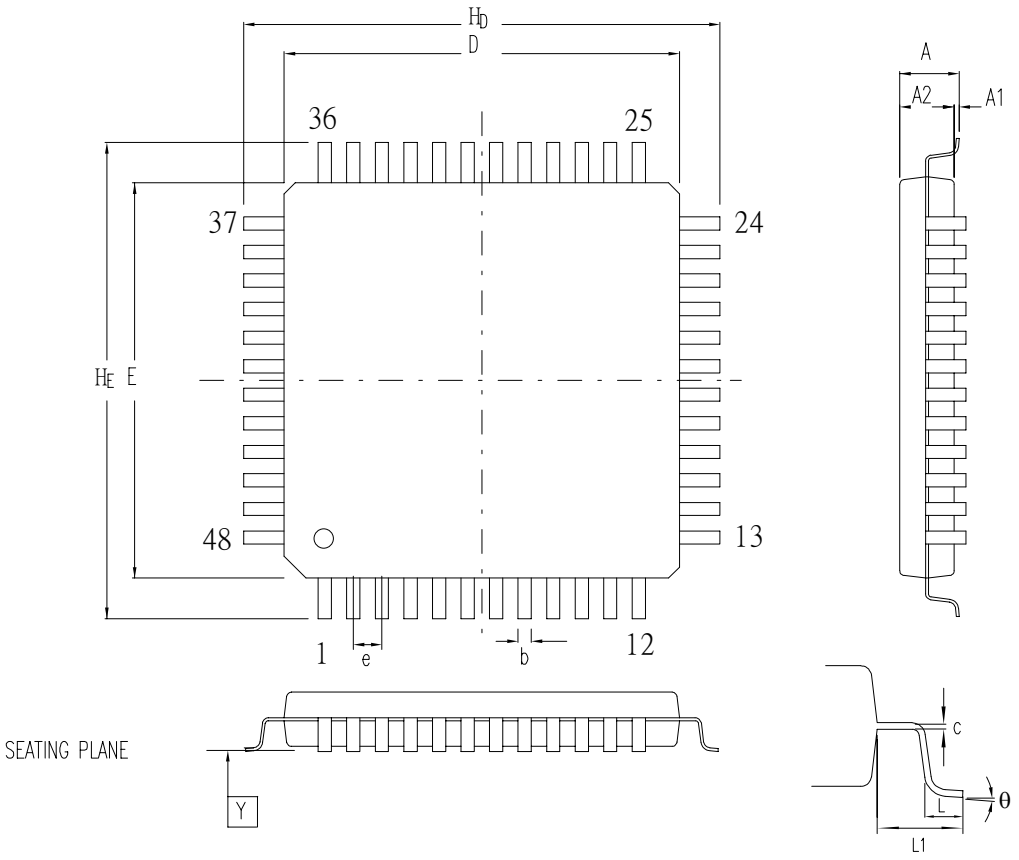
A: IC revision; A means version A, B means version B

01A: for internal use

SA: for internal use

10. PACKAGE DIMENSIONS

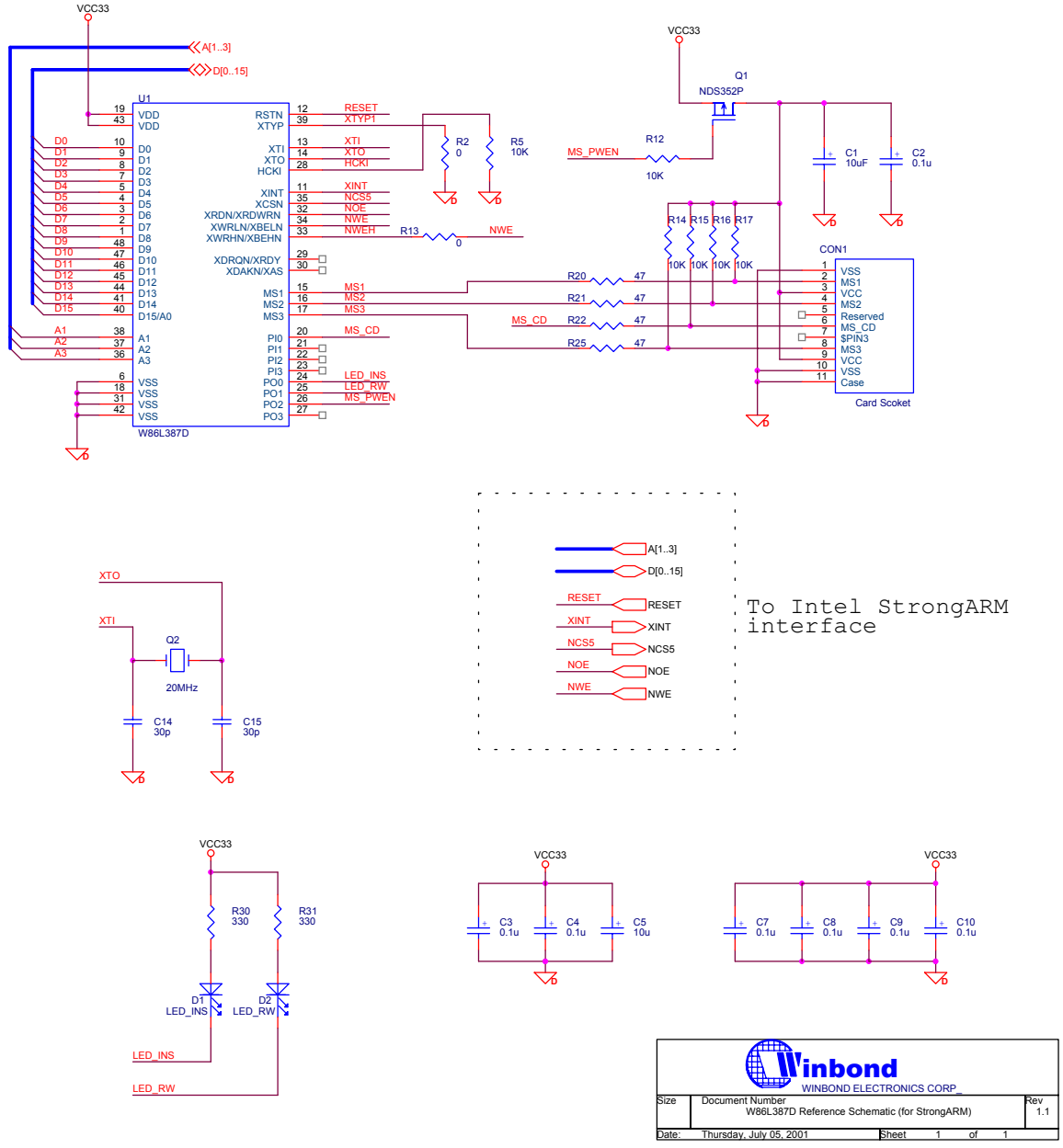
48-LQFP(7x7x1.4mm footprint 2.0mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7 °	0°	—	7 °

11. REFERENCE SCHEMATIC



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