Preliminary W91031

CALLING LINE IDENTIFIER

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GENERAL DESCRIPTION

The Winbond Caller Identification device W91031, is a low power CMOS integrated circuit used to receive physical layer signals transmitted according to Bellcore and British Telecom (BT) specifications. There are two types of Caller Identifications, the first type is on-hook calling with caller ID message and the second type is call on waiting. The W91031 device provides all the features and functions of the Caller Identification specification for both these types, including FSK demodulation, Tone Alert Signal detection and ring detection. The FSK demodulation function can demodulate Bell 202 and CCITT V.23 Frequency Shift Keying (FSK) with 1200 baud rate. The Tone Alert Signal detect function can detect the dual tones of the Bellcore CPE* Tone Alerting Signal (CAS) and the BT idle State and Loop State Tone Alert Signal. The line reversal for BT, ring burst for CCA or ring signal for Bellcore can be detected by the ring detector.

There are two modes of FSK data output interface. The first mode is a data transfer activated by the device, whose clock and data change depending upon the changing frequency of the FSK analog signal input. The second mode allows a microcontroller to extract 8-bit data from the device serially; the device notifies the micro-controller when 8-bit data has been received.

Note: "CPE*" Customer Primises Equipment

FEATURES AND APPLICATIONS

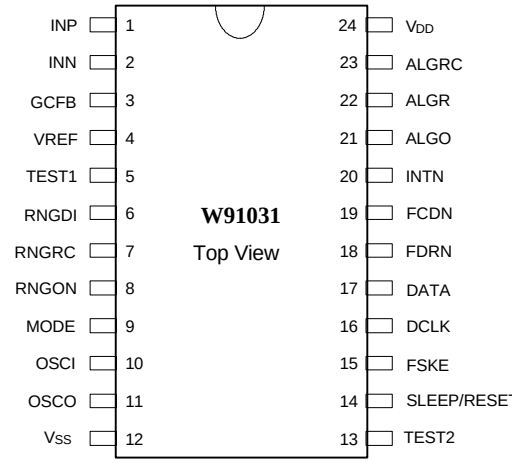
Features

- Compatible with Bellcore TR-NWT-000030 & SR-TSV-002476, British Telecom (BT) SIN227, U.K. Cable Communications Association (CCA) specification
- Ring and line reversal detection
- Bellcore CPE Alerting Signal (CAS) and BT idle State and Loop State Tone Alerting Signal detection use dual tone alerting signal detector
- BELL 202 and CCITT V.23 FSK demodulation with 1200 baud rate
- Use 3.579545 MHz crystal or ceramic resonator
- Low power CMOS technology with sleep mode
- High input sensitivity
- Variable gain input amplifier
- FSK carry detect output
- Two modes for 3-wire FSK data interface
- Packaged in 24-pin 0.6 inch (600 mil) plastic DIP and 24-pin 0.3 inch (300 mil) plastic SOP

Applications

- Bellcore Calling Identity Delivery (CID), and BT Calling Line Identity Presentation (CLIP), CCA CLIP systems
- Feature phones
- Phone set adjunct boxes
- FAX and answering machines
- Data base telephone system and Computer Telephony Integration (CTI) systems

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	INP	I	Non-inverting Input of the gain control op-amp.
2	INN	I	Inverting Input of the gain control op-amp.
3	GCFB	O	Op-amp Feed-back Gain Control signal. Select the input gain by connecting this pin and the INN pin with a feed-back resistor. It is recommended that the op-amp be set to unity gain.
4	VREF	O	Reference Voltage. Nominally, VDD/2 is used to bias the input of the gain control op-amp.
5	TEST1	I	Test pin, Must be connected to VDD for normal operation.
6	RNGDI	I	Ring Detect Input (Schmitt trigger input). Used for ring detection and line reversal detection. Must maintain a voltage between VDD and VSS.
7	RNGRC	O	Ring RC (Open drain output and schmitt trigger input). Used to set the time interval from the end of RNGDI pin to the inactive condition of the RNGON pin. An external resistor must connected to VDD and a capacitor connected to VSS, the time interval is the RC time constant.
8	RNGON	O	Ring detection output (Low active). Indicates the detection of line reversal and/or ringing.
9	MODE	I	FSK Data interface MODE select. Sets the FSK data output interface in mode 0 when low, or in mode 1 when high.
10	OSCI	I	Oscillator Input. A 3.579545 MHz crystal or ceramic resonator should be connected between this pin and the OSCO pin. May be driven by an external clock source.

Pin Descriptions, continued

PIN	NAME	TYPE	DESCRIPTION
11	OSCO	O	Oscillator Output. A 3.579545 MHz crystal or ceramic resonator should be connected between this pin and the OSCI pin. Should left open or to drive another clocked device when an external clock is connected to the OSCI pin.
12	VSS	I	Power Supply Ground.
13	TEST2	I	Test pin. Must be connected to VSS for normal operation.
14	SLEEP/ RESET	I	Reset or Sleep Input (Schmitt input). When high the device will be reseted and enter a low power state by disabling the gain control op-amp, the oscillator and other internal circuits. The function of RNGDI, RNGRC and the RNGON pins are not affected when the device is in a sleep condition. This pin must be set low for normal operation. The device must reseted by micro controller or by external RC pulse after power on.
15	FSKE	I	FSK Enable. Must be set high when for FSK demodulation. Should be set low to disable the FSK demodulator and enable the dual tone alert signal detector when a dual tone alert signal is expected.
16	DCLK	I, O	Data Clock for the FSK interface. In the FSK data output interface mode 0 (MODE pin low), this pin is an output with a changing FSK frequency. In the FSK interface mode 1, this pin is an input.
17	DATA	O	Data signal for the FSK interface. Serial data output according to the FSK frequency input in FSK data output interface mode 0 (MODE pin low). Data is shifted out on the rising edge of DCLK in FSK data output interface mode 1. Both logic 1 for mark and logic 0 for space.
18	FDRN	O	Data Ready of the FSK interface (Low active). In FSK interface mode 0 (MODE pin low), this pin identifies the 8-bit data boundary on the serial output string. In FSK interface mode 1, this pin is used to notify the micro-controller to extract the 8-bit data (ie. 8-bit data has been ready internally).
19	FCDN	O	FSK Carrier Detect (Low active). When low, it indicates the FSK signal has been detected.
20	INTN	O	Interrupt signal (open drain). It is used to interrupt the microcontroller when RNGON or FDRN are low, or if ALGO is high. Remains low until all three signals have become inactive.
21	ALGO	O	Dual tone Alert signal Guard time detect Output. When high, a guard time qualified for the dual tone alert signal has been detected.
22	ALGR	O	Dual tone Alert signal Guard time Resistor. Also functions as a dual tone alert signal detect output without guard time. An external resistor must connected between this pin and ALGRC to implement guard time detection.
23	ALGRC	I	Dual tone Alert signal Guard time RC (CMOS output and internal voltage comparator input). An external resistor must be connected between this pin and ALGR and an external capacitor between this pin and VDD to implement guard time detection.
24	VDD	I	Power supply input.

SYSTEM DIAGRAM

The W91031 device applications include telephone systems which have caller ID features and which can display the calling message on an LCD display. Figure 5 shows the system diagram. It illustrates how to use the chip to connect between the tip/ring and the microcontroller in the telephone system. The ring signal is detected by the W91031 device and then an interrupt sent to the microcontroller. The ring detected signal will also be directed to the ringer circuit. The data can be decoded by the microcontroller and displayed on the LCD display. The DTMF ACK signal can also be generated by the DTMF generator if a call on waiting is performed. Other functions are the same as the telephone set.

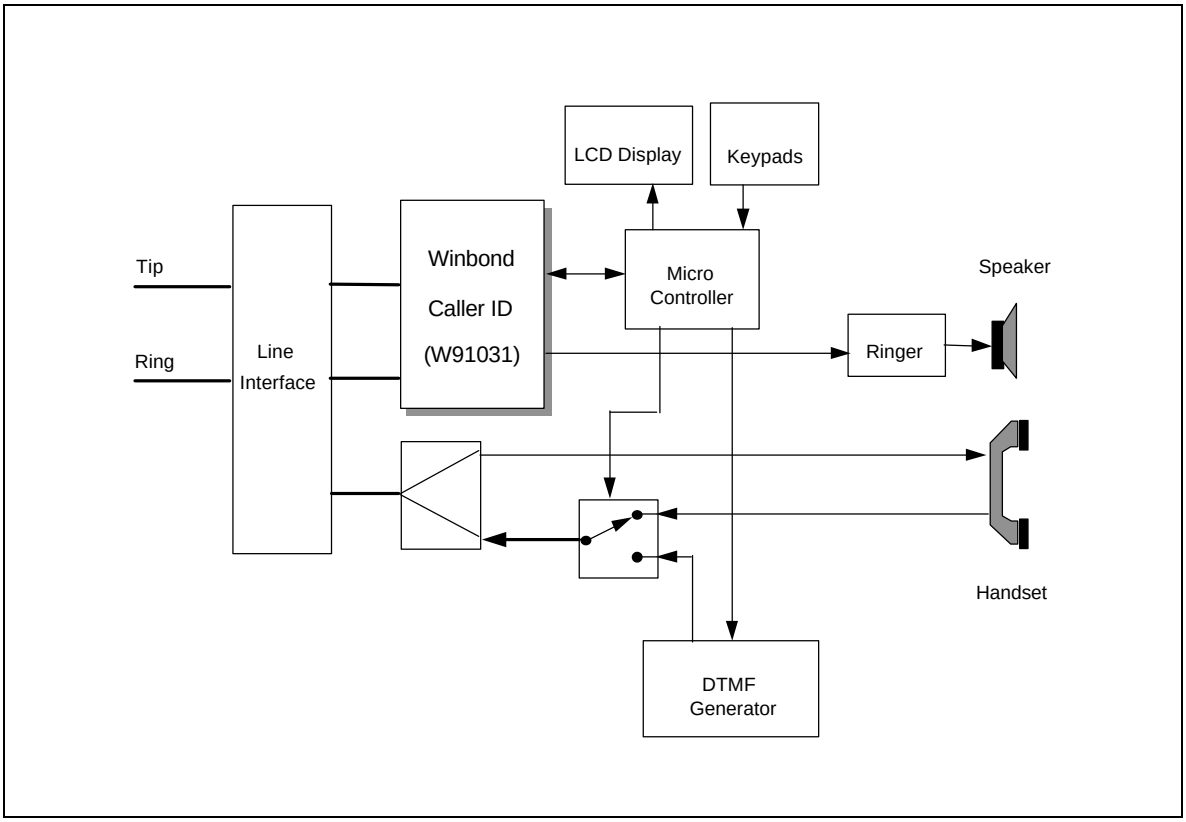


Figure 5. System Diagram for Caller ID Application

BLOCK DIAGRAM

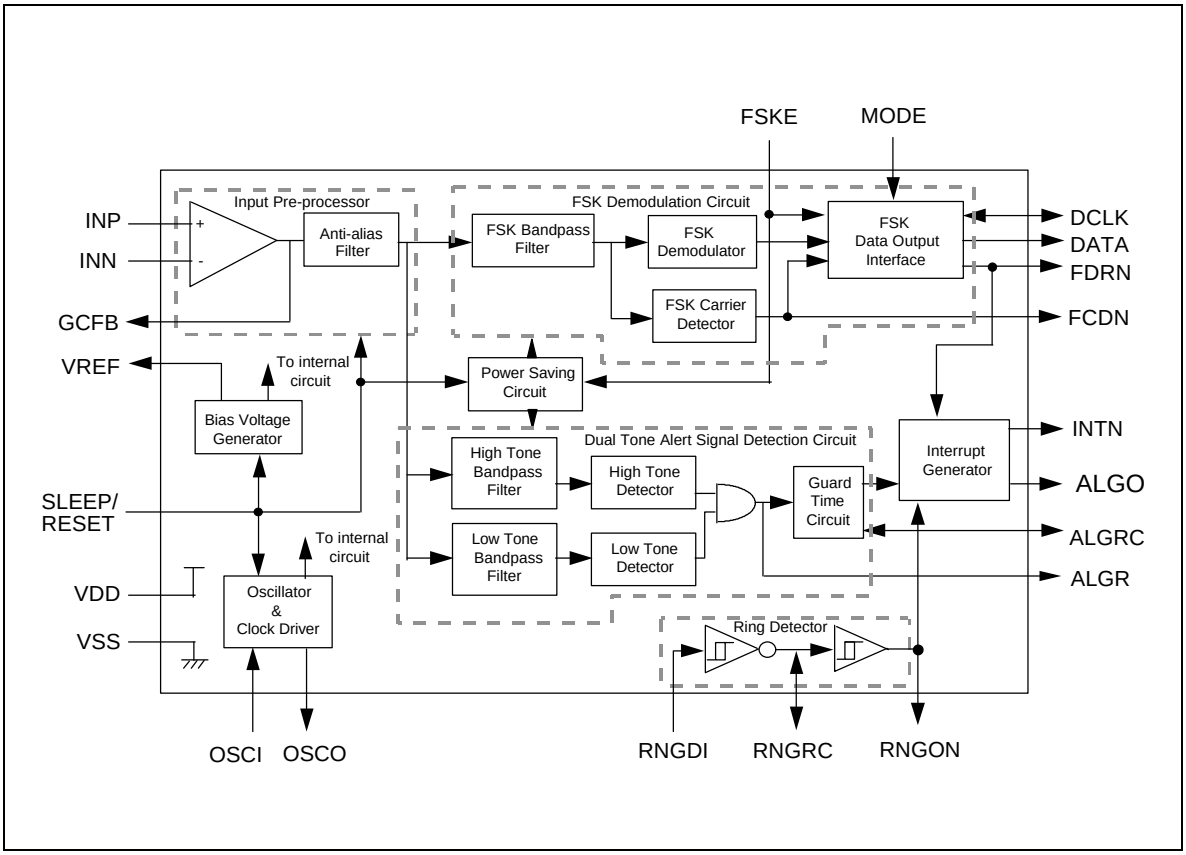


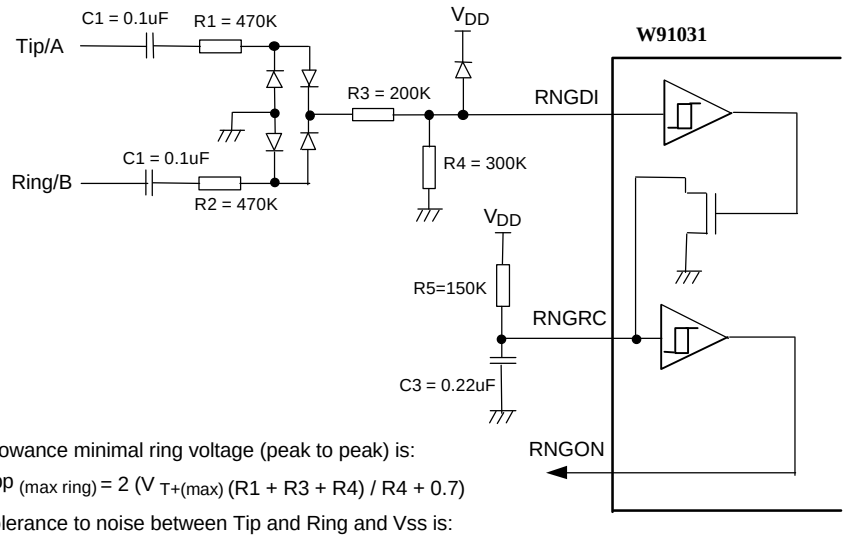
Figure 6. The Block Diagram of Winbond Caller ID

FUNCTIONAL DESCRIPTION

Figure 6 is shown functional blocks of W91031. The device must operate with a 3.579545 MHz system clock and consists four major functions and decribed as follows:

Ring Detector

The application circuit in Figure 7-1 illustrates the relationship between the RNGDI, RNGRC and RNGON signals. The three pin combination is used to detect an increase of the RNGDI voltage from ground to a level above the Schmitt trigger high going threshold voltage V_{T+}.



Allowance minimal ring voltage (peak to peak) is:

$Vpp_{(max\ ring)} = 2\ (V_{T+(max)}\ (R1 + R3 + R4) / R4 + 0.7)$

Tolerance to noise between Tip and Ring and Vss is:

$Vpeak_{(max\ noise)} = V_{T+(min)}\ (R1 + R3 + R4) / R4 + 0.7$

Time constant is:

$T = R5\ C3\ \ln [V_{DD} / (V_{DD} - V_{T+})]$

$V_{T+(min)} <= V_{T+} <= V_{T+(max)}$

R5 from 10K ohm to 500K ohm.
C3 from 47 nF to 0.68 uF.

Figure 7-1. Application Circuit of the Ring Detecter

The RC time constant of the RNGRC pin is used to delay the output pulse of the RNGON pin for a low going edge on RNGDI. This edge goes from above the V_{T+} voltage to the Schmitt trigger low going threshold voltage V_{T-}. The RC time constant must be greater than the maximum period of the ring signal, to ensure a minimum RNGON low interval and to filter the ring signal to get an envelope output.

The diode bridge shown in Figure 7-1 works for both single ended ring signal and balanced ringing. R1 and R2 are used to set the maximum loading and must be of equal value to achieve balanced loading at both the tip and ring line. R1, R3 and R4 form a resistor divider to supply a reduced voltage to the RNGDI input. The attenuation value is determined by the detection of minimal ring voltage and maximum noise tolerance between tip/ring and ground.

Input Pre-processor

The input signal is processed by an Input Pre-processor, which is added to the offset voltage to adjust the input amplitude and to filter out unwanted frequencies. The gain control op-amp is used to bias the input voltage with the VREF signal voltage. The voltage of VREF pin is $V_{DD}/2$ typically, this pin must connected a 0.1 µF capacitor to V_{SS}. It is also used to select the input gain by connecting a feedback resistor between this pin and the INN pin. Figure 7-2 shows the necessary connections with the tip/ring line inputs. In a single-ended configuration, the gain control op-amp is connected as shown in Figure 7-3.

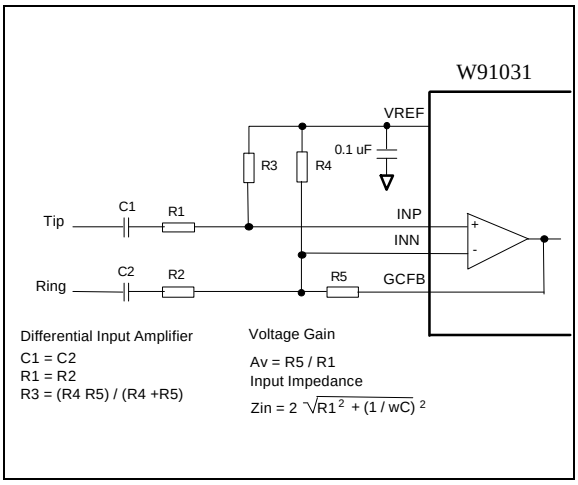


Figure 7-2 Differential Input Gain Control Circuit

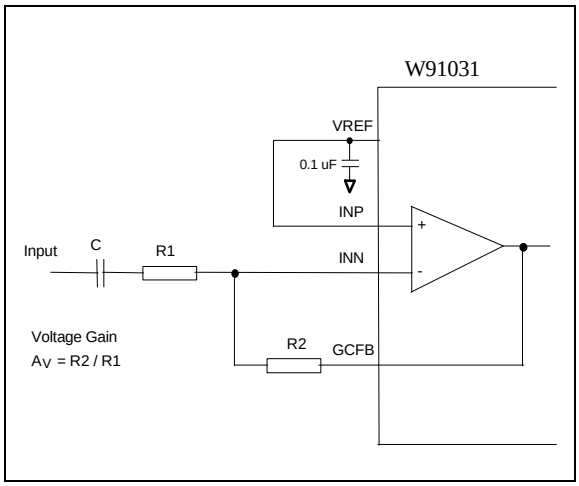


Figure 7-3 Single-ended Input Gain Control Circuit

Dual Tone Alert Signal Detection

The dual tone alert signal is separated into high and low tones and detected by a high/low tone detector. The dual tone alert signal detection circuit is enabled when the FSKE signal is low. It requires an enable time to enable the dual tone alert signal detector when FSKE goes from high to low. The ALGR is the output of the dual tone detector and when high indicates that the high tone and low tone alert signals have been detected. The guard time improves detection performance by rejecting detected signals with insufficient duration and by masking momentary detection dropout.

Figure 7-4 shows the relationship between the ALGR, ALGRC and ALGO pins and Figure 7-5 shows the guard time waveform of the same pins. The total recognition time is $t_{REC} = t_{DP} + t_{GP}$, where t_{DP} is the tone present detect time and t_{GP} is the tone present guard time. The tone present guard time is the RC time constant with the capacitor discharging from V_{SS} to V_{DD} (the ALGRC pin discharges from V_{SS} to V_{DD} through a resistor). The capacitor will discharge rapidly via a discharge switch after ALGO returns high. The total absent time is $t_{ABS} = t_{DA} + t_{GA}$, where t_{DA} is the tone absent detect time and t_{GA} is the tone absent guard time. The tone absent guard time is the RC time constant with the capacitor charging from V_{DD} to V_{SS} (the ALGRC pin charges from V_{DD} to V_{SS} through a resistor). The capacitor will charge rapidly via a charge switch after ALGO returns low. To obtain unequal present and absent guard times, a diode can be connected as shown in Figure 7-6, to give the unequal resistance required during capacitor charging and discharging.

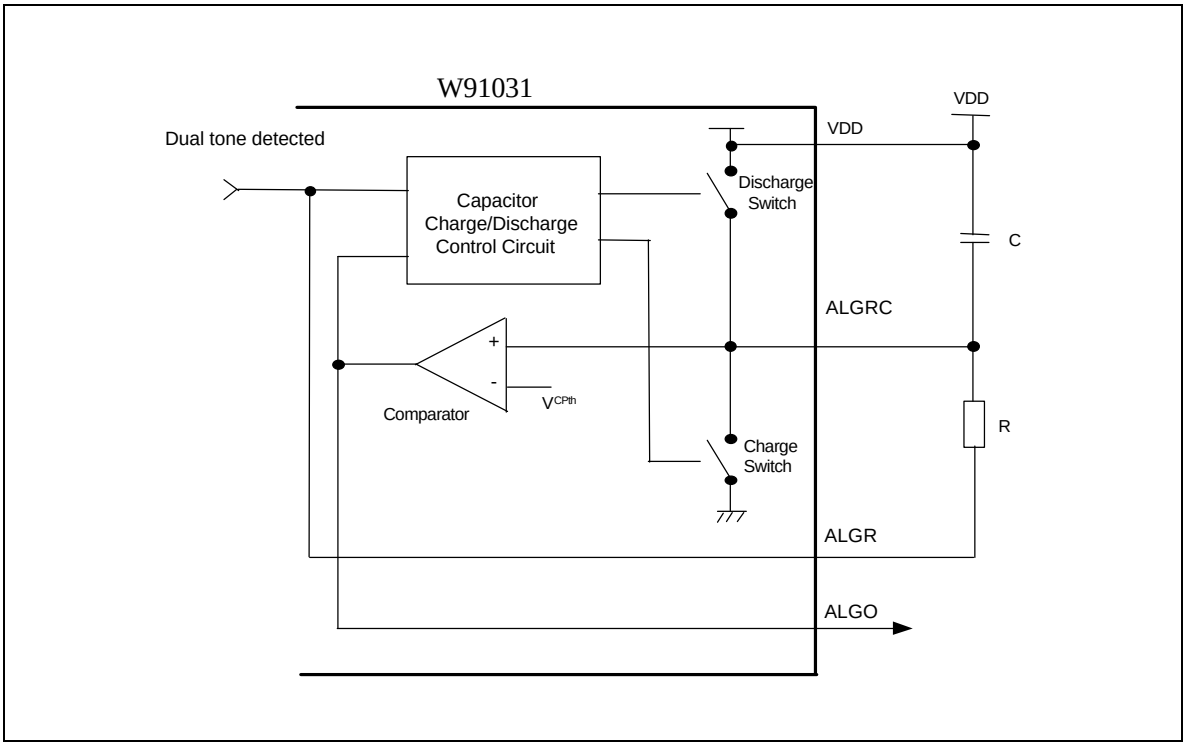


Figure 7-4. Guard Time Circuit of Dual Tone Alert Signal Detection

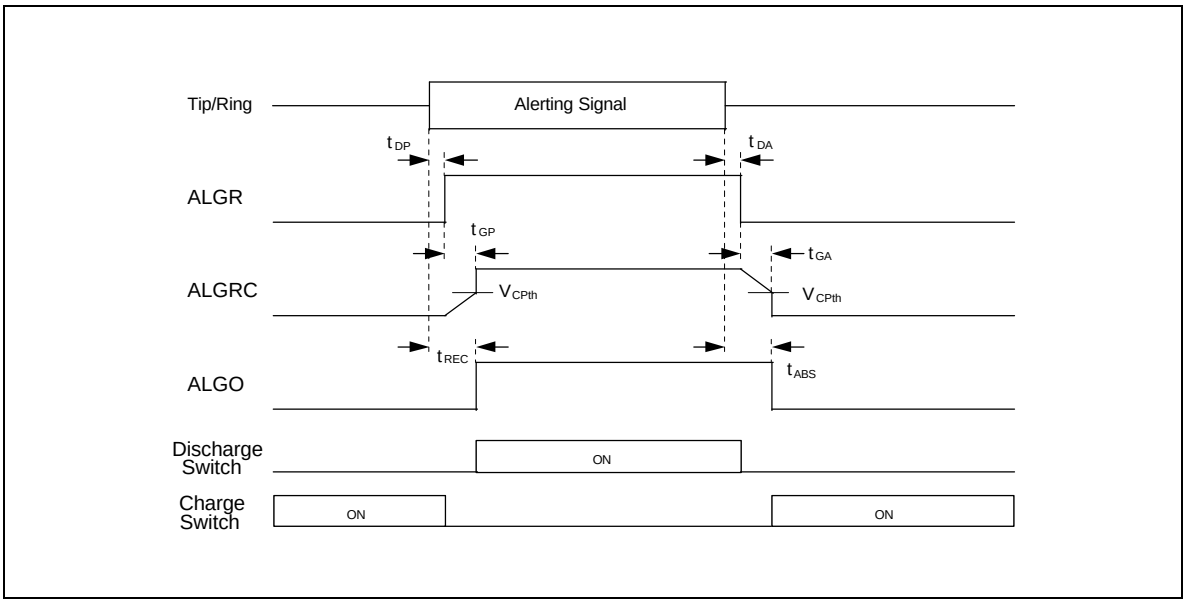


Figure 7-5. Guard Time Waveform of ALGR, ALGRC and ALGO Pins

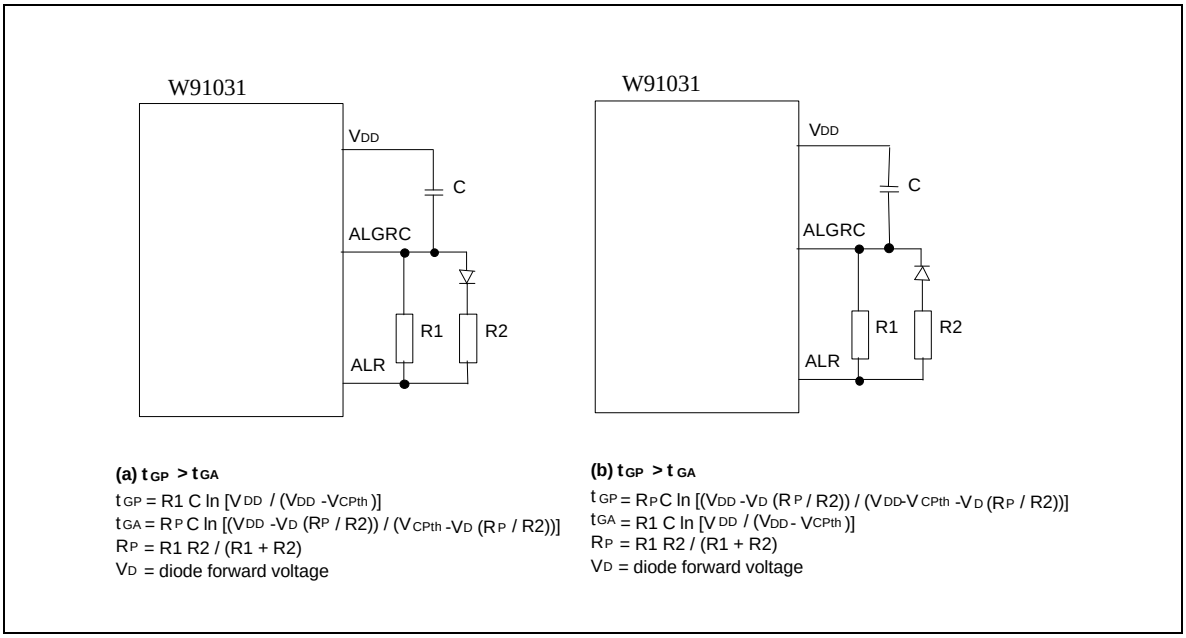


Figure 7-6. Guard Time Circuits with Unequal Present and Absent Time

FSK Demodulation

The FSK demodulation circuit is enabled when the FSKE signal is high. An enable time is required to enable the FSK demodulator circuitry after the FSKE signal goes from low to high.

FSK Carrier Detector

The FSK carrier detector provides an indication of the presence of a signal within the FSK frequency band. If the output amplitude of the FSK bandpass filter is of sufficient magnitude and holds for 8 mS, the FSK carrier detect output signal FCDN goes low. FCDN will be released if the FSK bandpass filter output amplitude is of insufficient magnitude for greater than 8 mS. The 8 mS hysteresis of the FSK carrier detector is to allow for momentary signal drop out after FCDN has been activated.

When FCDN is inactive, the output of the FSK demodulator is ignored by the FSK data output interface. In mode 0 of the 3-wire FSK data output interface, DCLK DATA and FDRN are all high and no clock and no data is driven. In mode 1, the internal shift registers are not updated, and FDRN is inactive (high state). The DATA is undefined if DCLK is clocked.

3-wire FSK Interface

The 3-wire interface, DCLK, DATA and FDRN pins, form the data interface of the FSK demodulation. The DCLK pin is the data clock which is either generated by the W91031 or by an external device. The DATA pin is the serial data pin that outputs data to external devices. The FDRN pin is the data ready signal, also an output from the W91031 to external devices. There are two modes of this 3-wire interface that can be selected. Mode 0, where the data transfer is initiated by the W91031 device, or Mode 1, where the data transfer is initiated by an external microcontroller.

Mode 0 (MODE = low):

The W91031 processes the FSK signal and outputs signals on the DCLK, DATA and FDRN pins. Figure 7-7 shows the timing diagram of the 3-wire signals and the input of the FSK signal in mode 0. For each received stop and start bit sequence, the device outputs a fixed frequency clock string of 8 pulses on the DCLK pin. Each clock rising edge occurs in the middle of each data bit. DCLK is not generated for the stop and start bits. The DCLK pin is used as a clock driving signal for a serial to parallel shift register or for a serial data input for a microcontroller. After the 8-bit data has been shifted out by the device, the FDRN pin will supply a low pulse to inform the microcontroller to process the 8-bit data.

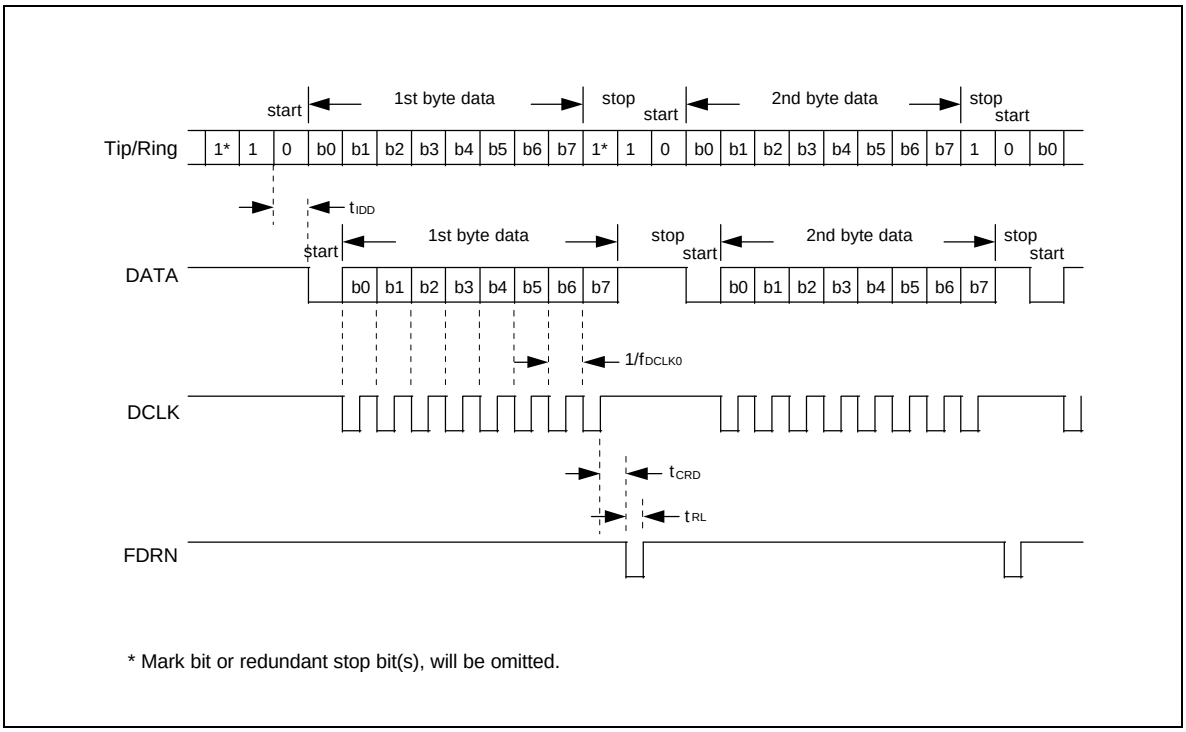


Figure 7-7. Serial Data Interface Timing of FSK Demodulation in Mode 0

Mode 1 (MODE = high):

The W91031 processes the FSK signal and sets the FDRN pin low to denote the 8-bit boundary and to indicate to the microcontroller that new data has been transmitted. FDRN will return high on the first rising edge of DCLK. FDRN is low for half of a nominal bit time (1/2400 sec) if DCLK is not driven high. DCLK is used to shift 8-bit data out (LSB shift first) on the rising edge. After the last bit (MSB) has been read, additional clock pulses on DCLK are ignored. Figure 7-8 shows the timing diagram of the 3-wire signals and the input of the FSK signal in mode 1.

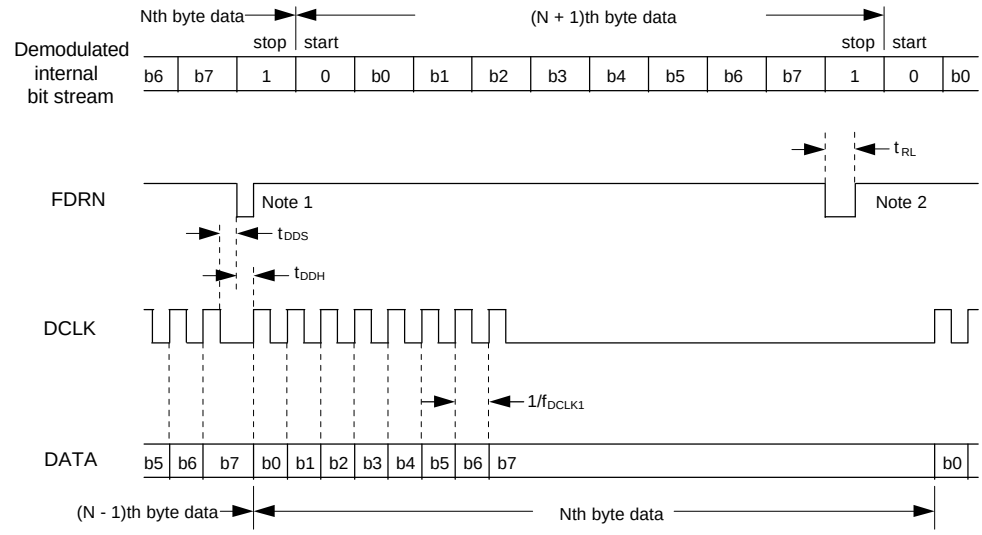


Figure 7-8. Serial Data Interface Timing of FSK Demodulation in Mode 1

Other Functions

Interrupt

The interrupt INTN is an open drain output and is used to interrupt the microcontroller. Either RNGON low, FDRN low or ALGO high will set INTN low and will remain low until all of these three pins return to an inactive state. The microcontroller must read these pins to know what kind of interrupt occurred and to make the correct interrupt response.

When the system is powered on, there is no charge on the capacitors. The voltage on the RNGRC pin is low and RNGON will be low. Also the voltage on the ALGRC pin is high and ALGO will be high if the SLEEP pin is low. This will cause an interrupt upon power up which will not be cleared until both capacitors are charged. The microcontroller should therefore ignore the interrupt from these source until the capacitors are charged up. The microcontroller can examine the RNGON and ALGO pins and wait until these signals are inactive during a power on interrupt.

It is possible to clear the ALGO pin and its interrupt quickly by setting the SLEEP pin high. In the sleep mode, the ALGO pin is forced low and the charge switch in Figure 7-4 will turn on, forcing the capacitor to charge up rapidly.

Sleep Mode

The W91031 can go into a sleep mode by setting SLEEP high, resulting in reduced power consumption. In this mode, the gain control op-amp, oscillator and all internal circuits, except the ring detector are disabled. The RNGDI, RNGRC and RNGON pins are not affected, so the device can still react to call arrival indicators and activate an interrupt to wake up the microcontroller. The sleep mode can be disabled by the microcontroller.

Crystal Oscillator

The operation frequency of the W91031 is 3.579545 MHz. Crystal oscillators, ceramic resonators or other clock sources can be used. A crystal oscillator or ceramic resonator can be directly connected to the OSCI and OSCO pins without the need for external components. If other clock sources are used, the OSCI pin should be driven by a clock source and the OSCO pin used to drive other external clocked devices, or left open. Figure 7-9 shows some applications.

The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency tolerance:	+/- 0.1 % (-40° C to +85° C)
Resonance mode:	Parallel
Load capacitance:	18 pF
Maximum series resistance:	150 Ω
Maximum drive level (mV):	2 mV

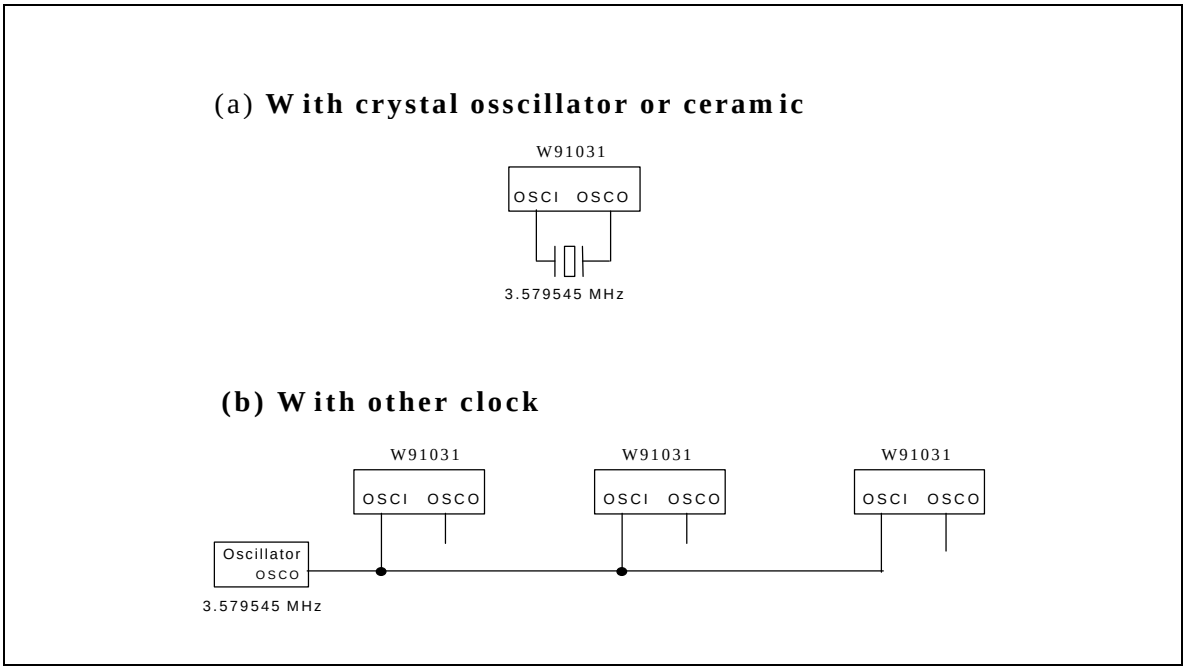


Figure 7-9. Some Application of Clock Driven Circuit

Bias Voltage Generator

The bias voltage generator provides a low impedance voltage source equal to $V_{DD}/2$ and is used to bias the gain control op-amp. The voltage source is also used for internal circuits. A 0.1 µF capacitor should be placed between the VREF pin and V_{SS} to reduce noise.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(Voltage referenced to V_{SS} pin)

PARAMETER	SYMBOL	RATING	UNITS
Supply Voltage with Respect to V_{SS}	V_{DD}	-0.3 to 6	V
Voltage on Any Pin Other Than Supplies (Note 1)		-0.7 to V_{DD} + 0.7	V
Current on Any Pin Other Than Supplies		0 to 10	mA
Storage Temperature	T_{st}	-65 to 150	°C

Notes:

1. V_{DD} +0.7 should not exceed the maximum rating of the supply voltage.
2. Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Recommended Operating Conditions

(Voltages referenced to V_{SS})

PARAMETER	SYMBOL	RATING	UNIT
Power Supplies	V_{DD}	3.0 to 5.5	V
Clock Frequency	F_{OSC}	3.579545	MHz
Clock Frequency Tolerance	Δf_C	-0.1 to +0.1	%
Operational Temperature	T_{OP}	0 to 75	°C

DC Electrical Characteristics

(V_{DD}–V_{SS} = 3.0V. The DC electrical characteristics supersede the recommended operating conditions unless otherwise stated.)

PARAMETER	CONDITION	SYM.	MIN.	TYP.*	MAX.	UNITS	TEST/ NOTES
Operating Supply Voltage			3.0		5.0		
Standby Supply Current		I_{DDQ}			1	µA	Test 1
Operating Supply Current	V_{DD} = 3.0V FSKE = FSK Mode	I_{DD1}		1.0	1.4	mA	Test 2
	V_{DD} = 3.0V FSKE = Alert Mode	I_{DD2}		1.6	2.3		
	V_{DD} = 5.0V FSKE = FSK Mode	I_{DD1}		1.6	2.3		
	V_{DD} = 5.0V FSKE = Alert Mode	I_{DD2}		2.5	3.6		

DC Electrical Characteristics, continued

PARAMETER	CONDITION	SYM.	MIN.	TYP.*	MAX.	UNITS	TEST/ NOTES
Schmitt Input High Threshold Schmitt Input Low Threshold	RNGDI, RNGRC SLEEP	VT+ VT-	0.48 V_{DD} 0.28 V_{DD}		0.68 V_{DD} 0.48 V_{DD}	V V	
Schmitt Hysteresis		VHYS	0.2			V	
CMOS Input High Voltage CMOS Input Low Voltage	DCLK, MODE, FSKE	V_{IH} V_{IL}	0.7 V_{DD} V_{SS}		V_{DD} 0.3 V_{DD}	V	
Output High Source Current	RGNON, DCLK, DATA, FDRN, FCDN, ALGO, ALGRC, ALGR	I_{OH}	0.5			mA	Note 1
Output Low Sink Current	RGNON, DCLK, DATA, FDRN, FCDN, ALGO, ALGRC, ALGR, INTN	I_{OL}	0.5			mA	Note 2
	RNGRC	I_{OL}	2.5			mA	Note 2
Input Current 1	INP, INN, RNGDI	I_{IN1}			1	µA	Note 3, 5
Input Current 2	SLEEP, DCLK, MODE, FSKE	I_{IN2}			10	µA	Note 3, 5
Output High-Z Current 1	RNGRC	I_{OZ1}			1	µA	Note 4, 5
Output High-Z Current 2	ALGRC	I_{OZ2}			5	µA	
Output High-Z Current 3	INTN	I_{OZ3}			10	µA	
Reference Output Voltage	VREF	VRef	0.5 V_{DD} -4%		0.5 V_{DD} +4%	V	Note 6
Reference Output Resistance	VREF	RRef			2	KΩ	
Comparator Threshold Voltage	ALGRC	VCPth	0.5 V_{DD} -4%		0.5 V_{DD} +4%	V	

Tests:

1: All input pins are V_{DD} or V_{SS} except for oscillator pins, no analog inputs, output unloaded and SLEEP = V_{DD}.

2: All input pins are V_{DD} or V_{SS} except for oscillator pins, no analog inputs, output unloaded, SLEEP = V_{SS} and FSKE = V_{DD} or FSKE = V_{SS}.

Notes:

" * " Typical figure are at V_{DD} = 5V and temperature = 25° C are design aids only, not guaranteed and not subject to production testing.

1. V_{OH} = 0.9 V_{DD}.
2. V_{OL} = 0.1 V_{DD}.
3. V_{IN} = V_{DD} to V_{SS}.
4. V_{OUT} = V_{DD} to V_{SS}.
5. Magnitude measurement, ignore signs.
6. Output - no load.

Electrical Characteristics - Gain Control OP-Amplifier

(Electrical characteristics supersede the recommended operating conditions unless otherwise stated.)

PARAMETER	SYM.	MIN.	TYP.*	MAX.	UNITS	TEST CONDITIONS
Input Leakage Current	I_{IN}			1	uA	$V_{SS} \le V_{IN} \le V_{DD}$
Input Resistance	R_{IN}	10			MΩ	
Input Offset Voltage	V_{OS}			25	mV	
Power Supply Rejection Ratio	PSRR	40			dB	1 KHz 0.1 Vpp ripple on V_{DD}
Maximum Capacitive Load (GCFB)	C_L			100	pF	
Maximum Resistive Load (GCFB)	R_L	50			KΩ	

Note: " * " typical figure are at V_{DD} = 5V and temperature = 25° C are design aids only, not guaranteed and not subject to production testing.

AC Electrical Characteristics

(AC electrical characteristics supersede the recommended operating conditions unless otherwise stated.)

Dual Tone Alert Signal Detection

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNITS	NOTES
Low Tone Frequency	F_L		2130		Hz	
High Tone Frequency	F_H		2750		Hz	
Frequency Deviation Acceptance		1.1			%	1
Frequency Deviation Rejection		3.5			%	2
Maximum Input Signal Level				0.22	dBm[a]	3
Input Sensitivity Per Tone		-43	-45		dBm	3, 4
Reject Signal Level Per Tone			-54		dBm	3, 4
Positive and Negative Twist[b] Accept		7			dB	
Noise Tolerance	SNR_{TONE}	20			dB	3, 4, 5

Notes:

a. dBm = decibels with a reference power of 1 mW into 600 ohms, 0 dBm = 0.7746 Vrms.

b. Twist = 20 log (F_H amplitude / F_L amplitude).

1: The range within which tones are accepted.

2: The range outside of which tones are rejected.

3: These characteristics are for V_{DD} = 5V and temperature = 25° C.

4: Both tones have the same amplitude. Both tones are at the nominal frequencies.

5: Band limited random noise 300–3400 Hz. Present only when the tone is present.

FSK Detection

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Input Frequency Detection					Hz	
Bell 202 Mark (logic 1)	FMARK	1188	1200	1212		+/-1%
Bell 202 Space (logic 0)	FSPACE	2178	2200	2222		+/-1%
CCITT V.23 Mark (logic 1)	FMARK	1280.5	1300	1319.5		+/-1.5%
CCITT V.23 Space (logic 0)	FSPACE	2068.5	2100	2131.5		+/-1.5%
Maximum Input Signal Level				-5.78	dBm	
Input Sensitivity		-43	-45		dBm	1, 2
Transmission Rate		1188	1200	1212	baud	
Input Noise Tolerance	SNRFSK	20			dB	1, 2, 3

Notes:
1: Both mark and space have the same amplitude and are at the nominal frequencies.
2: These characteristics are fort V_{DD} = 5V and temperature = 25° C.
3: Band limited random noise 300 - 3400 Hz. Present only when the FSK signal is present.

AC Timing Characteristics

(AC timing characteristics supersede the recommended operating conditions unless otherwise stated.)

System

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNITS	NOTES
Wake-up Time	t_{WAKE}	SLEEP			50	mS	
Sleep-down Time	t_{SLP}	OSCO			1	mS	

Note: " * " typical figures are for V_{DD} = 5V and temperature = 25° C are design aids only, not guaranteed and not subject to production testing.

Dual Tone Alert Signal Detection

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNITS	NOTES
Alert Detection Enable Time	tALTE	FSKE (low)			25	mS	
Alert Signal Present Detect Time	tDP	ALGR	0.5		10	mS	
Alert Signal Absent Detect Time	tDA		0.1		8	mS	

Note: " * " typical figure are at V_{DD} = 5V and temperature = 25° C are design aids only, not guaranteed and not subject to production testing.

FSK Detection

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNITS	NOTES
FSK Detection Enable Time	tFSKE	FSKE (high)			25	mS	
Input FSK to FCDN Low Delay	tCP				25	mS	

FSK Detection, continued

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNITS	NOTES
Input FSK to FCDN High Delay	tCA	FCDN	8			mS	
Hysteresis			8			mS	

Note: " * " typical figure are at V_{DD} = 5V and temperature = 25° C are design aids only, not guaranteed and not subject to production testing.

3-Wire Interface (Mode 0)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNITS	NOTES
Rise Time	tRR	FDRN			200	nS	4
Fall Time	tRF				200	nS	4
Low Time	tRL		415	416	417	µS	2
Rate		DATA	1188	1200	1212	bpS	1
Input FSK to Data Delay	tIDD			1	5	mS	
Rise Time	tR	DCLK DATA			200	nS	4
Fall Time	tF				200	nS	4
DATA to DCLK Delay	tDCD		6	416		µS	1, 2, 3
DCLK to DATA Delay	tCDD		6	416		µS	1, 2, 3
Frequency	fDCLK0	DCLK	1201.6	1202.8	1204	Hz	2
High Time	tCH		415	416	417	µS	2
Low Time	tCL		415	416	417	µS	2
DCLK to FDRN Delay	tCRD	DCLK, FDRN	415	416	417	µS	2

Notes:
" * " Ttypical figure are for V_{DD} = 5V and temperature = 25° C, are design aids only, not guaranteed and not subject to production testing.

1: FSK input data rate at 1200 +/-12 baud.
2: OSCI frequency at 3.579545 MHz +/-0.1%.
3: Function of signal condition.
4: 50 pF loading.

3-Wire Interface (Mode 1)

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.*	MAX.	UNITS	NOTES
Frequency	fDCLK1				1	MHz	
Duty Cycle		DCLK	30		70	%	
Rise Time	tR1				20	nS	
DCLK Low Set-up to FDRN	tDDS	DCLK,	500			nS	
DCLK Low Hold Time After FDRN	tDDH	FDRN	500			nS	

Note: " * " typical figure are at V_{DD} = 5V and temperature = 25° C are design aids only, not guaranteed and not subject to production testing.

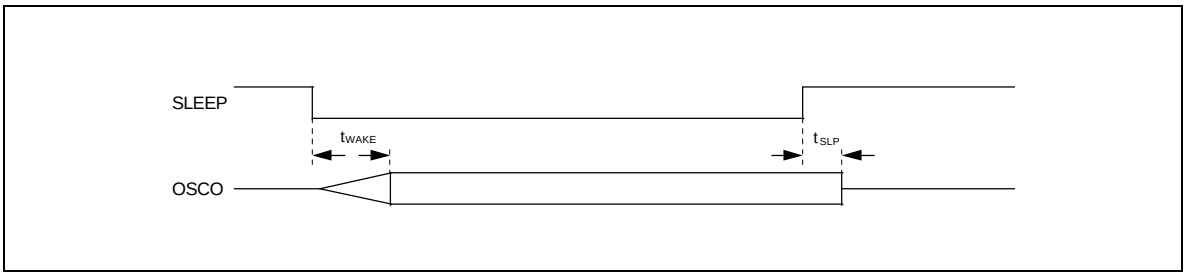


Figure 8-1. Wake up and Sleep Down Timing

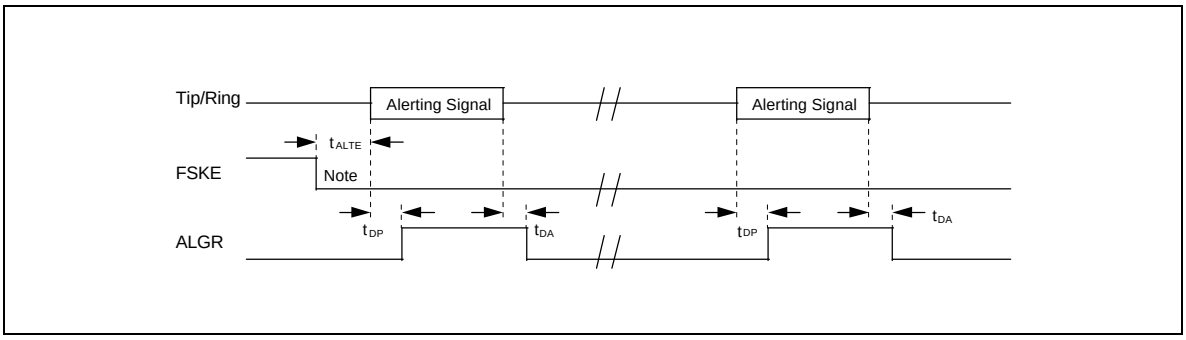


Figure 8-2. Alert Detection Enable and Alert Signal Present and Absent Detect Timing

Note: The minimal delay from FSKE low to ALGR high is $t_{ALTE} + t_{DP}$, if the alerting signal is present before t_{ALTE} has elapsed.

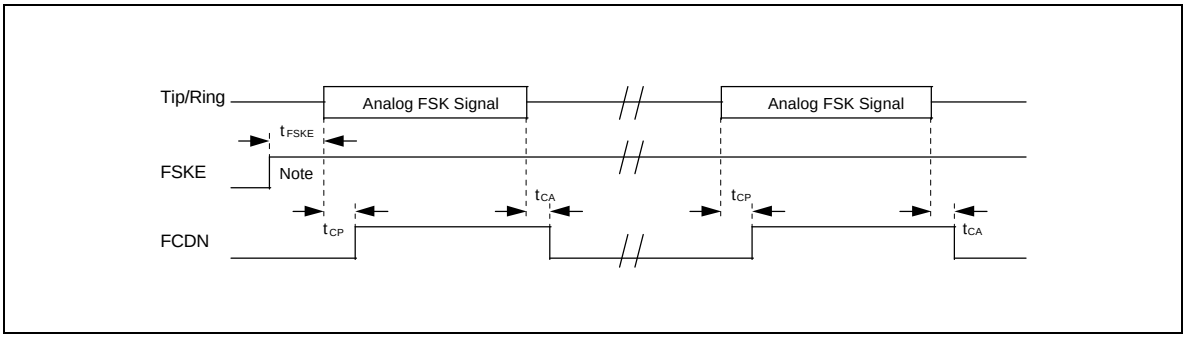


Figure 8-3. FSK Detection Enable and FSK Carrier Detect Present and Absent Timing

Note: The minimal delay from FSKE high to FCDN high is $t_{FSKE} + t_{CP}$, if the analog FSK signal is present before t_{FSKE} has elapsed.

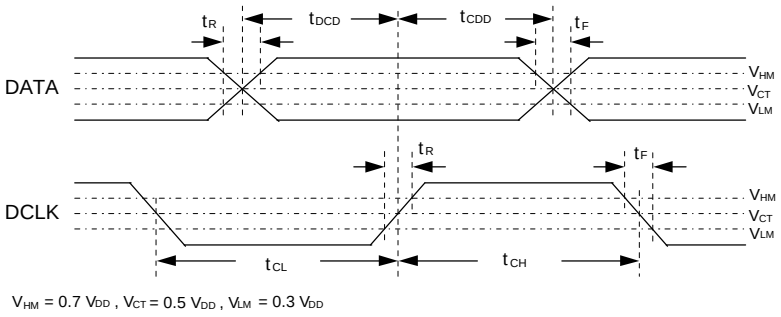


Figure 8-4. Data and DCLK Mode 0 Ouput Timing

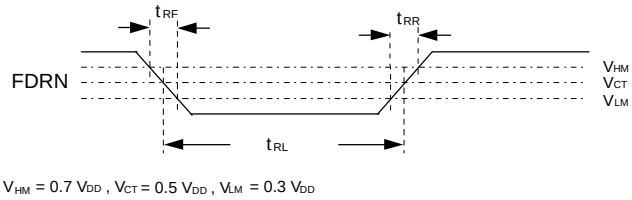


Figure 8-5. FDRN Output Timing

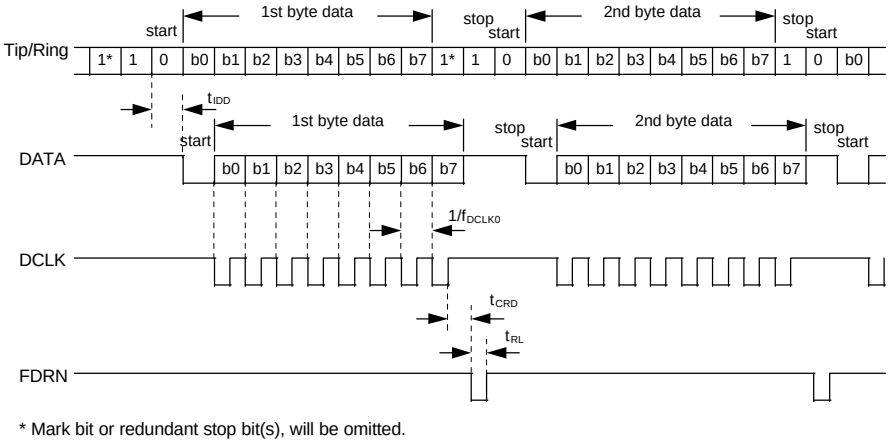


Figure 8-6. Serial Data Interface Timing of FSK Demodulation in Mode 0

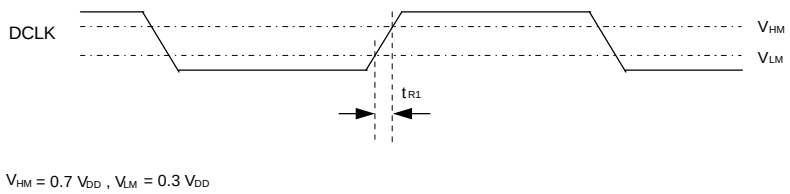
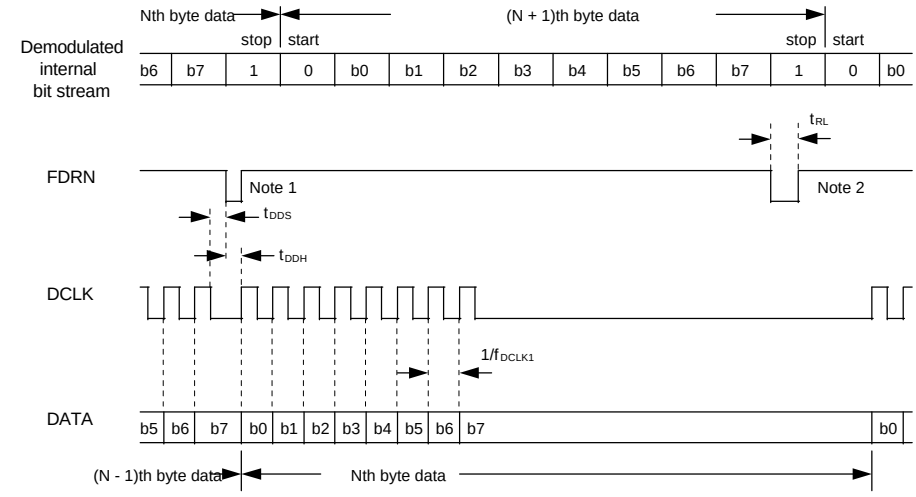


Figure 8-7. DCLK Mode 1 Input Timing



Notes:
1. FDRN cleared to high by DCLK.
2. FDRN not cleared, low for maximum time (1/2 bit width).

Figure 8-8. Serial Data Interface Timing of FSK Demodulation in Mode 1

APPLICATION INFORMATION

Application Circuit

The application circuit of the W91031 in Figure 9-1 shows the device being used within a typical CPE system. Note that only the circuit between the W91031 and the line interface is shown. The gain control op-amp is set to unity gain to allow the electrical characteristics to be met in this application circuit. It should also be noted that if a glitch with sufficient amplitude appears on the tip and ring interface, this will be detected as a ringing input by this circuit.

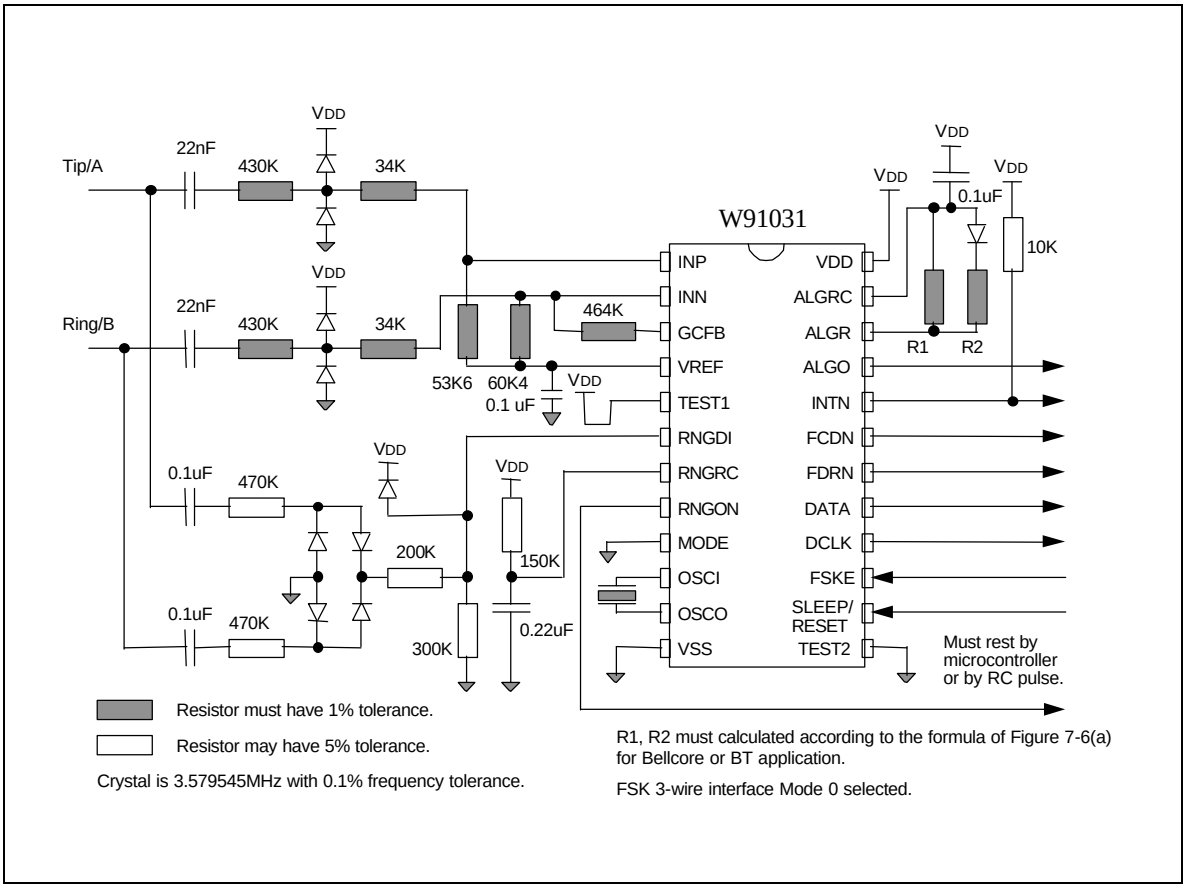


Figure 9-1. Application Circuit.

Another application circuit for the W91031, which provides common mode rejection of ringing circuit signals, is shown in Figure 9-2. When the AC voltage between the tip and ring is greater than the zener diode breakdown voltage, the photo-coupler LED will turn on, driving RNGDI high and thus detecting a ringing signal. Note however in this case, a glitch on the tip and ring interface is not able to turn on the photo-coupler and therefore will not be detected as a ringing signal.

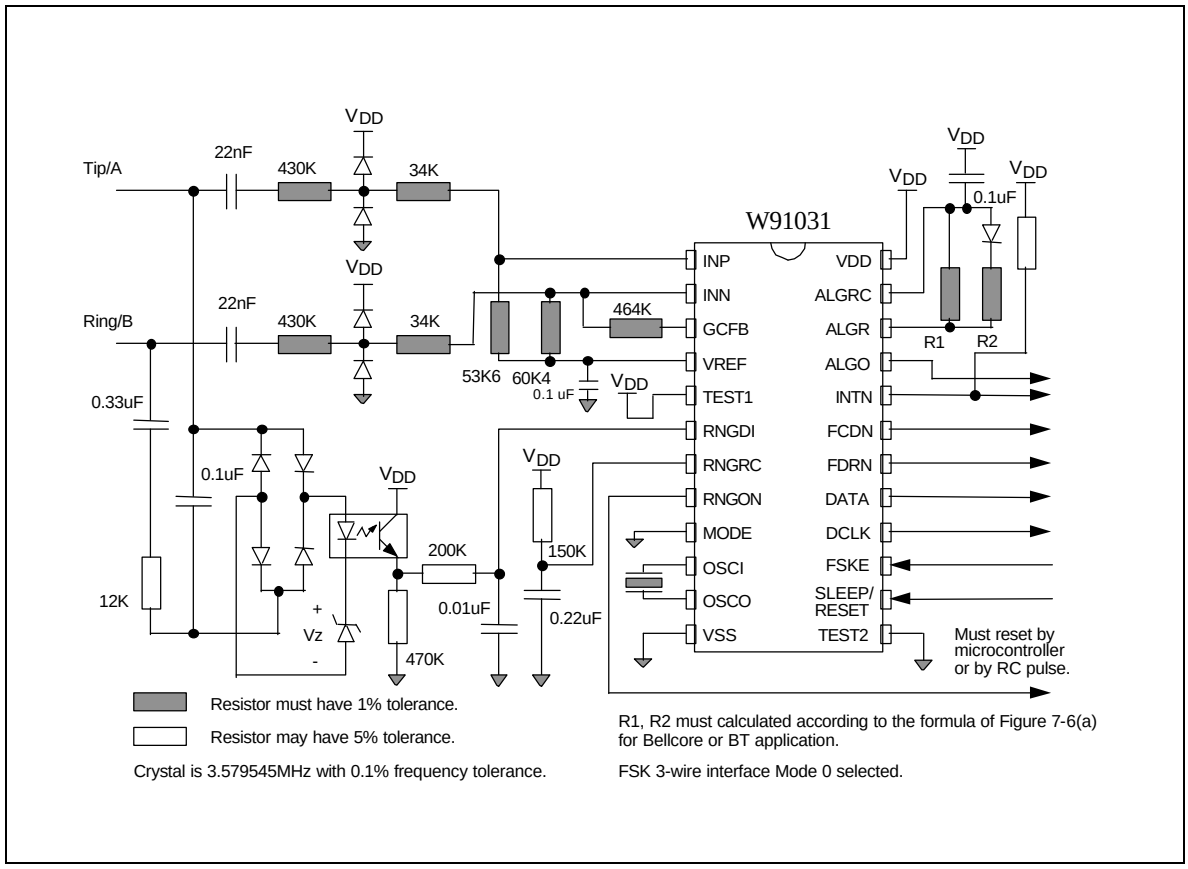


Figure 9-2. Application Circuit with Improved Common Mode Noise Immunity

Application Environment

There are three major timing differences for caller ID sequences, Bellcore, BT and CCA. Figure 9-3 is the timing diagram for the Bellcore on-hook data transmission and Figure 9-4 is the timing diagram for the Bellcore off-hook data transmission. Figure 9-5 is the timing diagram for the BT caller display service on-hook data transmission and Figure 9-6 is the timing diagram for the BT caller display service off-hook data transmission. Figure 9-7 is the timing diagram for the CCA caller display service for on-hook data transmission.

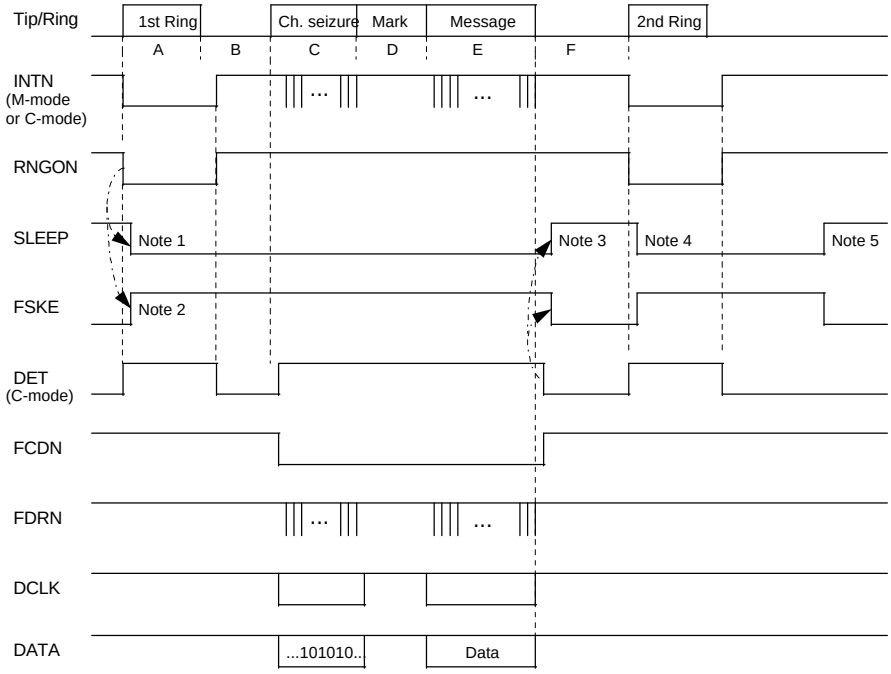


Figure 9-3. Input and Output Timing of Bellcore On-hook Data Transmission

A = 2 sec typical

B = 250–500 mS

C = 250 mS

D = 150 mS

E = Depends on data length

MAX C + D + E = 2.9 to 3.7 sec

F ≥ 200 mS

Notes :

1. The CPE designer may choose to wake up the W91031 only after the end of the RNGON signal to conserve power for a battery operated CPE. The delay from RNGON to SLEEP (and FSKE) is the reactive time of the microcontroller.
2. The CPE designer may choose to set FSKE to be always high while the CPE is on-hook, to ensure the FSK emodulator does not react to other in-band noise.
3. The microcontroller places the W91031 in a sleep condition after FCDN has become inactive.
4. The W91031 may not be woken up at this ring signal after the FSK data has been processed.
5. If the W91031 has been woken up at the 2nd ring, the microcontroller times out if FCDN is not activated and then puts the W91031 into a sleep condition.

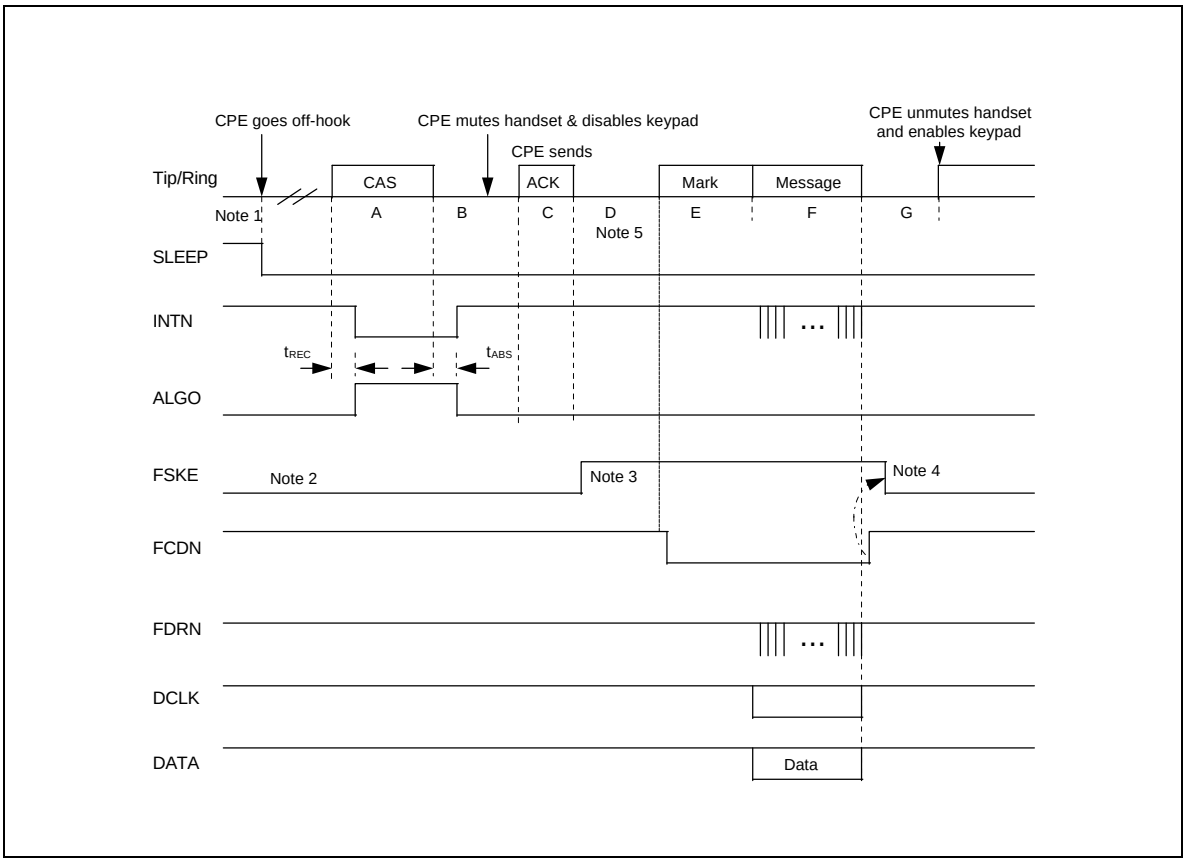


Figure 9-4. Input and Output Timing of Bellcore Off-hook Data Transmission

A = 75–85 mS	B = 0–100 mS
C = 55–65 mS	D = 0–500 mS
E = 58–75 mS	F = Depends on data length
G ≤ 50 mS	

Notes:

1. In a CPE where AC power is not available, the designer may choose to switch over to line power when the CPE goes off-hook and use battery power while on-hook.
2. The FSKE pin should be set low to enable the alert tone detector when the dual tone alert signal is expected. The CPE has the capability to disable the CAS detection by setting FSKE always high during the on-hook state.
3. FSKE may be set high as soon as the CPE has finished sending the acknowledge signal ACK.
4. FSKE should be set low when FCDN has become inactive.
5. For unsuccessful attempts where the end office does not send the FSK signal, the CPE should disable FSKE, unmute the handset and enable the keypad after this interval has elapsed.

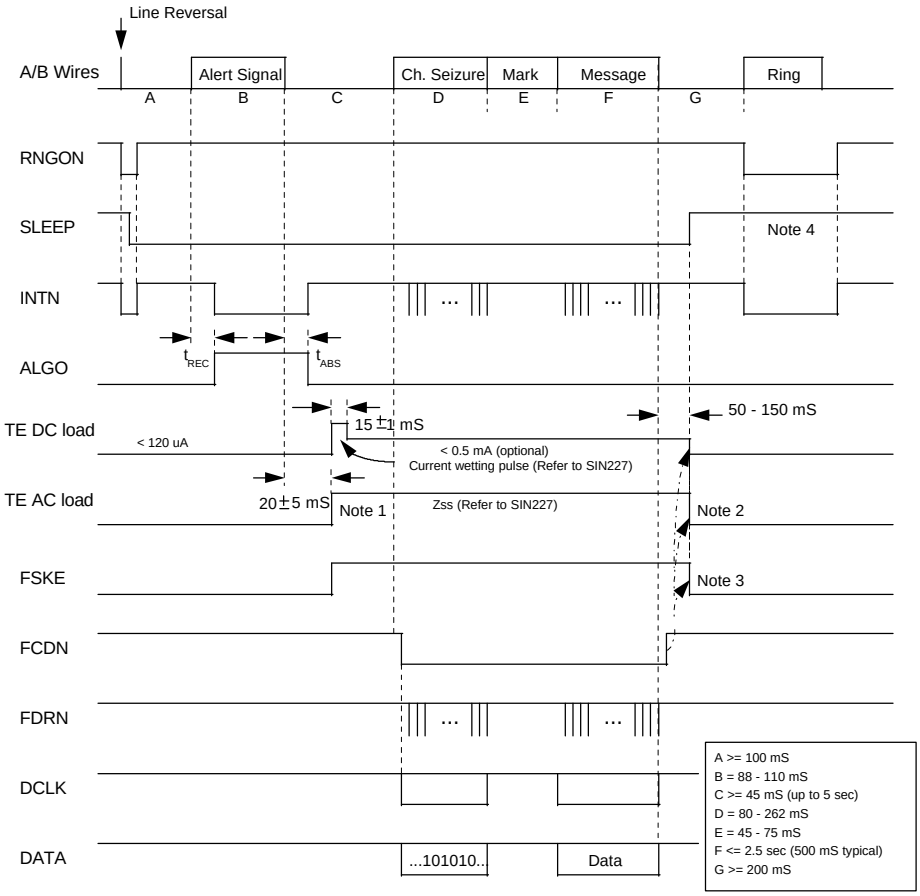


Figure 9-5. Input and Output Timing of BT Idle State (On-hook) Data Transmission

Notes:

1. SIN227 specifies that the AC and DC loads should be applied at 20 ±5 mS after the end of the dual tone alert signal.
2. SIN227 specifies that the AC and DC loads should be removed between 50–150 mS after the end of the FSK signal. The W91031 may also be placed in a sleep condition.
3. The FSKE pin should be set low to disable the FSK demodulator when FSK is not expected. The tone alerting signal speech and the DTMF tones are in the same frequency band as the FSK signal.
4. The W91031 may not be woken up at this ring signal after the FSK data has been processed.

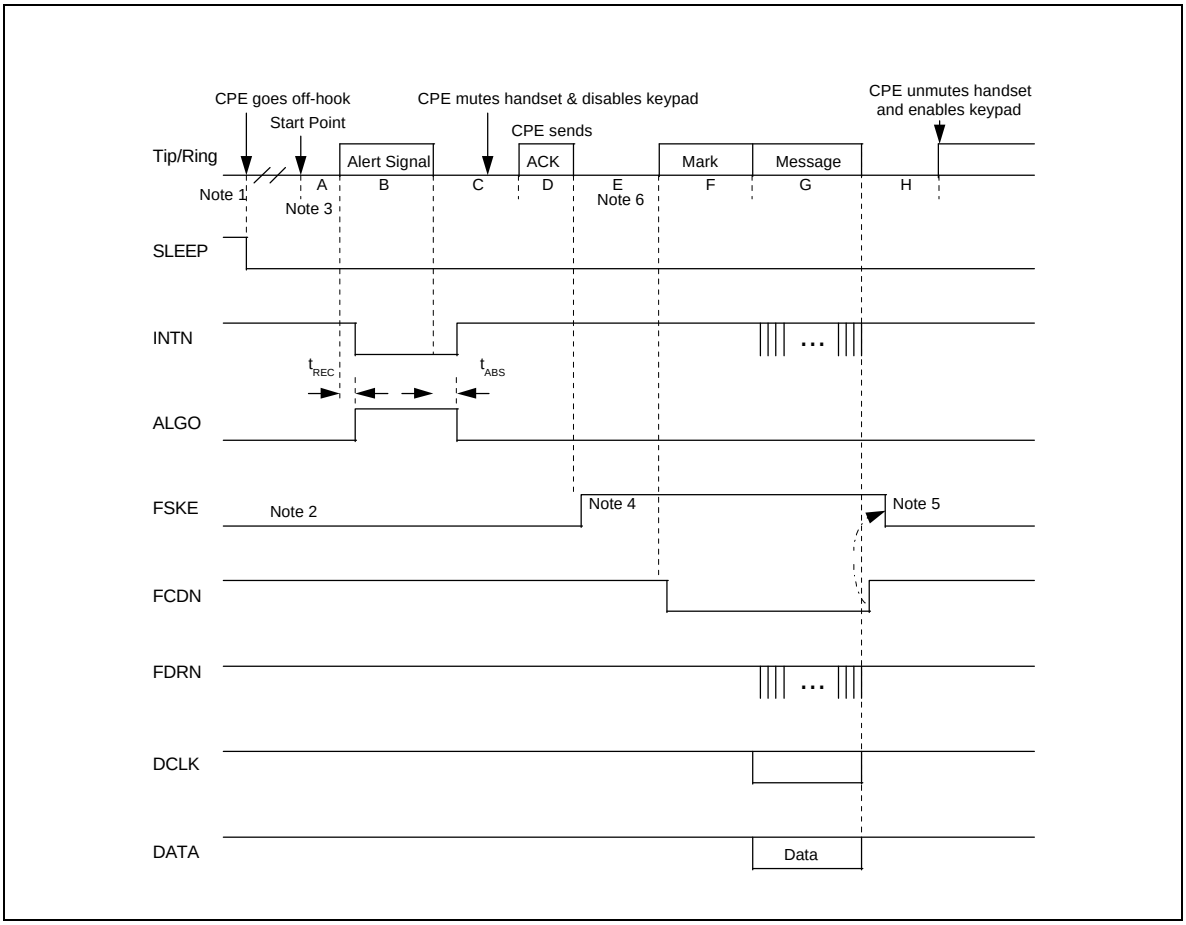


Figure 9-6. Input and Output Timing of BT Loop State (Off-hook) Data Transmission

A = 40–50 mS	B = 80–85 mS
C = ≤ 100 mS	D = 65–75 mS
E = 5–100 mS	F = 45–75 mS
G = Depends on data length	H ≤ 100 mS

Notes:

1. In a CPE where AC power is not available, the designer may choose to switch over to line power when the CPE goes off-hook and use battery power while on-hook.
2. The FSKE pin should be set low to enable the alert tone detector when the dual tone alert signal is expected.
3. The exchange will have already disabled the speech path to the distant customer in both transmission directions.
4. The FSKE may be set high as soon as the CPE has finished sending the acknowledge signal ACK.
5. FSKE should be set low when FCDN has become inactive.
6. In unsuccessful attempts where the exchange does not send the FSK signal, the CPE should disable FSKE, unmute the handset and enable the keypad after this interval.

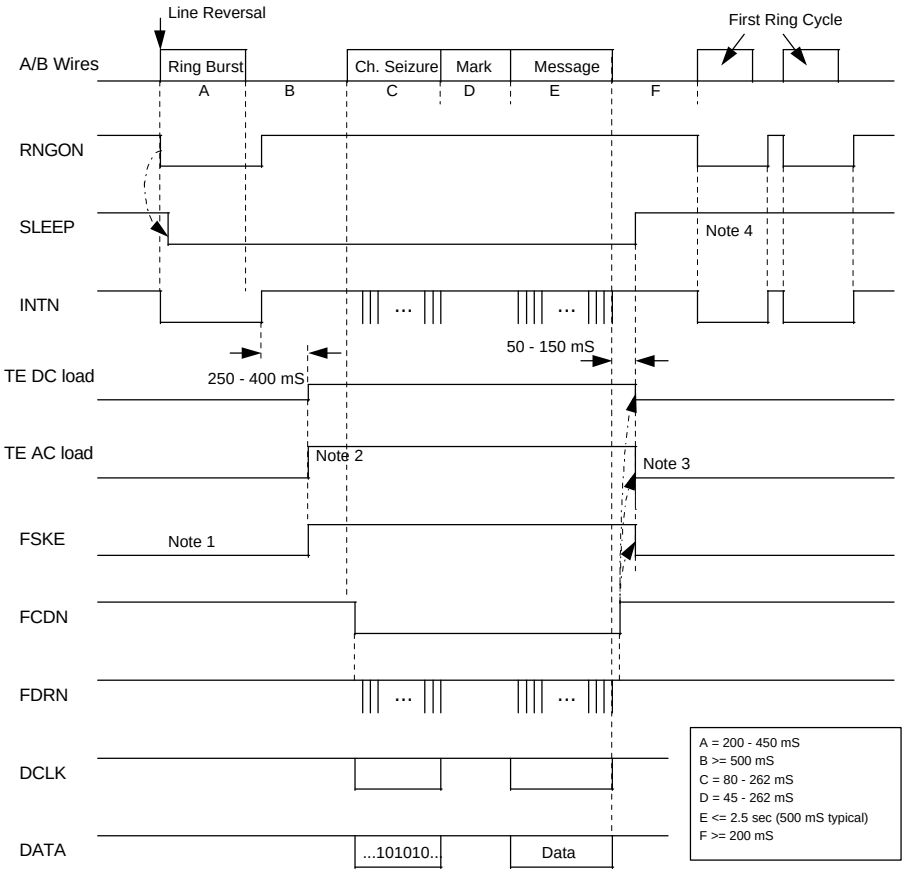


Figure 9-7. Input and Output Timing of CCA Caller Display Service Data Transmission

Notes:

1. The CPE designer may choose to set FSKE always high while the the CPE is on-hook and the FSK signal is expected.
2. TW/P & E/312 specifies that the AC and DC loads should be applied between 250–400 mS after the end of the ring burst.
3. TW/P & E/312 specifies that the AC and DC loads should be removed between 50–150 mS after the end of the FSK signal. The W91031 may also be placed in a sleep condition.
4. The W91031 may not be woken up at the first ring cycle after the FSK data had been processed.

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