

Preliminary W91510DN SERIES



TONE/PULSE DIALER WITH RTC AND LCD DISPLAY FUNCTIONS

GENERAL DESCRIPTION

The W91510DN series ICs are Si-gate CMOS IC that provide the signals needed for either pulse or tone dialing. They feature a 12/16-digit LCD driver for displaying telephone numbers and calling time. A real time clock is included to display the time of day. The W91510DN series is fabricated using CMOS technology and thus provide good performance in low voltage, low power applications.

FEATURES

- One by 32 digits for redial
- Uses 5 × 6 keyboard
- Pause, pulse-to-tone (*T) can be stored as a digit in memory
- Flash can be stored as a digit in memory when in store mode
- Minimum tone output duration: 87 mS
- Minimum intertone pause: 87 mS
- Tone/pulse mode pin selectable
- Make/break ratio pin selectable
- Dialing rate: 10 ppS
- Pause time: 3.6 Sec.
- Flash break time (73 mS, 100 mS, 300 mS or 600 mS) selectable by keypad
- Built-in 12 or 16-digit LCD driver (1/4 duty, 1/3 bias) selectable by mask option
- Built-in calling timer from [00:00] to [59:59]
- On-chip power-on reset and clear LCD
- Uses 3.579545 MHz TV quartz crystal or ceramic resonator
- Uses 32768 Hz crystal as RTC frequency base
- Packaged in 64-pin plastic QFP with RTC
- Switchable 24-hour clock or 12-hour clock with p.m. mode by keypad
- 0 or 9 dialing inhibition pin for PABX systems or long distance dialing lock out
- On hook debounce: 150 mS in normal mode and 20 mS in lock mode
- Off-hook delay 300 mS in lock mode ($\overline{DP}$ will keep low for 300 mS while off hook except the first off hook after power on reset that $\overline{DP}$ will keep high for 100 mS then go low for 200 mS)
- First key-in delay: 300 mS in lock mode
- Mixed dialing allowed

Preliminary W91510DN SERIES

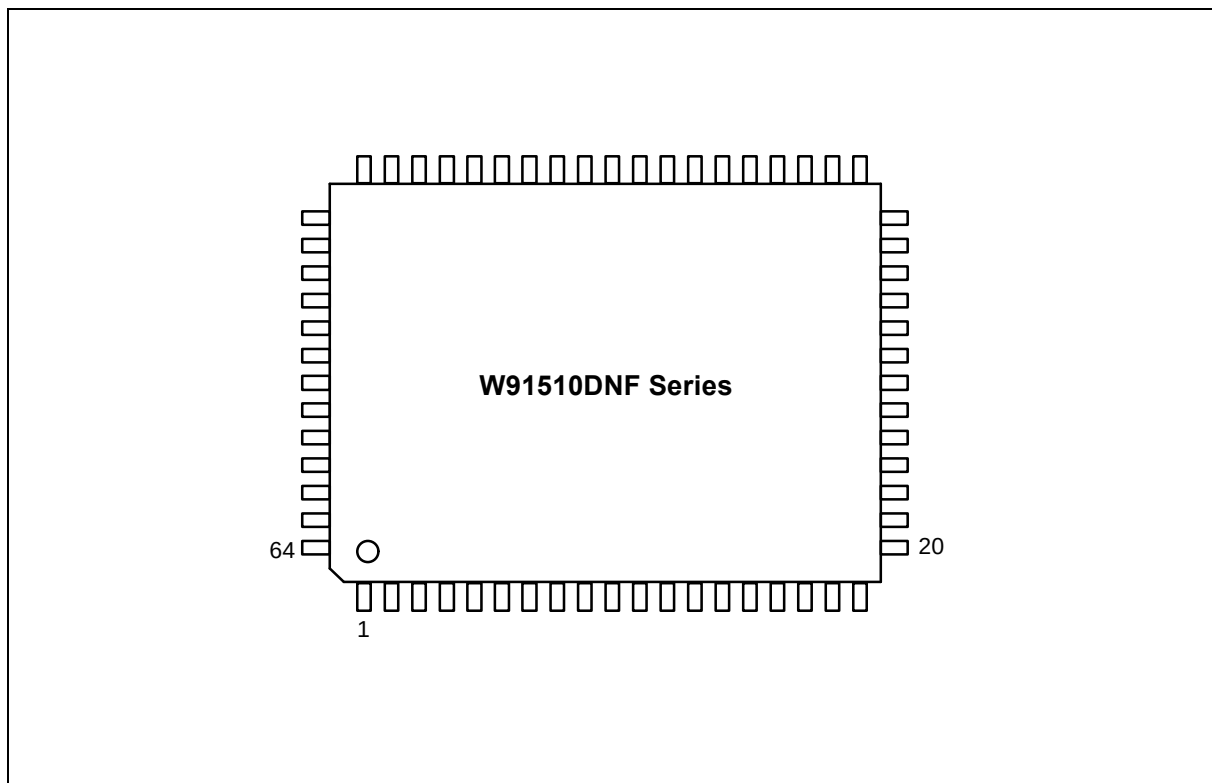


- The functions of the different dialers in the W91560DN series are shown in following table:

TYPE NO.	LCD DIGITS	LOCK	HOLD	PAUSE TIME
W91510DNF	16	–	Yes	3.6 Sec.
W91511DLNF	16	Yes	–	
W91512DNF	12	–	Yes	
W91513DLNF	12	Yes	–	
W91510DNH*	16	Yes	Yes	3.6 Sec.
W91512DNH*	12	Yes	Yes	

* Chip form package.

PIN CONFIGURATION



Preliminary W91510DN SERIES



PIN DESCRIPTION

SYMBOL	PIN NO.	I/O	FUNCTION								
Row, Column Inputs	18–21, 13–17	I	The keyboard inputs may be used with either the standard 5 × 6 keyboard, an inexpensive single contact (form A) keyboard or electronic input. A valid key entry is defined by a single row being connected to a single column.								
XT1, $\overline{\text{XT1}}$	22, 23	I, O	A built-in inverter provides oscillation with an inexpensive 3.579545 MHz crystal or ceramic resonator. The oscillator ceases when a keypad input is not sensed after chip enable and dialing finished. The crystal frequency deviation is ±0.02%.								
T/P $\overline{\text{MUTE}}$	8	O	The T/P $\overline{\text{MUTE}}$ is a conventional CMOS N-channel open drain output. The output transistor is switched on low level during dialing sequence (both pulse and tone mode), one-key redial break and flash break. Otherwise, it is switched off.								
H/P MUTE	9 (W91510DNF, W91512DNF, only)	O	The H/P MUTE is a conventional CMOS inverter output, During pulse dialing, one-key redial break, flash break and hold functions, this pin will output an active high. It remains in a low state at all other times.								
LOCK	9 (W91511DLNF, W91513DLNF only)	I	The LOCK pin is used to prevent "0" or "9" dialing under PABX system long distance call control. When the first key input after reset is "0" or "9", all the key inputs, including "0" or "9" key, become invalid, and the chip generates no output. The telephone is reinitialized by a reset. The following table describes the functions of the LOCK pin: <table><tr><th>LOCK PIN</th><th>FUNCTION</th></tr><tr><td>V_{DD}</td><td>"0", "9" dialing inhibited</td></tr><tr><td>Floating</td><td>Normal dialing</td></tr><tr><td>V_{SS}</td><td>"0" dialing inhibited</td></tr></table>	LOCK PIN	FUNCTION	V _{DD}	"0", "9" dialing inhibited	Floating	Normal dialing	V _{SS}	"0" dialing inhibited
LOCK PIN	FUNCTION										
V _{DD}	"0", "9" dialing inhibited										
Floating	Normal dialing										
V _{SS}	"0" dialing inhibited										
$\overline{\text{HKS}}$	24	I	Hook switch input. $\overline{\text{HKS}}$ = V _{DD} or floating: On-hook state. Chip in sleeping mode, no operation. $\overline{\text{HKS}}$ = V _{SS} : Off-hook state. Chip enable for normal operation. $\overline{\text{HKS}}$ pin is pulled to V _{DD} by internal resistor.								

Preliminary W91510DN SERIES



Pin Description, continued

SYMBOL	PIN NO.	I/O	FUNCTION																																								
$\overline{\text{HFI}}$, HFO	25, 10	I, O	Handfree control pins. A low pulse on the $\overline{\text{HFI}}$ input pin toggles the handfree control state. Status of the handfree control is listed in the following table: <table><tr><th colspan="2">CURRENT STATE</th><th colspan="3">NEXT STATE</th></tr><tr><th>Hook SW.</th><th>HFO</th><th>Input</th><th>HFO</th><th>Dialing</th></tr><tr><td>–</td><td>Low</td><td>$\overline{\text{HFI}}$ </td><td>High</td><td>Yes</td></tr><tr><td>On Hook</td><td>High</td><td>$\overline{\text{HFI}}$ </td><td>Low</td><td>No</td></tr><tr><td>Off Hook</td><td>High</td><td>$\overline{\text{HFI}}$ </td><td>Low</td><td>Yes</td></tr><tr><td>On Hook</td><td>–</td><td>Off Hook</td><td>Low</td><td>Yes</td></tr><tr><td>Off Hook</td><td>Low</td><td>On Hook</td><td>Low</td><td>No</td></tr><tr><td>Off Hook</td><td>High</td><td>On Hook</td><td>High</td><td>Yes</td></tr></table> $\overline{\text{HFI}}$ pin is pulled to V_{DD} by internal resistor. Detailed timing diagrams are shown in Figure 4(a), 4(b).	CURRENT STATE		NEXT STATE			Hook SW.	HFO	Input	HFO	Dialing	–	Low	$\overline{\text{HFI}}$ 	High	Yes	On Hook	High	$\overline{\text{HFI}}$ 	Low	No	Off Hook	High	$\overline{\text{HFI}}$ 	Low	Yes	On Hook	–	Off Hook	Low	Yes	Off Hook	Low	On Hook	Low	No	Off Hook	High	On Hook	High	Yes
CURRENT STATE		NEXT STATE																																									
Hook SW.	HFO	Input	HFO	Dialing																																							
–	Low	$\overline{\text{HFI}}$ 	High	Yes																																							
On Hook	High	$\overline{\text{HFI}}$ 	Low	No																																							
Off Hook	High	$\overline{\text{HFI}}$ 	Low	Yes																																							
On Hook	–	Off Hook	Low	Yes																																							
Off Hook	Low	On Hook	Low	No																																							
Off Hook	High	On Hook	High	Yes																																							
$\overline{\text{DP}}/\overline{\text{C6}}$	11	O	This pin is a CMOS N-channel open drain output. Flash key will cause $\overline{\text{DP}}$ to go active in either pulse mode or tone mode. In lock mode, the $\overline{\text{DP}}$ keeps low for 300 mS during off-hook delay time. The timing diagram is shown as Figure 1(a), 1(b), 1(c), 1(d).																																								
DTMF	6	O	In pulse mode, this pin remains in low state at all time. In tone mode, it will output a dual or single tone. Detailed timing diagram for tone mode is shown in Figure 2(a), 2(b), 2(c), 2(d). <table><tr><th colspan="4">OUTPUT FREQUENCY</th></tr><tr><th></th><th>Specified</th><th>Actual</th><th>Error %</th></tr><tr><td>R1</td><td>697</td><td>699</td><td>+0.28</td></tr><tr><td>R2</td><td>770</td><td>766</td><td>- 0.52</td></tr><tr><td>R3</td><td>852</td><td>848</td><td>- 0.47</td></tr><tr><td>R4</td><td>941</td><td>948</td><td>+0.74</td></tr><tr><td>C1</td><td>1209</td><td>1216</td><td>+0.57</td></tr><tr><td>C2</td><td>1336</td><td>1332</td><td>- 0.30</td></tr><tr><td>C3</td><td>1477</td><td>1472</td><td>- 0.34</td></tr></table>	OUTPUT FREQUENCY					Specified	Actual	Error %	R1	697	699	+0.28	R2	770	766	- 0.52	R3	852	848	- 0.47	R4	941	948	+0.74	C1	1209	1216	+0.57	C2	1336	1332	- 0.30	C3	1477	1472	- 0.34				
OUTPUT FREQUENCY																																											
	Specified	Actual	Error %																																								
R1	697	699	+0.28																																								
R2	770	766	- 0.52																																								
R3	852	848	- 0.47																																								
R4	941	948	+0.74																																								
C1	1209	1216	+0.57																																								
C2	1336	1332	- 0.30																																								
C3	1477	1472	- 0.34																																								
VLCD	29	O	Power supply pin for LCD driver. A 0.1 μF capacitor is connected between VLCD and V_{ss}.																																								
CP, CN	31, 32	I	CP is the voltage control capacitor positive pin. CN is the voltage control capacitor negative pin. A 0.1 μF capacitor is connected between these two pins.																																								

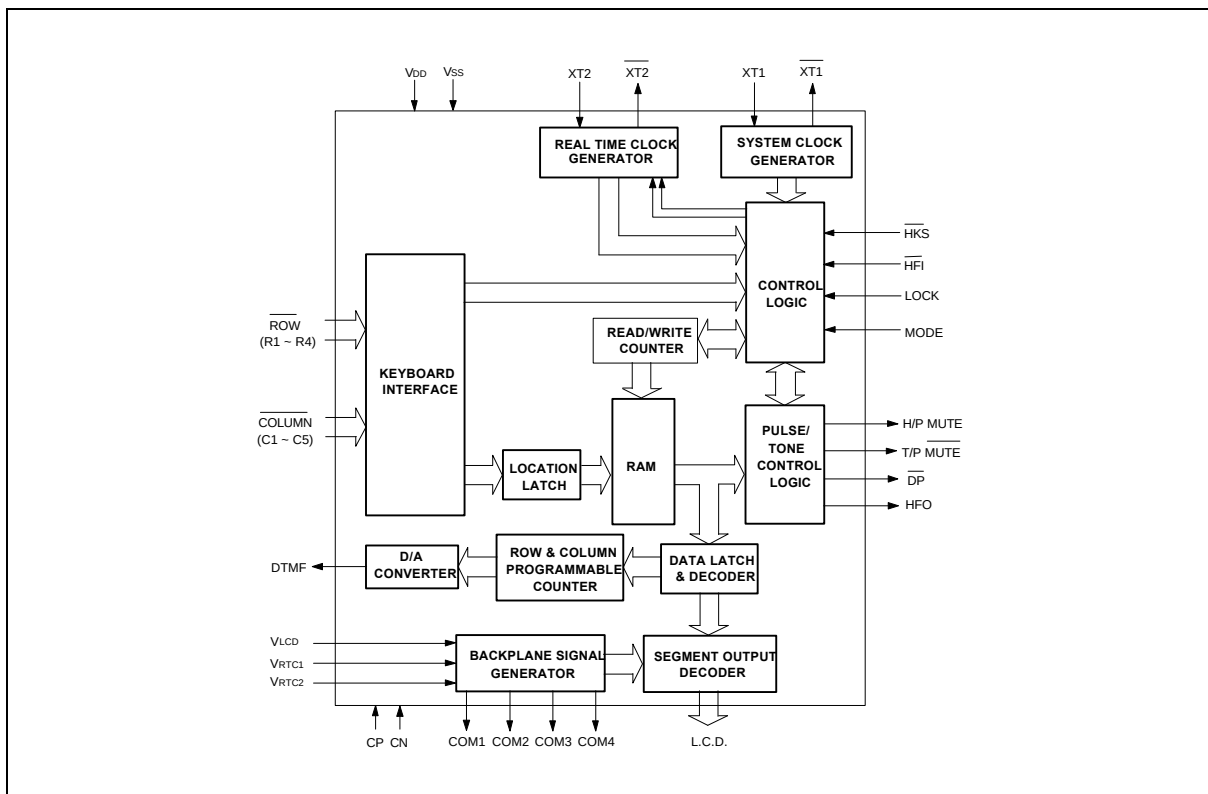
Preliminary W91510DN SERIES



Pin Description, continued

SYMBOL	PIN NO.	I/O	FUNCTION
COM1 to COM4	33–36	O	COM1 to COM4 are the common signal output terminal for the 1/4 duty LCD.
SEG1 to SEG32	37–64, 1–4	O	SEG1 to SEG32 are the 16-digit segment signal outputs.
XT2, $\overline{\text{XT2}}$	26, 27	I, O	A quartz crystal oscillator provides an RTC frequency time base of 32.768 KHz.
VRTC1, VRTC2	28, 30	I	Either VRTC1 should be connected to a 1.5V battery, and VRTC2 should be connected a capacitor 0.1 μF to ground.
VDD, VSS	5, 7	I	Power input pins.
MODE	12	I	Pulling mode pin to VSS places the dialer in tone mode. Pulling mode pin to VDD places the dialer in pulse mode (10 ppS, M/B = 1/2). Leaving mode pin floating places the dialer in pulse mode (10 ppS, M/B = 2/3).

BLOCK DIAGRAM



Publication Release Date: May 1997

Revision A2

Preliminary W91510DN SERIES



FUNCTIONAL DESCRIPTION

Keyboard Operation

C1	C2	C3	C4	C5	$\overline{DP} / \overline{C6}$	
1	2	3			HOLD1	R1
4	5	6	F4		HOLD2	R2
7	8	9	CHK		APSET	R3
* / T	0	#	R / P	RTC / HOUR	SET	R4
F1	F2	F3	OKR	TIM / MIN		Vx

- * / T: * in tone mode and P → T in pulse mode
- F1, F2, F3, F4: Flash keys
- R / P: Redial and pause function key
- OKR: One-key redial function
- RTC: Real time clock toggle key
- TIM: a. Display last calling time
b. Start and/or stop counting up calling time
- HOUR and MIN: Adjusting time setting keys
- HOLD1, HOLD2: Hold function keys
- APSET: Toggle to set RTC display mode
- SET: Toggle the RTC set function on/off.
- CHK: a. Check dialing number
b. Check dialing time

Note: D1, ..., Dn, D1', ..., Dn': 0, ..., 9, * / T, #

Normal Dialing

OFF HOOK (or ON HOOK & $\overline{HFI} \overline{IO}$), D1, D2, ..., Dn

1. D1, D2, ..., Dn will be dialed out.
2. Dialing length is unlimited, but redial is inhibited if length oversteps 32 digits in normal dialing.

Redialing

1. OFF HOOK (or ON HOOK & $\overline{HFI} \overline{IO}$), D1, D2, Check Memory (or Number Store), D3, ..., Dn, Busy, Come ON HOOK, OFF HOOK (or ON HOOK & $\overline{HFI} \overline{IO}$), R / P

Preliminary W91510DN SERIES



- a. The **R/P** key can execute the redial function only as the first key-in after off-hook; otherwise, it will invoke pause function.
- b. The redial memory content will be D3, ..., Dn.
- c. Redial memory can be checked in memory check mode. (**CHK** , **R/P**)
- d. If redialing length oversteps 32 digits, the redialing function will be inhibited.
2. **OFF HOOK** (or **ON HOOK** & **HFI I₀**), **D1** , **D2** , ..., **Dn** , Busy, **OKR**
 - a. If the dialing of **D1** to **Dn** is finished, pressing the **OKR** key will cause the pulse output pin to go low for 2.2 seconds break time and 0.6 seconds pause time will automatically be added.
 - b. If the pulses of the dialed digits **D1** to **Dn** have not finished, **OKR** will be ignored.
 - c. The one-key redialing function timing diagram is shown in Figure 3.

Access Pause

OFF HOOK (or **ON HOOK** & **HFI I₀**), **D1** , **D2** , **R/P** , **D3** , ..., **Dn**
 , Busy, Come **ON HOOK** , **OFF HOOK** (or **ON HOOK** & **HFI I₀**), **R/P**

1. The first R/P functions as a pause key and the second as a first key-in redial key.
2. The pause function can be stored in memory.
3. The pause function is executed in normal dialing, redialing, or memory dialing.
4. The pause duration time is 3.6 Sec.
5. The pause function timing diagram is shown in Figure 5

Pulse- to-tone (*T)

OFF HOOK (or **ON HOOK** & **HFI I₀**), **D1** , **D2** , ..., **Dn** , ***T** , **D1'**
 , **D2'** , ..., **Dn'**

1. If the mode switch is set to pulse mode, then the output signal will be:
D1, D2, ..., Dn, Pause (3.6 sec), D1', D2', ..., Dn'
(Pulse) (Tone)
2. If the mode switch is set to tone mode, then the output signal will be:
D1, D2, ..., Dn, *, D1', D2', ..., Dn'
(Tone) (Tone)
3. The dialer remains in tone mode after the digits have been dialed out and can be reset to pulse mode only by going on-hook.
4. The pulse-to-tone function timing diagram is shown in Figure 6(a), 6(b).

Preliminary W91510DN SERIES



Flash (F = F1, F2, F3, F4)

(or &) ,

1. The dialer will execute flash break time of 600 mS(F1), 300 mS(F2), 73 mS(F3) or 100 mS(F4) and pause time of 1S before the next digit (except flash key) is dialed out.
2. The system will return to the initial state after flash break time is finished.
3. Keyboard functions are inhibited during flash break is being executed.
4. The flash timing daigram is shown in Figure 7.

Hold Key

(or &) , (or)

1. The hold function is toggled on and off by HOLD1 or HOLD2 key. When the hold function is toggled on, the hold mark (dot of digit_4) will be lit and all key-in (except hold keys and icon keys) will be ignored.

2. The following are examples of hold function toggled on and off:

a. , (or) , (or)

b. , (or) ,

c. , (or) , ,

d. & , (or) ,

3. HOLD1 and HOLD2 have the same function in off-hook state. The difference between HOLD1 and HOLD2 are shown as follows:

a. If , (or) , , is entered, then the dialer will be off-line.

If , (or) , , is entered, then the dialer will stay at hold function.

b. If & , (or) , is entered, then the dialer will be off- line.

c. If & , (or) , and is entered, then the dialer will stay at hold function.

4. The function timing diagram is shown in Figure 8(a), 8(b), 8(c).

Adjusting Time Setting

(or &) , , , ,

(or)

Preliminary W91510DN SERIES



1. Only HOUR and MIN keys are valid in RTC set mode.
2. Hours and minutes count forward as long as HOUR or MIN key is pressed.
3. The on/off function of SET is toggled, and the dialer will be initialized after toggle SET key.
4. If the dialing sequence D1, D2, ..., Dn (including flash and pause) has not finished, SET will be ignored.

RTC Display Mode

(or &),

1. The real time clock display mode can be toggled on and off by RTC key.
2. The icon display will not be changed when enter RTC display mode and set RTC mode.

APSET

1. In the off-hook state, pressing APSET key to toggle the RTC function in 24-hour clock mode or 12-hour clock with p.m. mode.
2. The default mode is 12-hour clock with p.m. mode after power on.

Check Key

(or &), ,

The redial content will be displayed on the LCD when either or is key in.

TIM

(or &), , , ..., (or or),

1. If no key is pressed after dialing finish, the LCD will display counting time after 6 seconds.
2. If the dialing sequence D1, D2, ..., Dn has not finished, TIM will be ignored.
3. The timer will be initialized by flash and toggle SET key.

Preliminary W91510DN SERIES



ABSOLUTION MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD} -V _{SS}	-0.3 to +7.0	V
Input/Output Voltage	V _{IL}	V _{SS} -0.3	V
	V _{IH}	V _{DD} +0.3	
	V _{OL}	V _{SS} -0.3	
	V _{OH}	V _{DD} +0.3	
Power Dissipation	P _D	120	mW
Operating Temperature	T _{OPR}	-0.5 to +70	°C
Storage Temperature	T _{STG}	-55 to +125	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(V_{DD}-V_{SS} = 2.5V. F_{OSC} = 3.58 MHz, T_A = 25° C, all outputs unloaded.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{DD}	-	2.0	-	5.5	V
Operating Current	I _{OP}	Tone, Unloaded	-	0.5	0.7	mA
		Pulse, Unloaded	-	0.4	0.5	
Standby Current	I _{SB}	HKS = 0, Unloaded and no key entry	-	-	15	μA
Memory Retention Current	I _{MR}	HKS = 1 V _{DD} = 1.0V	-	-	0.5	μA
Tone Output Voltage	V _{TO}	Row group RL = 10 KΩ	130	150	170	mVrms
Pre-emphasis		Col/Row V _{DD} = 2.0 to 5.5V	-	2	3	dB
DTMF Distortion	THD	RL = 10 KΩ V _{DD} = 2.0 to 5.5V	-	-30	-23	dB
DTMF Output DC Level	V _{TDC}	V _{DD} = 2.0 to 5.5V	1.0	-	3.0	V
DTMF Output Sink Current	I _{TL}	V _{TO} = 0.5V	0.2	-	-	mA
DP Output Sink Current	I _{PL}	V _{PO} = 0.5V	0.5	-	-	mA

Preliminary W91510DN SERIES



DC characteristics, continued

PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Common Output Voltage	V _{CH}	-	4.2	4.5	4.8	V
	V _{CL}	-	-	0	0.3	
Common Output Current	I _{CH}	-	-20	-	-	μA
	I _{CL}	-	20	-	-	
Segment Output Voltage	V _{SH}	-	4.2	4.5	4.8	V
	V _{SL}	-	-	0	0.3	
Segment Output Current	I _{SH}	-	-5	-	-	μA
	I _{SL}	-	5	-	-	
RMS Voltage Across a Segment	V _{ON}	-	2.4	2.6	-	V _{rms}
	V _{OFF}	-	-	1.5	1.7	
Average DC Offset Voltage	V _{DC}	-	-	-	100	mV
HFI High Voltage	V _{HFIH}	-	0.8 V _{DD}	-	V _{DD}	V
HFI Low Voltage	V _{HFIL}	-	-	-	0.2 V _{DD}	V
T/P MUTE Output Sink Current	I _{TML}	V _{TMO} = 0.5V	0.5	-	-	mA
H/P MUTE Output Drive Current	I _{HMH}	V _{HMO} = 2.0V	0.5	-	-	mA
H/P MUTE Output Sink Current	I _{HML}	V _{HMO} = 0.5V	0.5	-	-	mA
Keypad Input Drive Current	I _{KD}	V _I = 0V	4	-	-	μA
Keypad Input Sink Current	I _{KS}	V _I = 2.5V	200	-	-	μA
Keypad Resistance	R _K	-	-	-	5	KΩ
Control Input Pull-up/Down Resistor	R _{IH}	-	100	-	-	KΩ
HKS Input Pull-high Resistor	R _{HK}	-	-	500	-	KΩ

Preliminary W91510DN SERIES



AC CHARACTERISTICS

(V_{DD}-V_{SS} = 2.5V, F_{osc.} = 3.58 MHz, T_A = 25°C, all outputs unloaded.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Key-in Debounce	TKID	-	-	20	-	mS
Key Release Debounce	TKRD	-	-	20	-	mS
Off-hook Delay Time	TOFD	-	-	300	-	mS
First Key-in Delay Time	TFKD	-	-	300	-	mS
On-hook Debounce Time	TOHD	Unlock	-	150	-	mS
		Lock	-	20	-	
Pulse Mute Delay	TMD	Mode = V _{DD}	-	40	-	mS
		Mode = Floating	-	33.3	-	
Pre-digit-Pause 10 ppS	TPDP	Mode = V _{DD}	-	40	-	mS
		Mode = Floating	-	33.3	-	
Inter-digit Pause (Auto Dialing)	TIDP	10 ppS	-	800	-	mS
Make/Break Ratio	M:B	Mode = V _{DD}	-	40:60	-	%
		Mode = Floating	-	33:67	-	
Tone Output Duration	TTD	-	-	87	-	mS
Inter-tone Pause	TITP	-	-	87	-	mS
Flash Break Time	TFB	F1	-	600	-	mS
		F2	-	300	-	
		F3	-	73	-	
		F4	-	100	-	
Flash Pause Time	TFP	F1, F2, F3,F4	-	1	-	S
Pause Time	TP	R/P	-	3.6	-	
One Key Redialing Break Time	TRB	-	-	2.2	-	S
One Key Redialing Pause Time	TRP	-	-	0.6	-	S
LCD Frame Frequency	FLCD	-	-	32	-	Hz

Preliminary W91510DN SERIES



RTC DC CHARACTERISTICS

(V_{RTC} = 1.5V, V_{SS} = 0V, F_{OSC} = 32.768 KHz, T_A = 25° C, all outputs unloaded.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V _{RTC}	-	1.2	1.5	1.8	V
Supply Current	I _{RTC}	No Load	-	2.0	4.0	μA
OSC. Starting Time	T _{OSC}	-	-	-	3	S
OSC. Output Built-in Cap.	C _O	C _I = 12.5 pF	-	25	-	pF
OSC. in Trimmer Cap.	C _{TRIM}	-	5	-	35	pF
Frequency Stability	Δf/f	V _{DD} -V _{SS} = 1.3 to 1.6V	-	-	1	ppM

Notes :

1. Crystal parameters suggested for proper operation are R_s < 100 ohms, L_m = 96 mH, C_m = 0.02 pF, C_n = 5 pF, C_I = 18 pF, and F_{osc} = 3.579545 MHz ±0.02%
2. Crystal oscillator accuracy directly affects these times.

TIMING WAVEFORMS

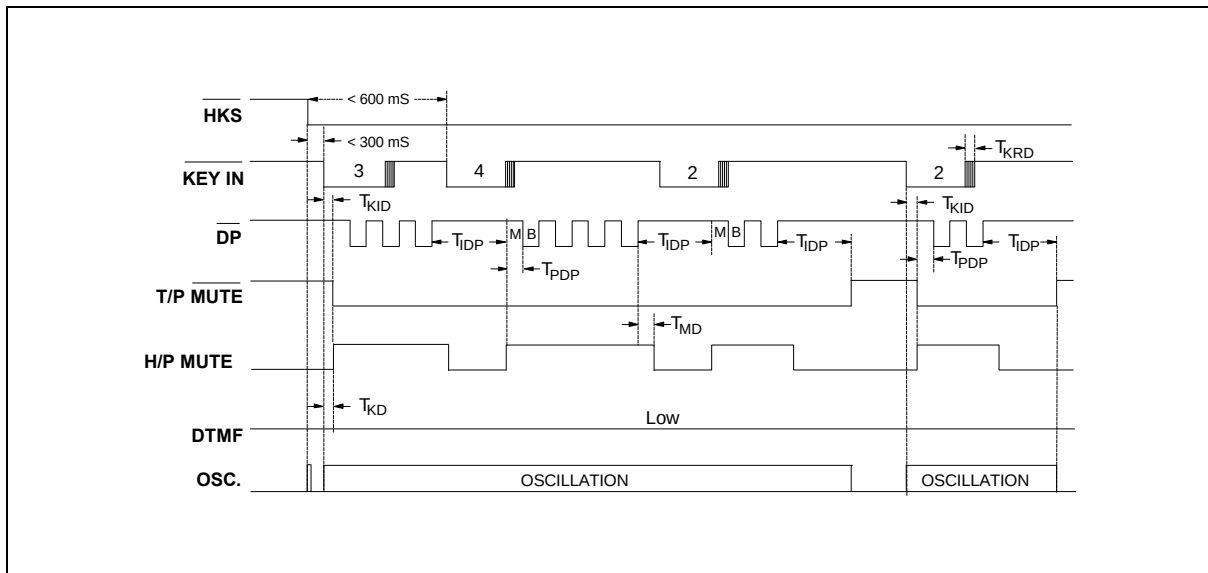


Figure 1(a). Normal Dialing Timing Diagram (Pulse Mode without Lock Function)

Preliminary W91510DN SERIES



Timing Waveforms, continued

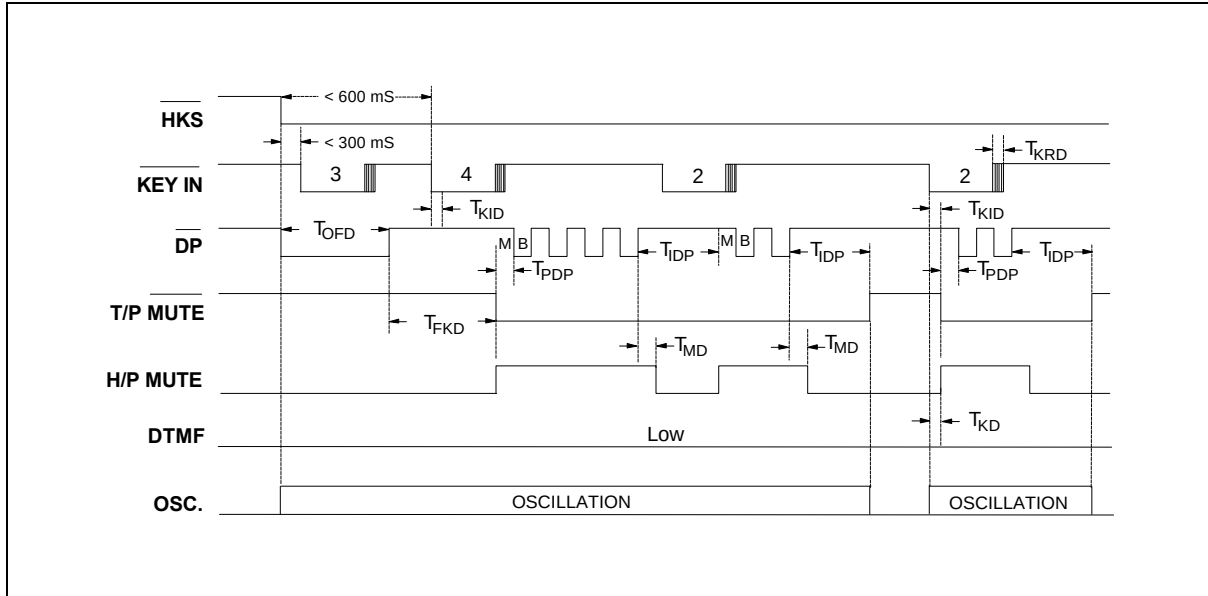


Figure 1(b). Normal Dialing Timing Diagram (Pulse Mode with Lock Function)

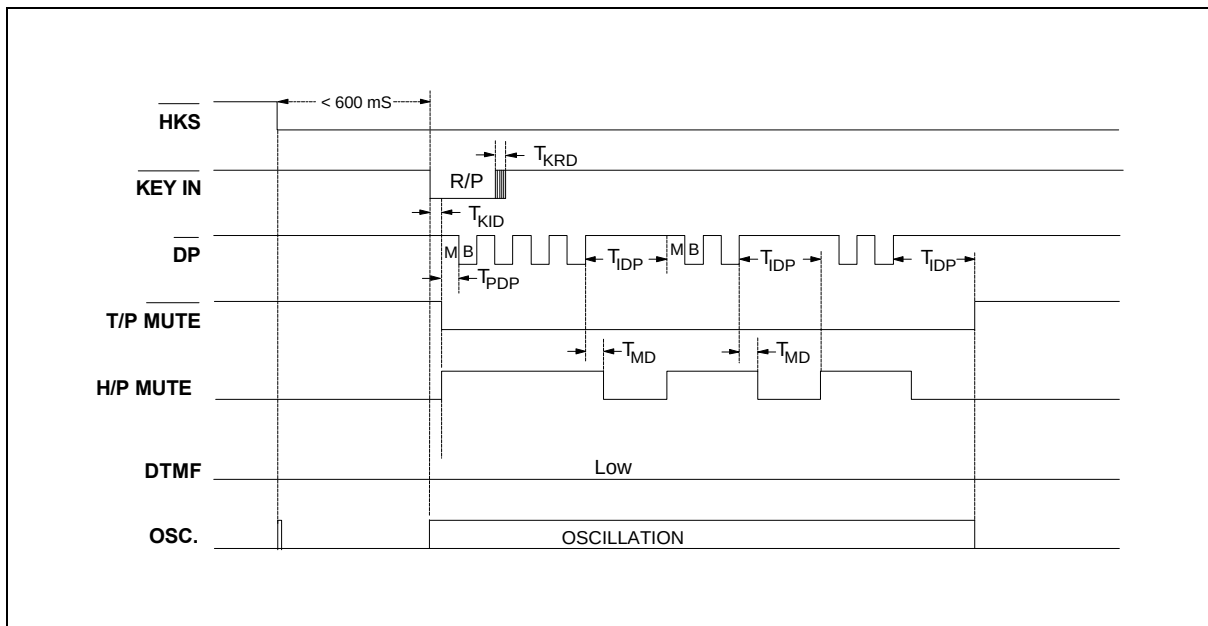


Figure 1(c). Auto Dialing Timing Diagram (Pulse Mode Without Lock Function)

Preliminary W91510DN SERIES



Timing Waveforms, continued

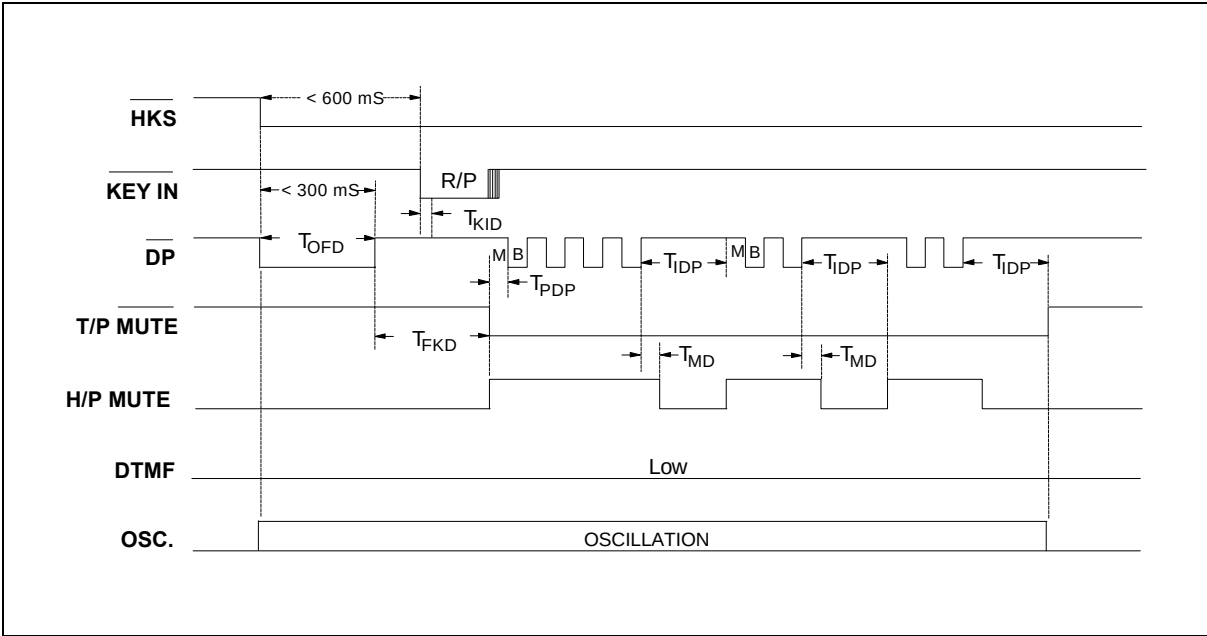


Figure 1(d). Auto Dialing Timing Diagram (Pulse Mode with Lock Function)

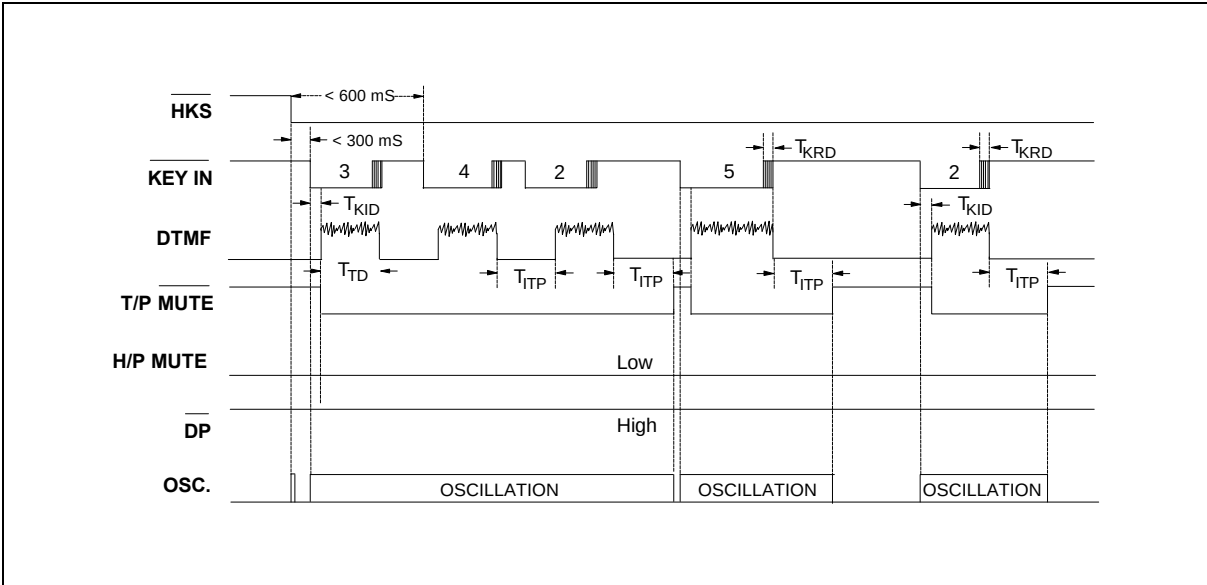


Figure 2(a). Normal Dialing Timing Diagram (Tone Mode Without Lock Function)

The timing diagram illustrates the sequence of events for the HKS system. The signals and their timing characteristics are as follows:

- HKS:** A high-level signal that remains active for a duration of $< 600 \text{ mS}$.
- KEY IN:** A signal that transitions from low to high, with a pulse width of $< 300 \text{ mS}$. It shows a sequence of pulses labeled 3, 4, 2, 5, and 2. The time between the first and second pulse is T_{KD} . The time between the last pulse and the next high-level signal is T_{KRD} .
- DTMF:** A signal that transitions from low to high, with a pulse width of T_{TD} . It shows a sequence of pulses labeled 3, 4, 2, 5, and 2. The time between the first and second pulse is T_{ITP} . The time between the last pulse and the next high-level signal is T_{ITP} .
- T/P MUTE:** A signal that transitions from low to high, with a pulse width of T_{ITP} . It shows a sequence of pulses labeled 3, 4, 2, 5, and 2. The time between the first and second pulse is T_{ITP} . The time between the last pulse and the next high-level signal is T_{ITP} .
- H/P MUTE:** A signal that transitions from low to high, with a pulse width of T_{FKD} . It shows a sequence of pulses labeled 3, 4, 2, 5, and 2. The time between the first and second pulse is T_{FKD} . The time between the last pulse and the next high-level signal is T_{FKD} .
- DP:** A signal that transitions from low to high, with a pulse width of T_{OFD} . It shows a sequence of pulses labeled 3, 4, 2, 5, and 2. The time between the first and second pulse is T_{OFD} . The time between the last pulse and the next high-level signal is T_{OFD} .
- OSC.:** A signal that transitions from low to high, with a pulse width of T_{OFD} . It shows a sequence of pulses labeled 3, 4, 2, 5, and 2. The time between the first and second pulse is T_{OFD} . The time between the last pulse and the next high-level signal is T_{OFD} .

The timing diagram illustrates the sequence of events for the HPS-1000. The signals and their timing are as follows:

- HKS**: A signal that transitions from low to high at the start of the sequence and returns to low at the end.
- KEY IN**: A signal that transitions from low to high, followed by a pulse labeled **R/P** (Reset/Pulse) with a duration of T_{KRD} .
- DTMF**: A signal that transitions from low to high, followed by a series of pulses labeled T_{KID} (Key Inter-Digit Delay) and T_{ITP} (Inter-Tone Pulse).
- T/P MUTE**: A signal that transitions from low to high, followed by a series of pulses labeled T_{TD} (Tone Delay) and T_{ITP} (Inter-Tone Pulse).
- H/P MUTE**: A signal that transitions from low to high, followed by a series of pulses labeled T_{ITP} (Inter-Tone Pulse).
- DP**: A signal that transitions from low to high, followed by a series of pulses labeled T_{ITP} (Inter-Tone Pulse).
- OSC.**: A signal that transitions from low to high, followed by a series of pulses labeled T_{ITP} (Inter-Tone Pulse).

The diagram also includes a time interval of $< 600 \text{ mS}$ for the initial setup and a time interval of T_{OHD} (Off-Hook Delay) for the final state.

- 16 -

Preliminary W91510DN SERIES



Timing Waveforms, continued

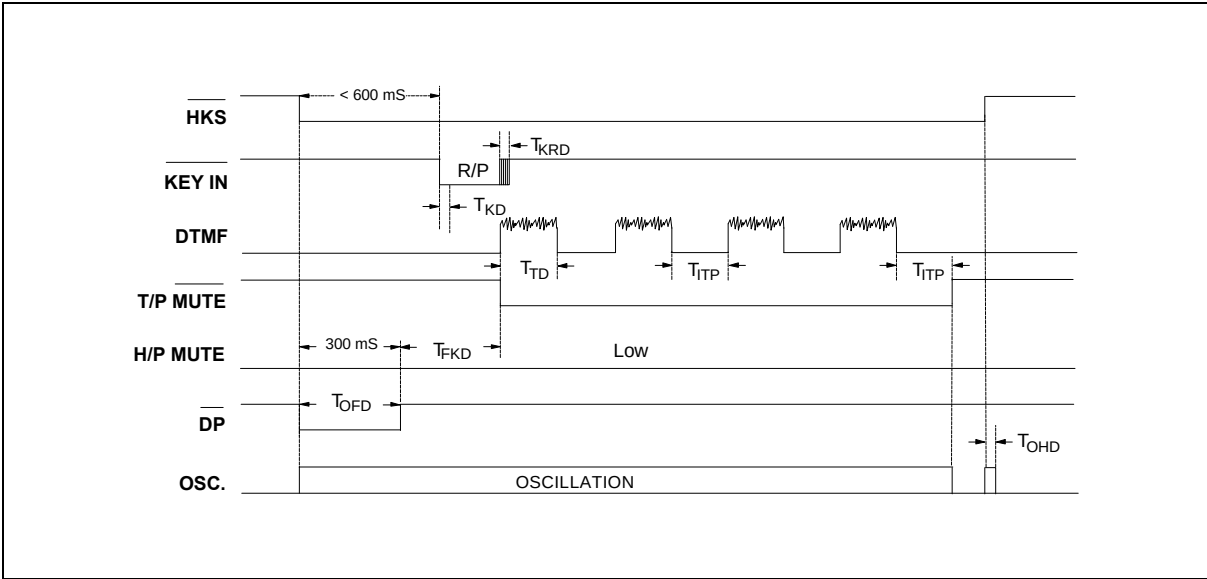


Figure 2(d). Auto Dialing Timing Diagram (Tone Mode with Lock Function)

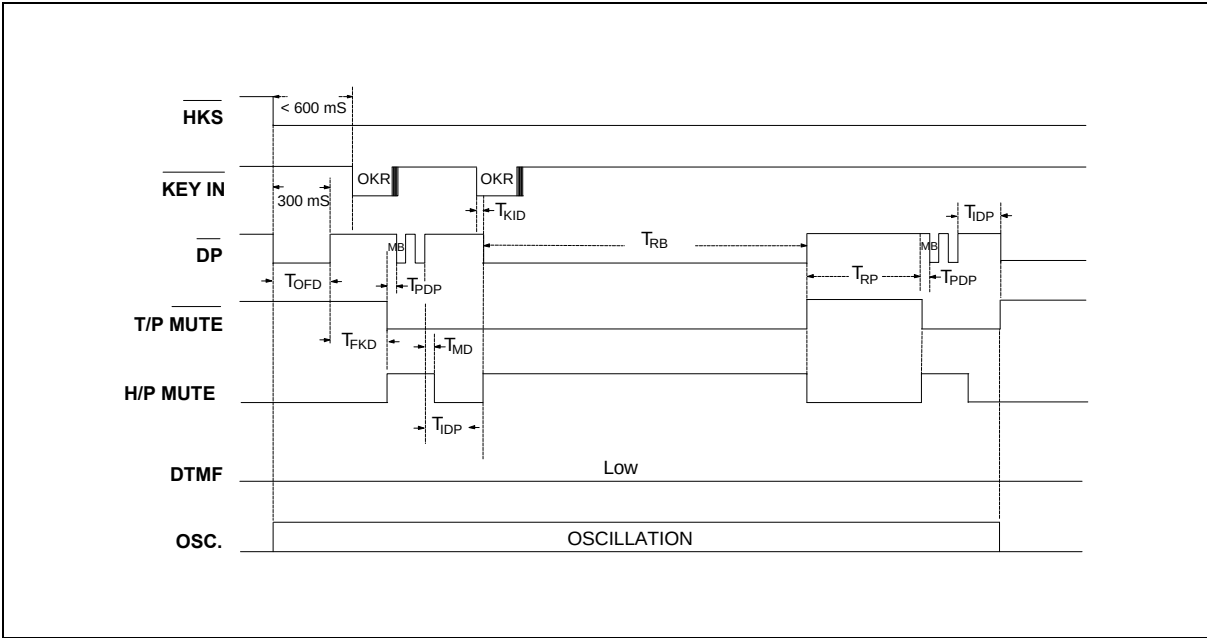


Figure 3. One-key Redial Timing Diagram

Preliminary W91510DN SERIES



Timing Waveforms, continued

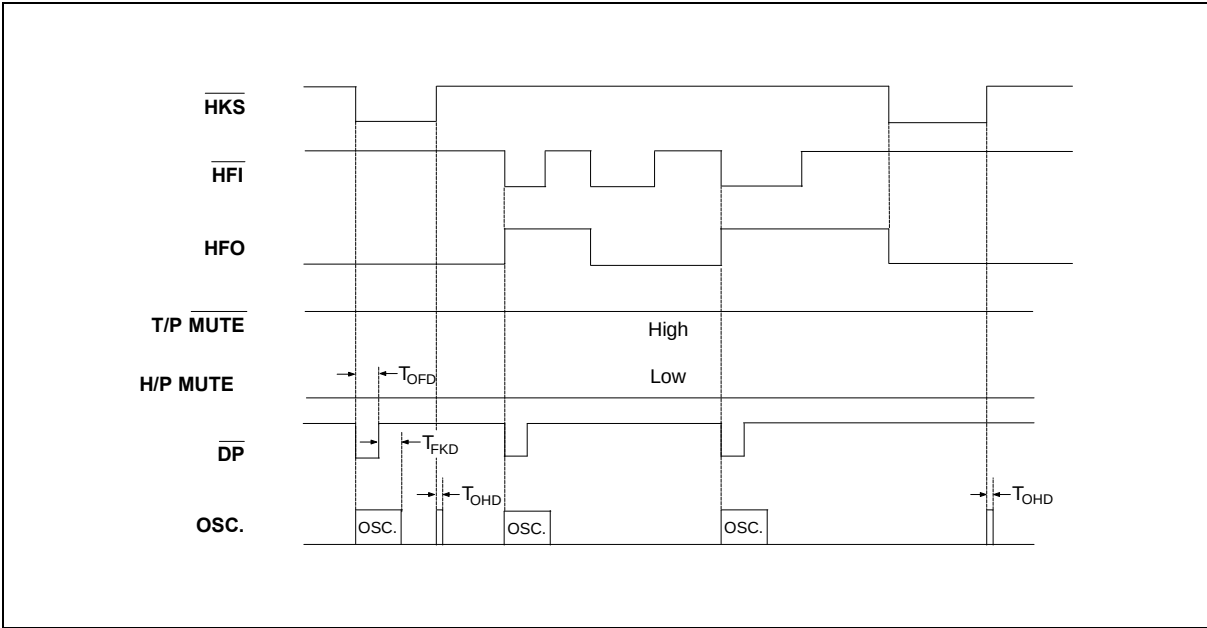


Figure 4(a). Handfree Timing Diagram (with Lock Function)

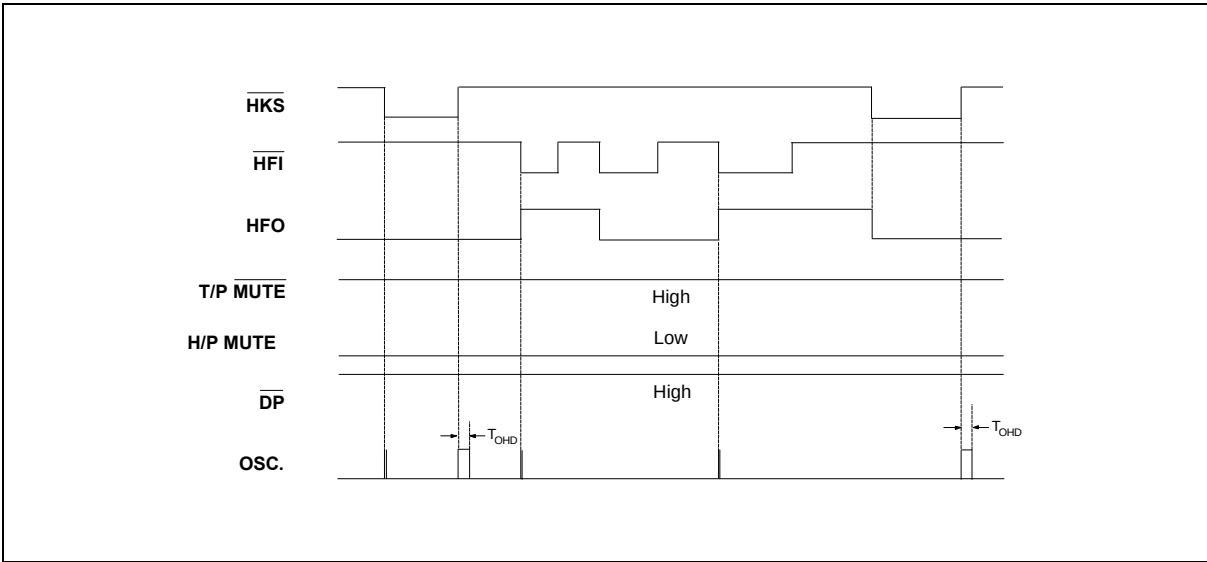


Figure 4(b). Handfree Timing Diagram (Without Lock Function)

Preliminary W91510DN SERIES



Timing Waveforms, continued

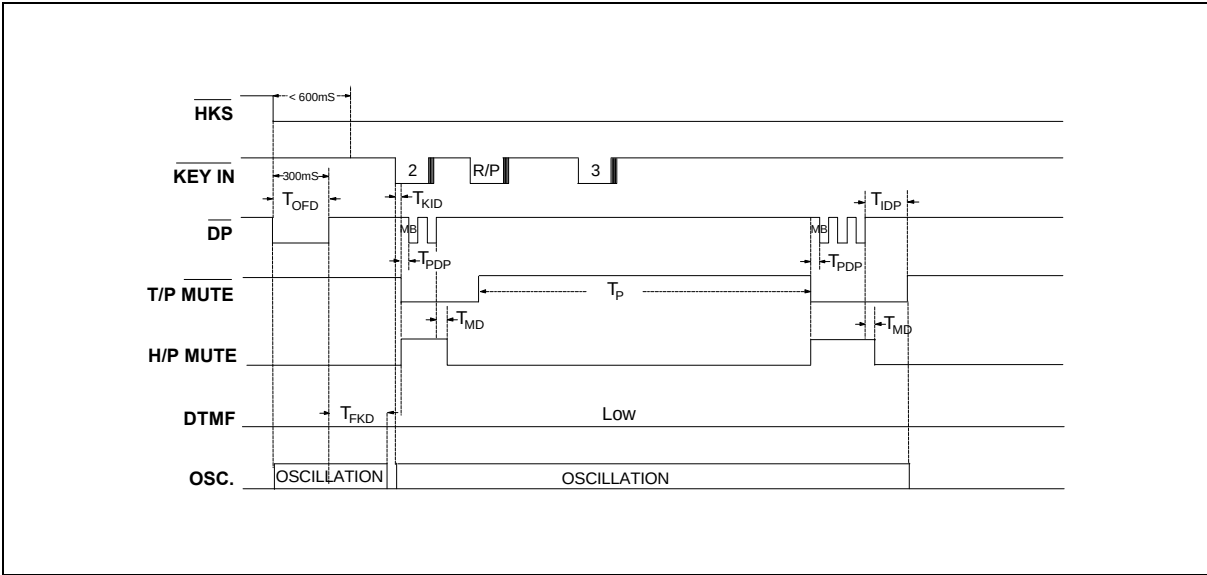


Figure 5. Pause Function Timing Diagram (Pulse Mode)

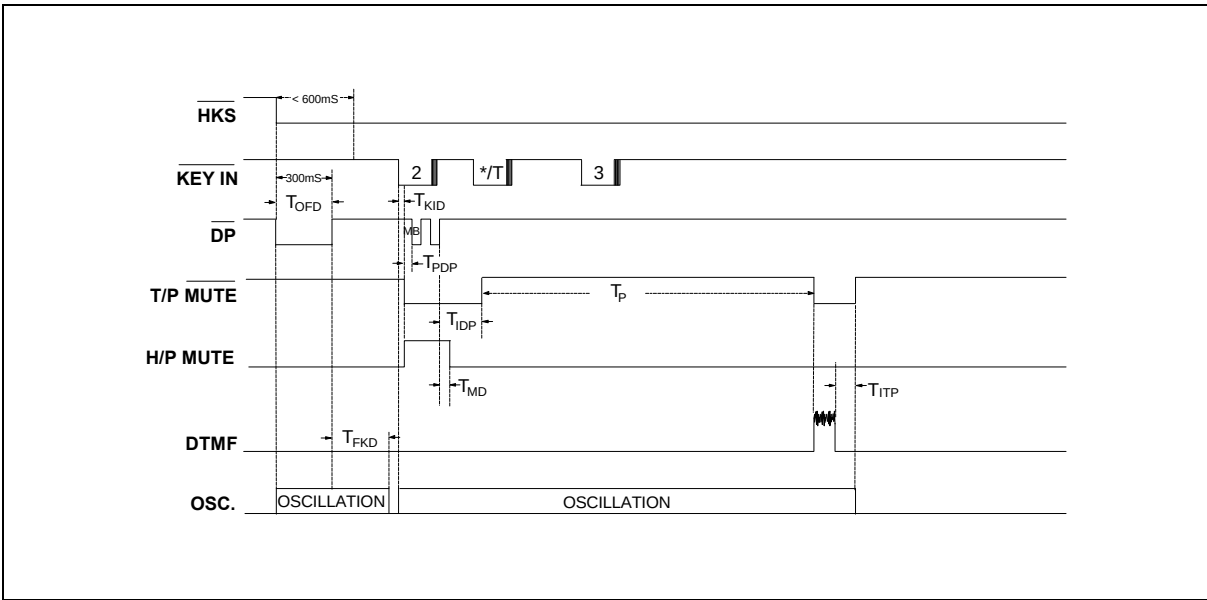


Figure 6(a). Pulse-to-tone Timing Diagram

Preliminary W91510DN SERIES



Timing Waveforms, continued

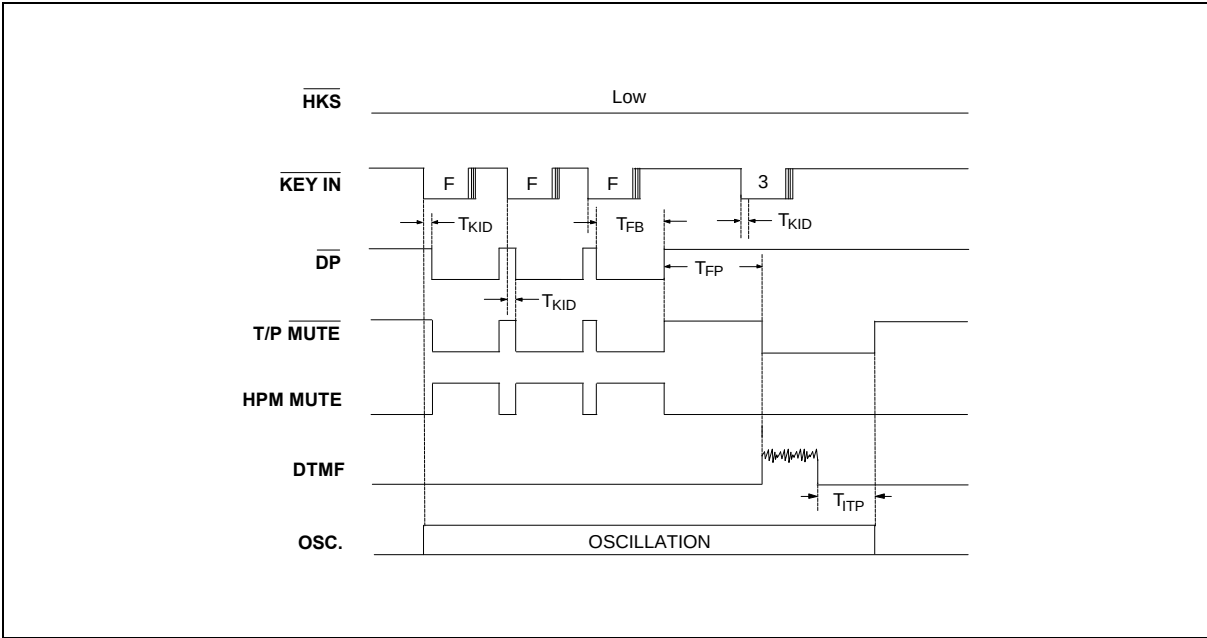


Figure 7. First Priority Flash Timing Diagram

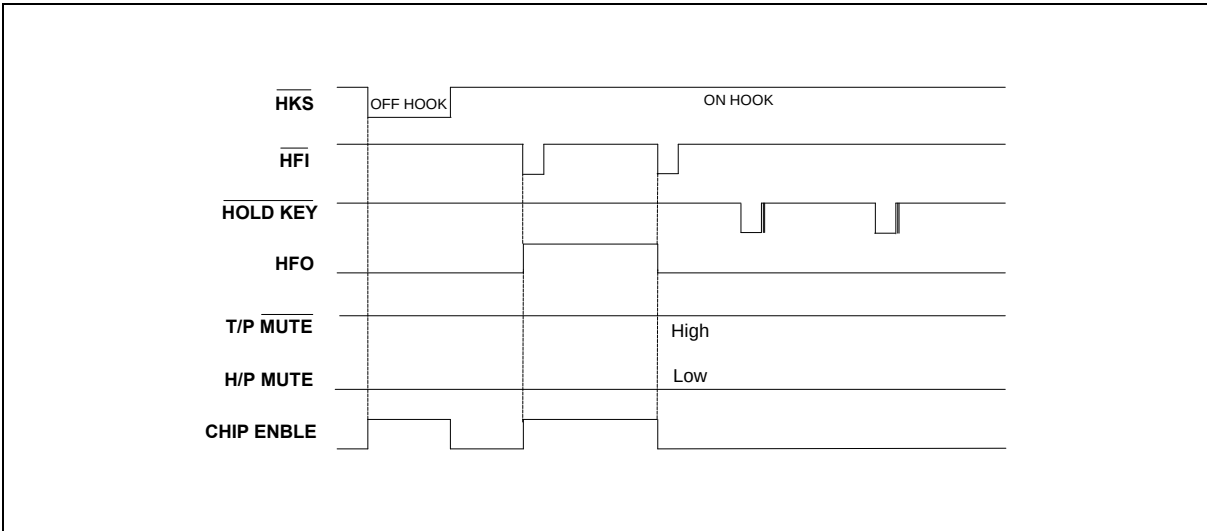


Figure 8(a). Hold and Handfree Timing Diagram

Note: The HOLD KEY cannot be enabled when chip is disabled.

Preliminary W91510DN SERIES



Timing Waveforms, continued

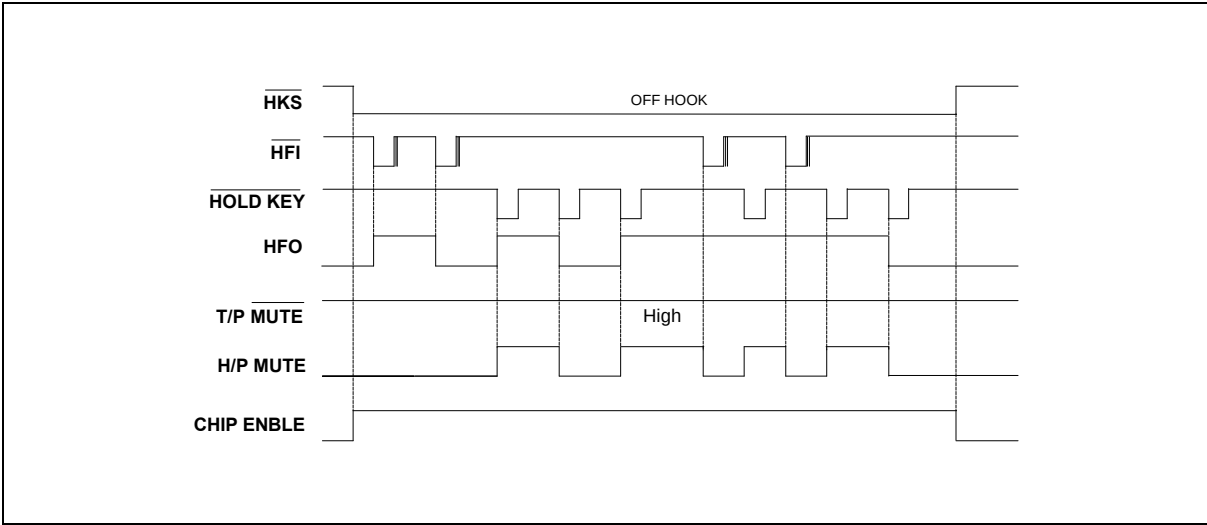


Figure 8(b). Hold and Handfree Timing Diagram

Note: The $\overline{\text{HFI}}$ and $\overline{\text{HOLD KEY}}$ inputs will toggle the HFO signal; as soon as either $\overline{\text{HFI}}$ or $\overline{\text{HOLD KEY}}$ is activated, the HFO signal will go high and previous activate inputs will be ignored.

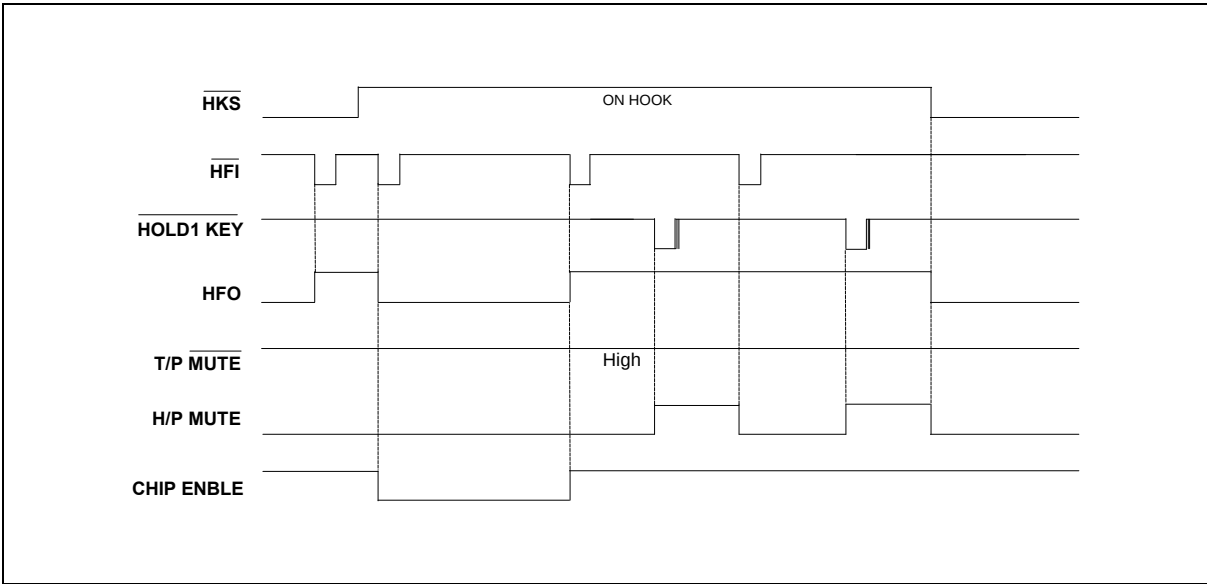


Figure 8(c). Hold and Handfree Timing Diagram

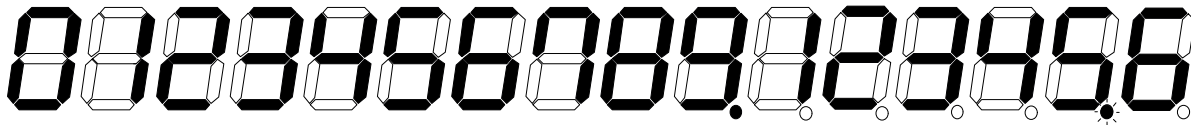
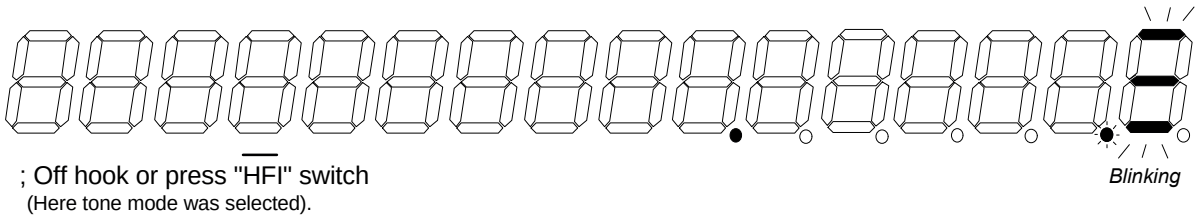
Note: Changing the state of the $\overline{\text{HKS}}$ signal from high to low will initialize the HFO and H/P MUTE signals.

Preliminary W91510DN SERIES

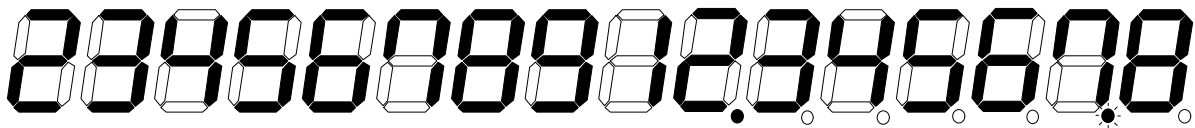


LCD DISPLAY FORMAT

A. Normal Dialing

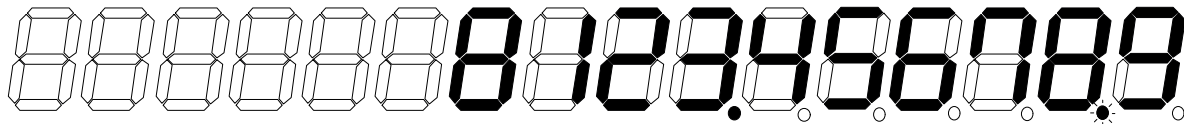
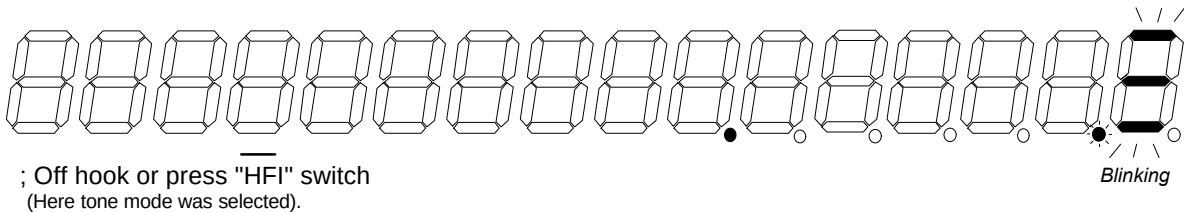


; dial" 0123456789123456"



; and "78"

B. Redialing, One touch dialing

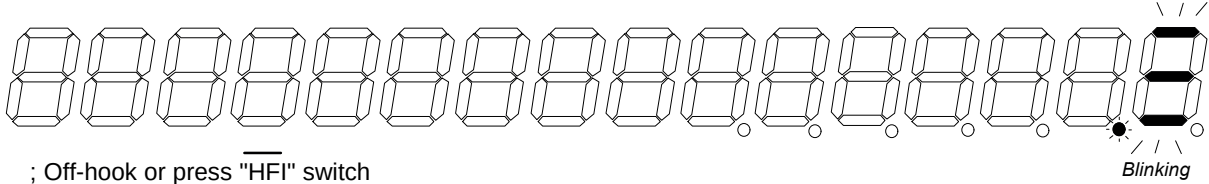


; Press "R/P" or "OKR" key
(Redial = "8123456789")

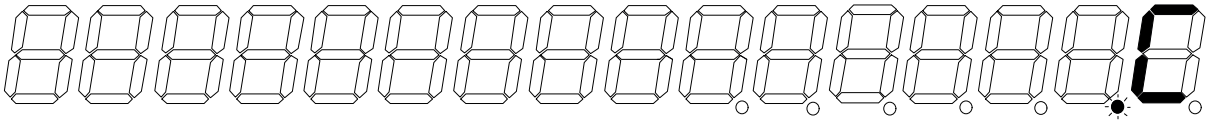
Preliminary W91510DN SERIES



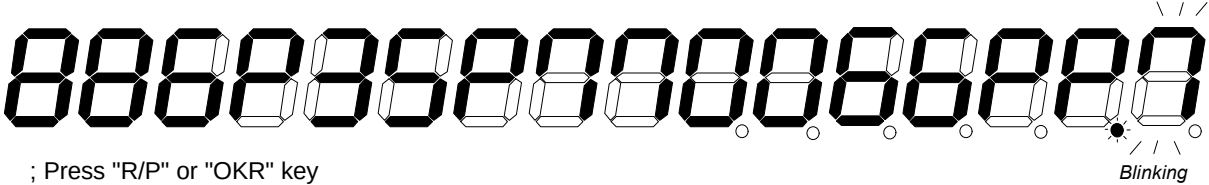
C. Redial memory Check



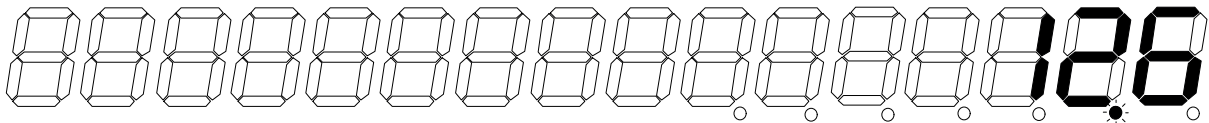
; Off-hook or press "HFI" switch
(M1= "886P35P770066PP7126", and here pulse mode was selected)



; Press "CHK" key



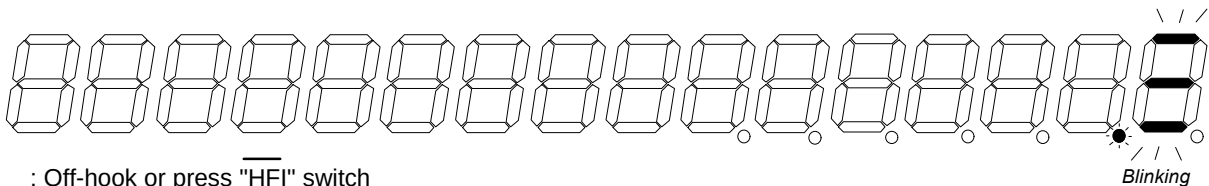
; Press "R/P" or "OKR" key
(Display 1 to 16 digits)



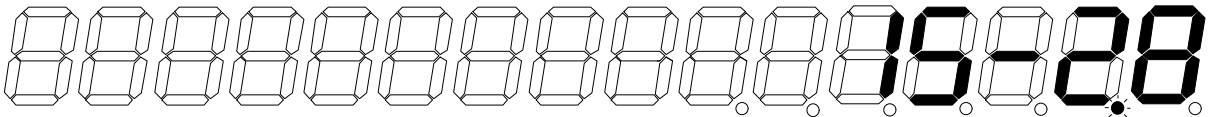
; Press "any key"
(Display 17 to 19 digits)

D. Timer Function

a.

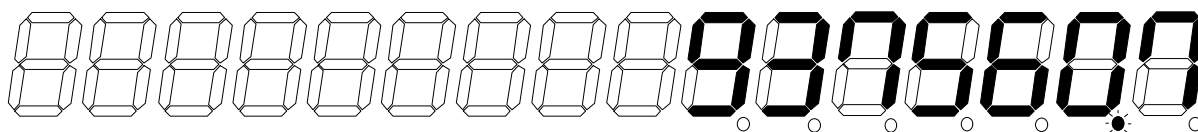


; Off-hook or press "HFI" switch
(Here pulse mode was selected)

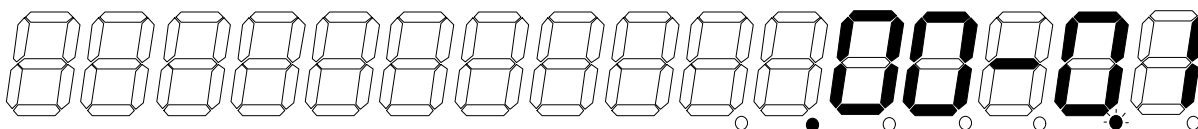


; Press "CHK" key
(Display last calling time)

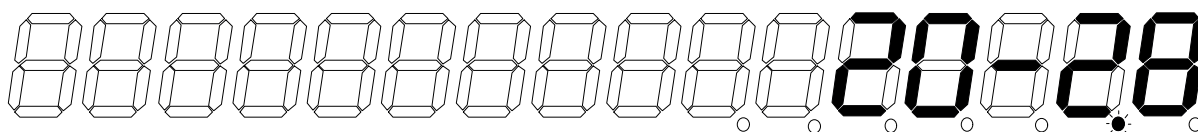
Preliminary W91510DN SERIES



; Dial "9375607"

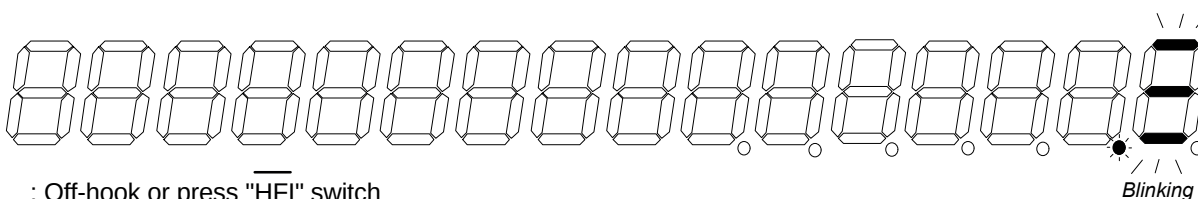


; If "9375607" is dialed completed, the system will start timer after 6 seconds
(Timer will start counting up)

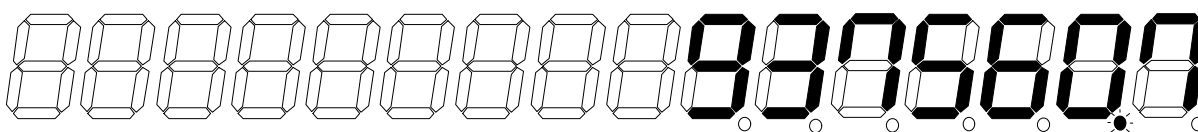


; Press "TIM" key
(Timer will stop)

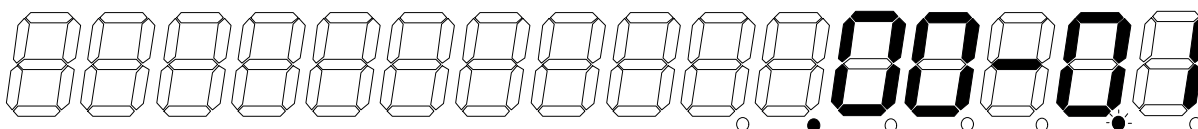
b.



; Off-hook or press "HFI" switch
(here pulse mode was selected)

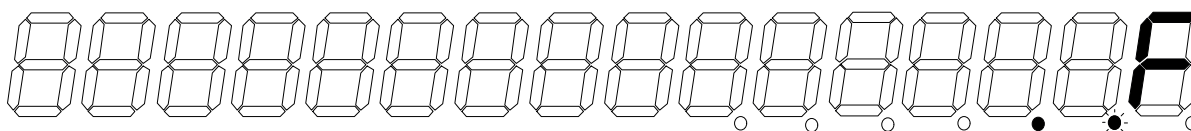


; Dial "9375607"

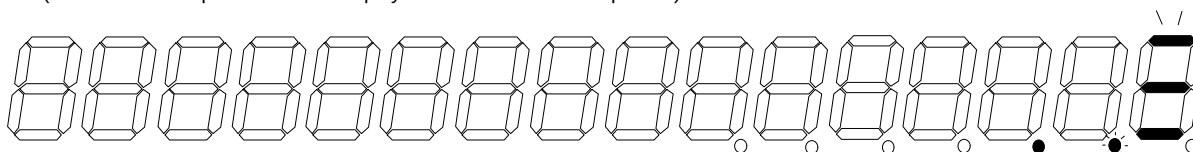


; If "9375607" is dialed completed
press "TIM" key
(Timer will start counting up)

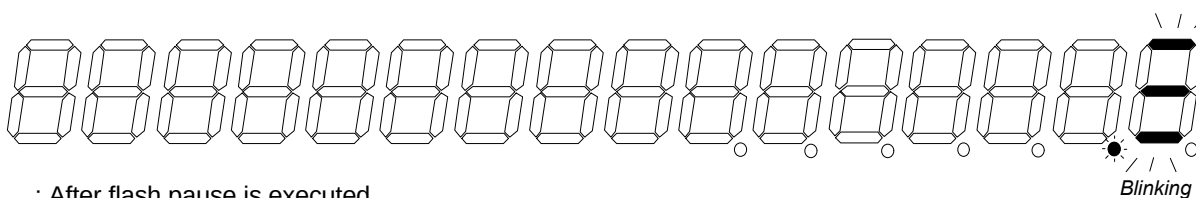
Preliminary W91510DN SERIES



; Press "F1", "F2", "F3" or "F4" key
(The timer will stop and LCD will display a flash mark and flash pattern)

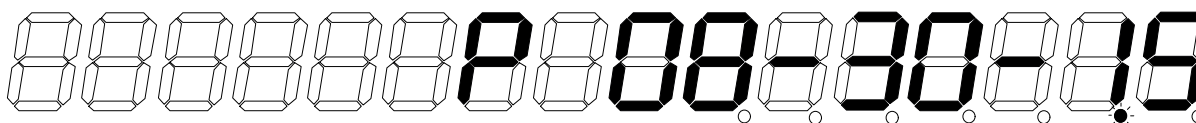


; After flash break is executed

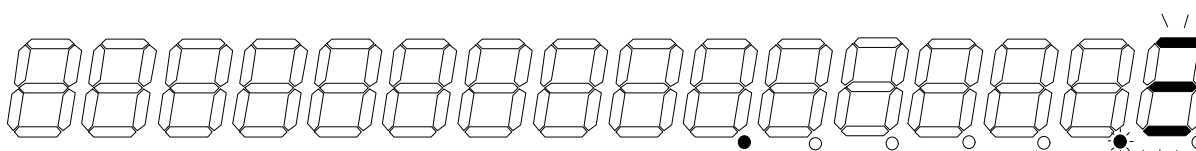


; After flash pause is executed

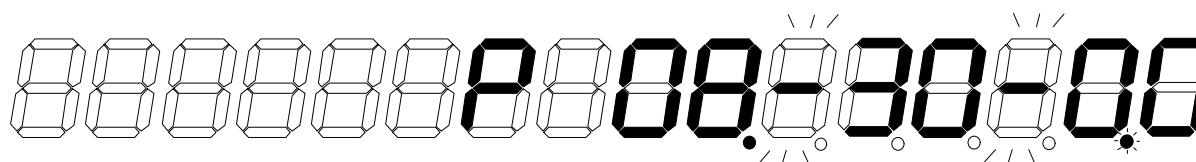
E. RTC Setting Function



; On-hook
(Display real time)

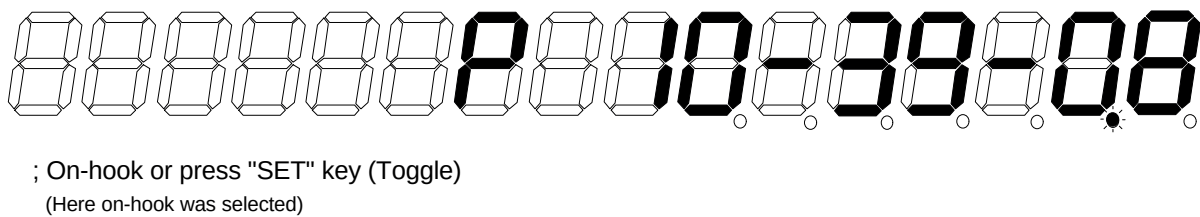
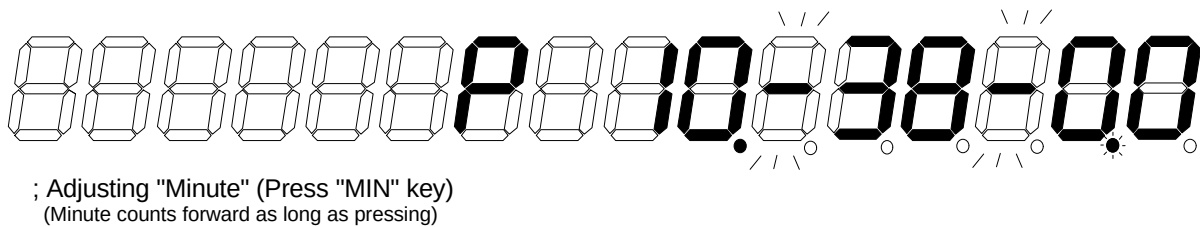
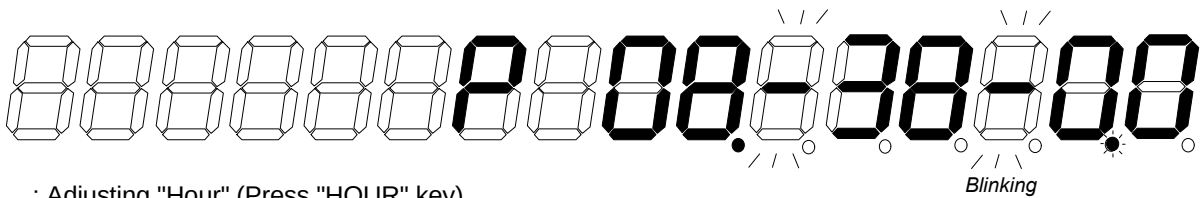


; Off-hook, before press "SET" key
(Here tone mode was selected)

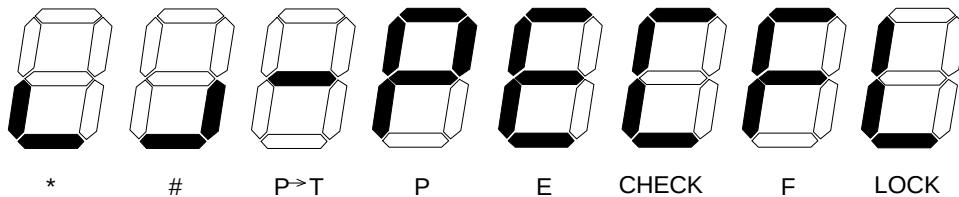
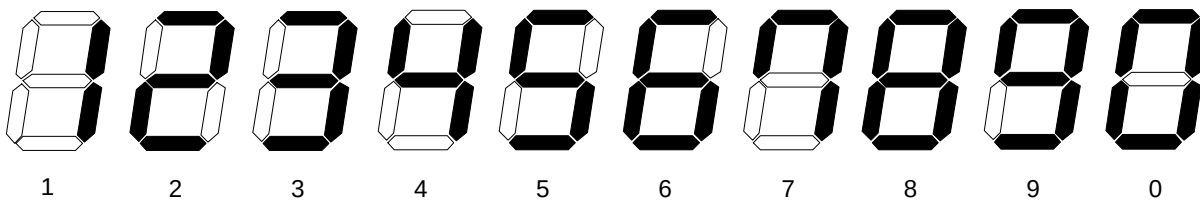


; Entering "Setting Mode" (Press "SET" key)

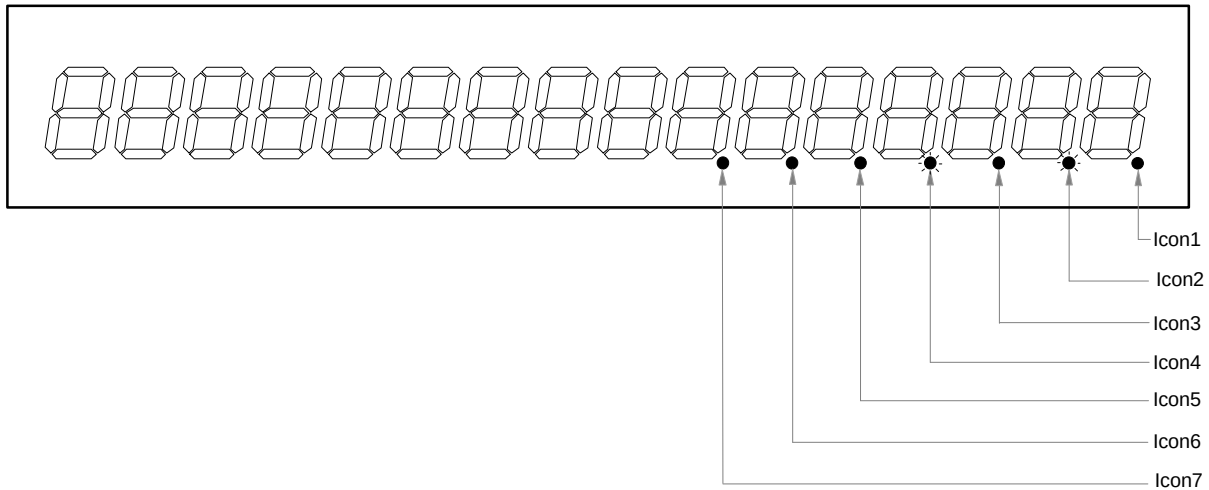
Preliminary W91510DN SERIES



LCD PATTERN FOR DATA

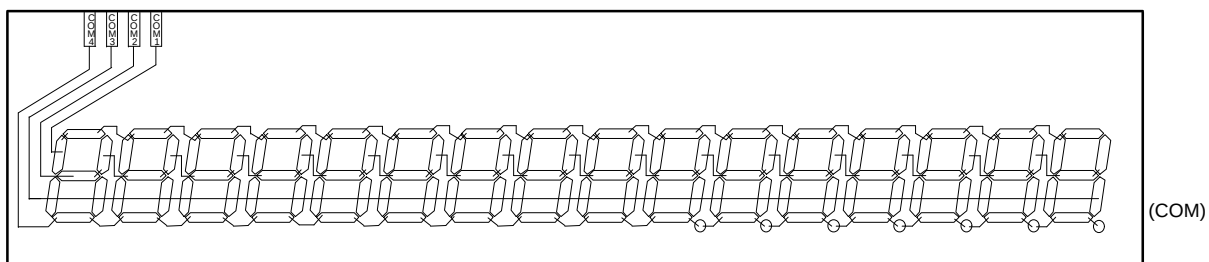
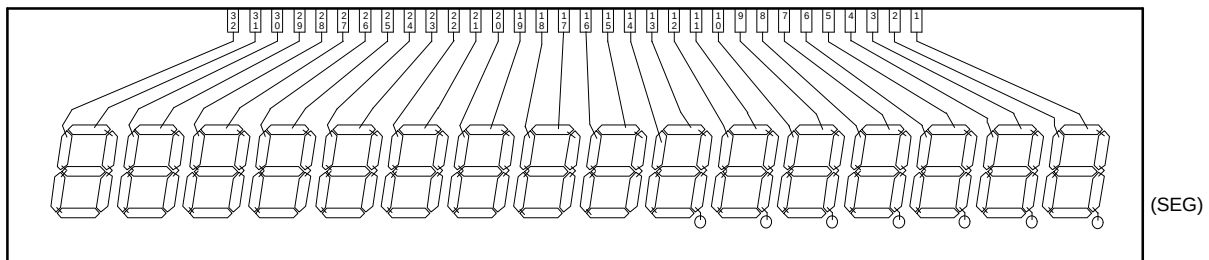


Preliminary W91510DN SERIES

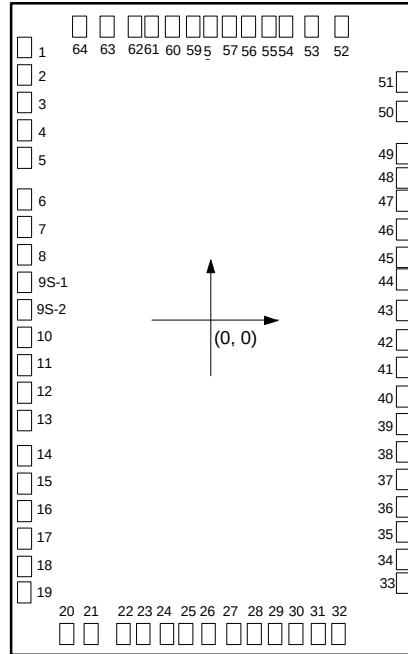


Notes:

- Icon1: Pause
- Icon2: The icon will be blinking after power on.
- Icon3: Flash
- Icon4: Hold
- Icon5: Handfree
- Icon6: Timer
- Icon7: Tone



Bonding Pad Diagram



Notes:

1. The substrate must be connected to Vss.
2. The chip size is $2940 \times 3630 \mu\text{m}^2$

Preliminary W91510DN SERIES



Pad List

PAD NO.	PAD NAME	PIN #	X	Y	PAD NO.	PAD NAME	PIN #	X	Y
1	SEG29	1	-1335.00	1430.70	33	OCM1	33	1335.00	-1307.90
2	SEG30	2	-1335.00	1294.50	34	COM2	34	1335.00	-1166.10
3	SEG31	3	-1335.00	1158.50	35	COM3	35	1335.00	-1024.30
4	SEG32	4	-1335.00	1022.30	36	COM4	36	1335.00	-882.50
5	VDD	5	-1335.00	883.40	37	SEG1	37	1335.00	-746.30
6	DTMF	6	-1335.00	665.20	38	SEG2	38	1335.00	-607.50
7	VSS	7	-1335.00	515.50	39	SEG3	39	1335.00	-471.30
8	T/P MUTE	8	-1335.00	373.50	40	SEG4	40	1335.00	-335.30
9S-1	H/P MUTE	9*	-1335.00	229.30	41	SEG5	41	1335.00	-199.10
9S-2	LOCK	9*	-1335.00	88.20	42	SEG6	42	1335.00	-63.00
10	HFO	10	-1335.00	-49.80	43	SEG7	43	1335.00	73.00
11	DP/C6	11	-1335.00	-191.80	44	SEG8	44	1335.00	209.20
12	MODE	12	-1335.00	-327.80	45	SEG9	45	1335.00	345.20
13	COL1	13	-1335.00	-467.80	46	SEG10	46	1335.00	481.40
14	COL2	14	-1335.00	-627.20	47	SEG11	47	1335.00	617.40
15	COL3	15	-1335.00	-769.20	48	SEG12	48	1335.00	753.60
16	COL4	16	-1335.00	-928.60	49	SEG13	49	1335.00	889.60
17	COL5	17	-1335.00	-1070.60	50	SEG14	50	1335.00	1102.10
18	ROW1	18	-1335.00	-1226.40	51	SEG15	51	1335.00	1270.80
19	ROW2	19	-1335.00	-1368.40	52	SEG16	52	941.30	1657.50
20	ROW3	20	-1080.40	-1679.90	53	SEG17	53	749.00	1657.50
21	ROW4	21	-841.70	-1679.90	54	SEG18	54	534.80	1657.50
22	XT1	22	-598.40	-1679.90	55	SEG19	55	398.60	1657.50
23	XT1	23	-453.20	-1679.90	56	SEG20	56	262.60	1657.50
24	HKS	24	-307.90	-1679.90	57	SEG21	57	126.40	1657.50
25	HFI	25	-167.90	-1679.90	58	SEG22	58	-9.60	1657.50
26	XT2	26	24.20	-1679.90	59	SEG23	59	-145.80	1657.50
27	XT2	27	188.80	-1679.90	60	SEG24	60	-281.80	1657.50
28	VRTC1	28	326.30	-1679.90	61	SEG25	61	-418.00	1657.50
29	VLCD	29	488.50	-1679.90	62	SEG26	62	-554.00	1657.50
30	VRTC2	30	636.30	-1679.90	63	SEG27	63	-757.70	1657.50
31	CN	31	798.50	-1679.90	64	SEG28	64	-932.00	1657.50
32	CP	32	946.30	-1679.90					

Note: "*" is bonding option.

Publication Release Date: May 1997

Revision A2

Preliminary W91510DN SERIES



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5792697

<http://www.winbond.com.tw/>

Voice & Fax-on-demand: 886-2-7197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-7190505
FAX: 886-2-7197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.

2730 Orchard Parkway, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-9436668

Note: All data and specifications are subject to change without notice.