



## Video Graphics Controller

### FEATURES

#### □ Integrated Video Graphics Controller

- 64-bit graphics engine
- Integrated video accelerator
- On-chip 24-bit true color RAMDAC with up to 135 MHz pixel clock rate
- On-chip clock synthesizers generating up to 135 MHz VCLK and 80 MHz MCLK

#### □ Graphics Engine

- 64-bit graphics acceleration
- 8/16/24 bit-per-pixel true color acceleration
- Deep command queue to improve GE performance
- Bit block transfer between system memory and display memory
  - HostBLT
  - Pattern BLT
  - Color/font expanding BLT
  - Transparent BLT
  - Color/font expansion
  - Rectangle fill
  - 256 three-operand (source, pattern and destination) ROPs
- Bresenham line drawing
- Short stroke vector drawing
- Rectangle and line clipping
- $64 \times 64 \times 2$  or  $32 \times 32 \times 2$  hardware cursor

#### □ Video Acceleration

- Video (YUV) and graphics (RGB) shared frame buffer architecture
- Two-dimensional bilinear interpolation scaling with 1-pixel resolution from  $1 \times 1$  to  $8 \times 8$
- On-chip standard CCIR 601 YUV to RGB color space conversion
- Cropping window and filtering supports
- Hardware support for Microsoft DirectDraw feature set
  - Double buffering and page flipping to prevent from tearing in image
  - Transparent BitBLTs of sprites for game

- acceleration
  - Color keying, chroma keying and window keying to overlay video and graphics streams
  - On-the-fly blending of video and graphics streams
- Supports  $2 \times$  scaling to allow  $320 \times 200$  game image to be displayed at  $640 \times 480$  full-screen resolution
- High-quality video playback requiring only 1 MByte DRAM in  $1024 \times 768$  256-color mode
- Dual hardware-accelerated video windows for video conference applications

#### □ Multimedia Video Interface

- Glueless MPEG-1 video decoder (W9920DF) support for YUV 4:2:2 video input
- Glueless TV decoder support for YUV 4:2:2, NTSC or PAL live-video input
- Support for RGB 5:5:5, 5:6:5 or YUV 4:2:2 software CODEC video input
- Glueless support for 16-bit baseline VESA Advanced Feature Connector (VAFC)
- Glueless support for 8-bit bidirectional pass-through VGA feature connector

#### □ Compatibility

- 100% hardware compatible with IBM VGA standard
- VESA BIOS extension support and VESA monitor timing compliant
- Driver support for all major operating systems, such as Windows 3.1, Windows 95, Windows NT, and OS/2 Warp 3.0

#### □ System Bus Interface

- Glueless support for 32-bit PCI Local Bus Revision 2.1 specification
- Zero-wait-state PCI burst mode support
- Linear addressing
- Memory-mapped I/O

#### □ Display Memory Interface

- 64 or 32-bit DRAM interface in a 1, 2, or 4 MByte configuration
- Flexible interface support for  $128K \times 8$ ,  $128K \times 16$ ,  $256K \times 4$ ,  $256K \times 8$ , or  $256K \times 16$  DRAMs



- EDO DRAM support, dual-CAS# and dual-WE# ×16 DRAMs support
- Auto memory size detection and auto bank switching
- Supports UMA (Unified Memory Architecture) to share frame buffer with system memory
- **Green PC support**
  - VESA DPMS
- RAMDAC/clock synthesizers power management
- **Smart monitor control**
  - VESA-compatible DDC1 and DDC2
- **Packaging**
  - 208-pin PQFP package

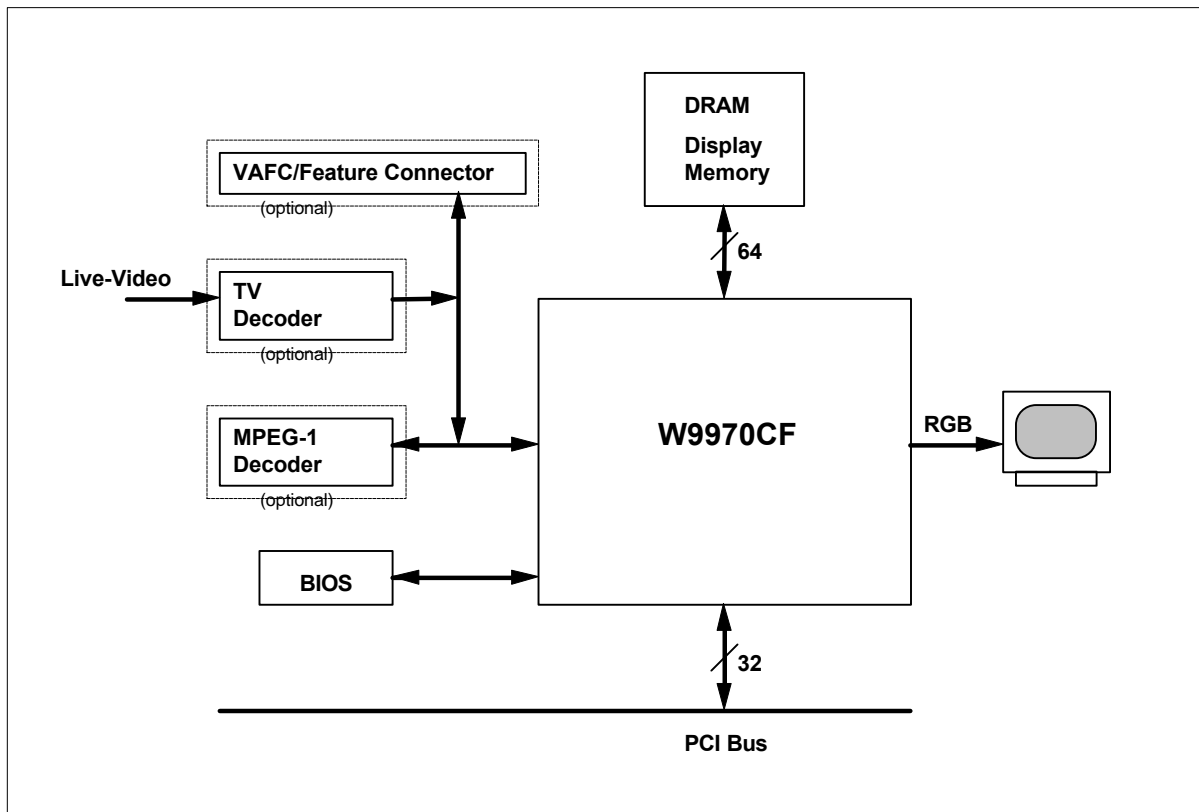


Figure 1. W9970CF System Application Diagram



## OVERVIEW

The W9970CF Integrated Video Graphics Accelerator is a highly integrated product offered by Winbond to provide high-performance graphical user interface (GUI) acceleration and TV-quality full-screen motion video acceleration for PCI Bus-based IBM PCs or their compatibles. An on-chip RAMDAC and dual programmable clock synthesizers with up to 135 MHz pixel data rate are also integrated to simplify system design and reduce cost.

The W9970CF is a high-performance graphics accelerator specially designed for the Microsoft Windows family, IBM OS/2, and DOS-based applications. Besides the 100% IBM VGA register-level compatibility, the W9970CF incorporates a 64-bit graphics engine (GE) to accelerate drawing functions such as bit block transfer (BitBLT), line drawing, clipping, and hardware cursor manipulation.

The integrated video accelerator (VA) features high-quality video filtering, bilinear interpolation scaling along both the X and Y axes, color space conversion and overlay keying. In addition to accelerating software video playback, the W9970CF also provides an advanced multimedia video interface for glueless

interfacing to the Winbond W9920DF MPEG-1 video decoder and TV decoders such as the Philips SAA7110 and Brooktree Bt815A/7A/9A. The 16-bit baseline VESA Advanced Feature Connector (VAFC) and the 8-bit bidirectional IBM Feature Connector are also supported for legacy video applications. By performing scaling and color space conversion on the fly, the W9970CF provides high-quality video playback in  $1024 \times 768$  256-color mode with only 1 MBytes of DRAM.

The integration of a GE, a VA, RAMDAC and dual clock synthesizers in one chip provides an all-in-one controller for graphics and video display subsystem. The flexible display memory interface design of the W9970CF allows system designers to select various types of DRAMs, including  $128K \times 8$ ,  $128K \times 16$ ,  $256K \times 4$ ,  $256K \times 8$ , and  $256K \times 16$  in either fast page or extended data out (EDO) modes.

The W9970CF supports a glueless interface with the 32-bit PCI Local Bus. Green PC power management is supported via VESA Display Power Management Signaling (DPMS) and power-down of the on-chip RAMDAC and clock synthesizers. The VESA DDC1 and DDC2 smart monitor control is also supported.

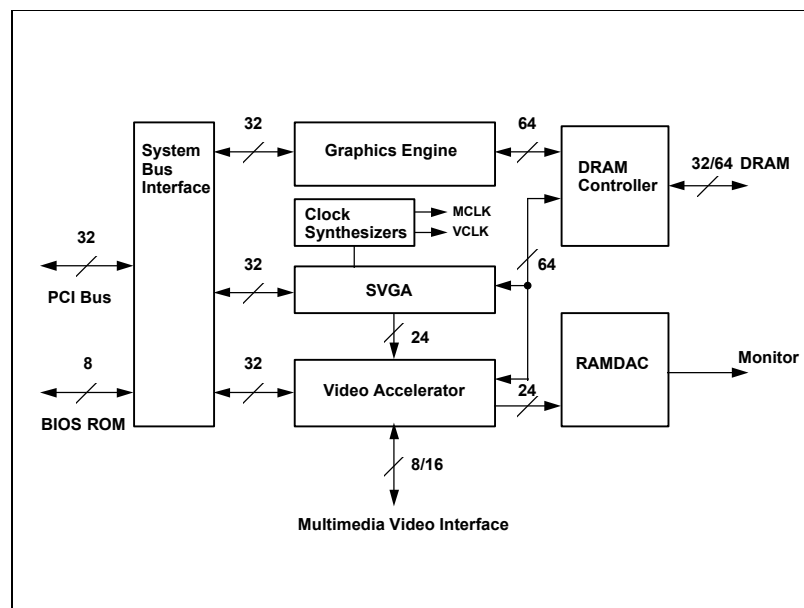


Figure 2. W9970CF Block Diagram



## GRAPHICS ENGINE

The 64-bit graphics engine (GE) is specially designed to improve the performance of applications such as Microsoft Windows and other graphical user interface software. Performance is enhanced by accelerating GUI functions such as BitBLTs, Bresenham line draw, and short stroke vector. The GE performs several types of BitBLTs, including HostBLT, pattern BLT, color/font expanding BLT, transparent BLT, color expansion, and rectangle fill, with 256 ROPS on source, pattern, and destination. The graphics engine operates at all pixel depths in enhanced modes, including 8/16/24 bit-per-pixel modes. A  $64 \times 64 \times 2$  or  $32 \times 32 \times 2$  hardware cursor, fully compatible with Microsoft Windows, is used to speed up cursor performance and accelerate all graphics operations by eliminating the CPU overhead associated with cursor manipulation.

## VIDEO ACCELERATOR

The Video Accelerator is a high-quality video processor for enhancing and displaying video images. It not only accelerates software video playback but also facilitates the interface to MPEG-1 video decoders and TV decoders.

The video accelerator employs back-end color space conversion and a scaling mechanism (see Figure 3). Video and game-generated graphics frames are read from an off-screen buffer and sent to the overlay and blending control block as the secondary stream. Color space conversion and scaling are performed along the way. This on-the-fly video acceleration and overlaying ensure game and video playback at full speed.

### Color Space Conversion

The built-in color space converter converts YUV format to 24-bit RGB format according to the CCIR 601-2 Recommendation.

### Down Scaling

The down-scaling function is performed by dropping

pixels or lines. To support arbitrary scaling factors, the video accelerator uses a digital differential accumulator (DDA) to drop pixels or lines smoothly. The scaling factor may range from 1/64 to 63/64.

### Scaling up by 2D Interpolation

Rather than duplicating pixels or lines for enlargement, the video accelerator uses a 2-D bilinear interpolation algorithm to enhance the output for high-quality video display.

The interpolation algorithm creates seven weighted, intermediate values between two original pixels or lines, which allows a maximum of 800% enlargement. For non-integer scaling, a 10-bit DDA with 1/1024 resolution is used to interpolate pixels by averaging.

### 2x Scaling

The 2x scaling located in the RAMDAC is used to optionally scale up, both horizontally and vertically, by a factor of 2 for the overlaid data stream. This is used to scale  $320 \times 240$  game-generated frames to full screen.

### Filtering

The video accelerator provides horizontal RGB or YUV filtering to reduce noise and aliasing artifacts in the video data stream

### Cropping

A rectangular cropping window is supported in the video accelerator for subsampling the incoming video data stream. Only video located in the cropping window can be stored into the off-screen buffer.

### Alpha Blending

Alpha blending is supported for overlaying the primary stream and secondary stream. The alpha value can be 1 bit or 3 bits. The 1-bit alpha depth overlaying (also known as software key) is supported only for the pixel format of RGB 1:5:5:5, where the alpha bit value of 0 is transparent and value of 1 is opaque.

An overlay control register specifies the 3-bit alpha value for the primary stream ( $K_p$ ) and secondary stream ( $K_s$ ). Note that  $K_p + K_s$  must be  $\leq 8$ . The blending equation is  $[P_p \times K_p + P_s \times K_s]/8$ , where  $P_p$



is the primary stream pixel data and Ps is the secondary stream pixel data.

**Overlay Control**

The overlay controller provides control for overlaying of four input sources: the primary stream (normally the graphics data), secondary stream, blending stream, and FC/VAFC pass-through data stream. When the hardware cursor is active, it is overlaid on top of all stream images. The W9970CF supports a range of advanced forms of keying including window key, color

key, chroma key, software key (1-bit alpha overlaying in RGB 1:5:5:5 format), external key (FC/VAFC only), and a logic combination of these keys.

**Dual Video Windows**

Two video windows may be displayed on the monitor simultaneously. This makes W9970CF highly suitable for video conferencing applications. If the two video windows are placed at different scan lines, they can be scaled separately with different factors.

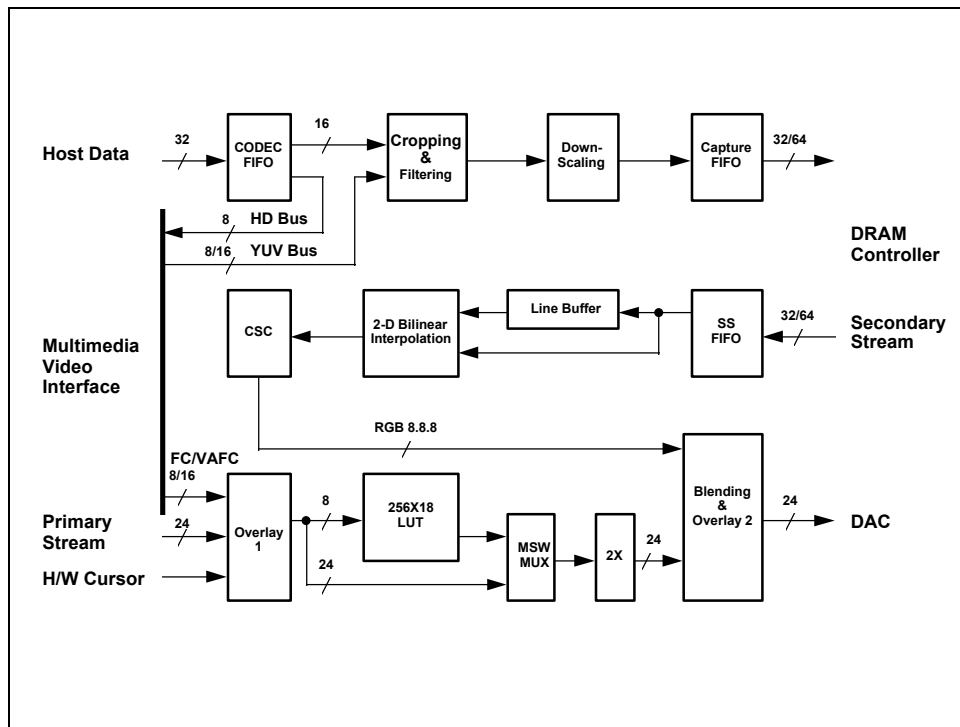


Figure 3. Video Accelerator Block Diagram

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