



May 2000  
Revised April 2003

## NC7WB3125 TinyLogic® UHS 2-Bit Low Power Bus Switch

### General Description

The NC7WB3125 is a 2-bit ultra high-speed CMOS FET bus switch with TTL-compatible active LOW control inputs. The low On Resistance of the switch allows inputs to be connected to outputs with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 2-bit switch with independent bus enable ( $\overline{OE}$ ) controls. When  $\overline{OE}$  is LOW, the switch is ON and Port A is connected to Port B. When  $\overline{OE}$  is HIGH, the switch is OPEN and a high-impedance state exists between the two ports. Control inputs tolerate voltages up to 5.5V independent of  $V_{CC}$ .

### Features

- Space saving US8 surface mount package
- MicroPak™ leadless package
- Typical 3Ω switch resistance at 5.0V  $V_{CC}$
- Minimal propagation delay through the switch
- Power down high impedance input/output
- Zero bounce in flow through mode
- TTL compatible active LOW control inputs
- Control inputs are overvoltage tolerant
- Bus switch replacement for Logic x125 part

### Ordering Code:

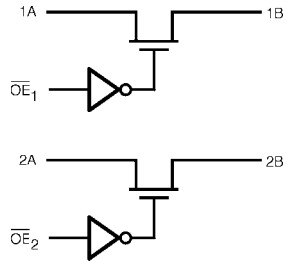
Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WB3125K8X	MAB08A	WB25	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
NC7WB3125L8X (Preliminary)	MAC08A	T4	8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

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### Logic Diagram



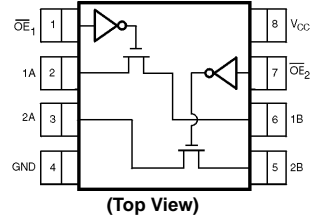
### Pin Descriptions

Pin Name	Description
A	Bus A
B	Bus B
$\overline{OE}$	Bus Enable Input

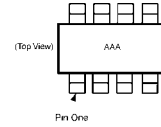
### Function Table

Bus Enable Input $\overline{OE}$	Function
L	B Connected to A
H	Disconnected

### Connection Diagrams

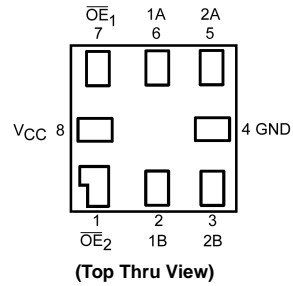


### Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code  
**Note:** Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

### Pad Assignments for MicroPak



### Absolute Maximum Ratings (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output ( $I_{OUT}$ ) Current	128 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}/I_{GND}$ )	$\pm 100$ mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature under Bias ( $T_J$ )	+150°C
Junction Lead Temperature ( $T_L$ ) (Soldering, 10 Seconds)	+260°C
Power Dissipation ( $P_D$ ) @ +85°C	250 mW

### Recommended Operating Conditions (Note 3)

Supply Operating ( $V_{CC}$ )	4.0V to 5.5V
Control Input Voltage ( $V_{IN}$ )	0V to 5.5V
Switch Input Voltage ( $V_{IN}$ )	0V to 5.5V
Output Voltage ( $V_{OUT}$ )	0V to 5.5V
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
Switch Control Input	0 ns/V to 5 ns
Switch I/O	0 ns/V to DC
Thermal Resistance ( $\theta_{JA}$ )	250°C/W

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Unused logic inputs must be held HIGH or LOW. They may not float.

### DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Units	Conditions
			Min	Typ	Max		
$V_{IK}$	Clamp Diode Voltage	4.5			-1.2	V	$I_{IN} = -18$ mA
$V_{IH}$	HIGH Level Input Voltage	4.0 to 5.5	2.0			V	
$V_{IL}$	LOW Level Input Voltage	4.0 to 5.5			0.8	V	
$V_{OH}$	HIGH Level Output Voltage	4.0 to 5.5	See Figure 3			V	$V_{IN} = V_{CC}$
$I_{IN}$	Input Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq V_{IN} \leq 5.5V$
$I_{OFF}$	Switch OFF Leakage Current	5.5			$\pm 1.0$	$\mu\text{A}$	$0 \leq A, B \leq V_{CC}$
$R_{ON}$	Switch On Resistance (Note 4)	4.5		3	7	$\Omega$	$V_{IN} = 0V, I_{IN} = 64$ mA
		4.5		3	7		$V_{IN} = 0V, I_{IN} = 30$ mA
		4.5		6	15		$V_{IN} = 2.4V, I_{IN} = 15$ mA
		4.0		10	20		$V_{IN} = 2.4V, I_{IN} = 15$ mA
$I_{CC}$	Quiescent Supply Current	5.5			3	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input (Note 5)	5.5		1	2.5	mA	$V_{IN} = 3.4V$ , One $\overline{OE}$ Input only, Other $\overline{OE} = V_{CC}$

**Note 4:** Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

**Note 5:** Per TTL driven input ( $V_{IN} = 3.4V$ , control input only). A and B pins do not contribute to  $I_{CC}$ .

## AC Electrical Characteristics

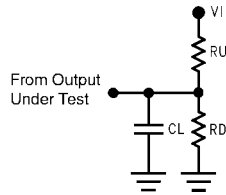
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF, R <sub>U</sub> = R <sub>D</sub> = 500Ω			Units	Conditions	Figure Number
			Min	Typ	Max			
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus (Note 6)	4.0 to 5.5			0.25	ns	V <sub>I</sub> = OPEN	Figures 1, 2
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	4.5 to 5.5	0.8	2.5	4.2	ns	V <sub>I</sub> = 7V for t <sub>PZL</sub> V <sub>I</sub> = 0V for t <sub>PZH</sub>	Figures 1, 2
		4.0	0.8	3.0	4.6			
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	4.5 to 5.5	0.8	3.1	4.8	ns	V <sub>I</sub> = 7V for t <sub>PLZ</sub> V <sub>I</sub> = 0V for t <sub>PHZ</sub>	Figures 1, 2
		4.0	0.8	2.9	4.4			

**Note 6:** This parameter is guaranteed by design. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance). The specified limit is calculated on this basis.

## Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions
C <sub>IN</sub>	Control Pin Input Capacitance	2.5		pF	V <sub>CC</sub> = 0V
C <sub>I/O (OFF)</sub>	Port Off Capacitance	6		pF	V <sub>CC</sub> = 5.0V = $\overline{OE}$
C <sub>I/O (ON)</sub>	Switch ON Capacitance	12		pF	V <sub>CC</sub> = 5.0V, $\overline{OE}$ = 0V

## AC Loading and Waveforms



Input driven by 50Ω source terminated in 50Ω  
C<sub>L</sub> includes load and stray capacitance  
Input PRR = 1.0 MHz; t<sub>W</sub> = 500 ns

FIGURE 1. AC Test Circuit

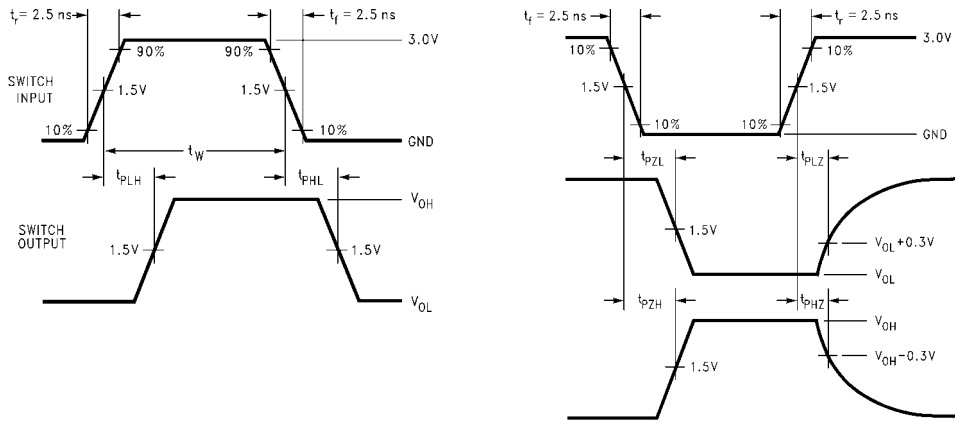


FIGURE 2. AC Waveforms

**DC Characteristics**

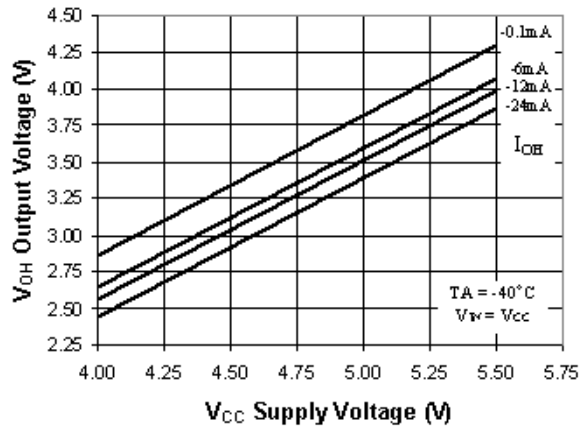
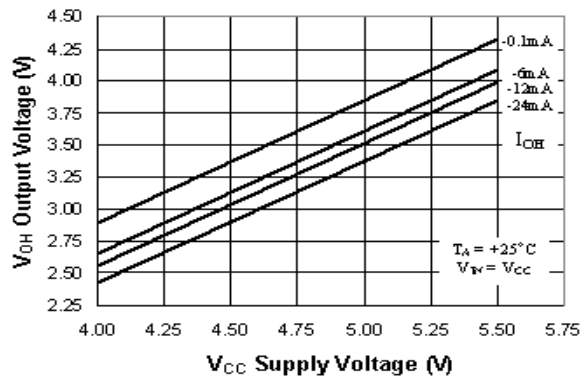
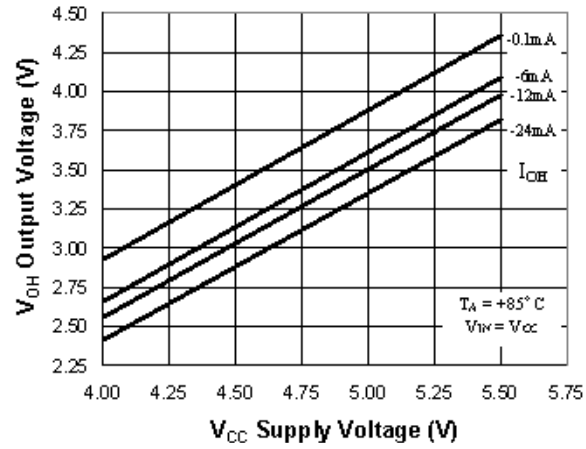
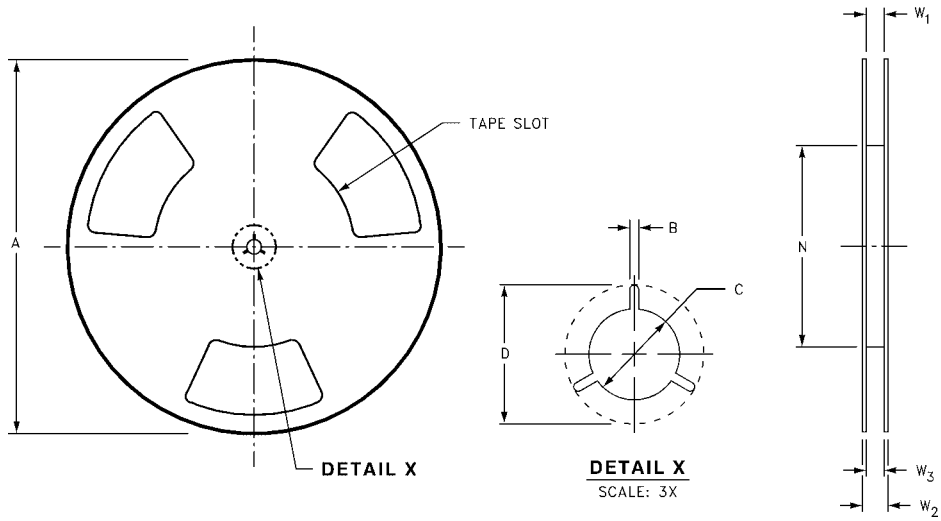


FIGURE 3. Typical High Level Output Voltage vs. Supply Voltage



**Tape and Reel Specification** (Continued)

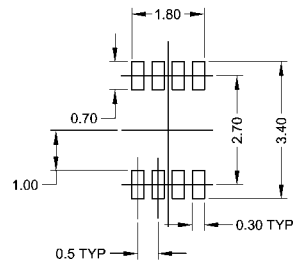
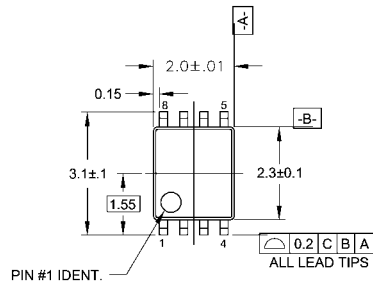
REEL DIMENSIONS inches (millimeters)



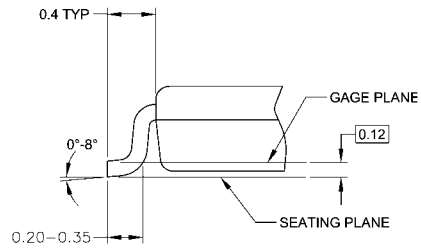
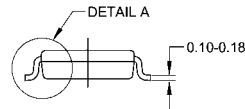
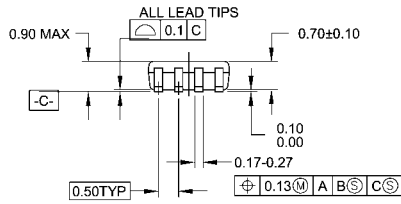
Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

NC7WB3125

**Physical Dimensions** inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DETAIL A

NOTES:

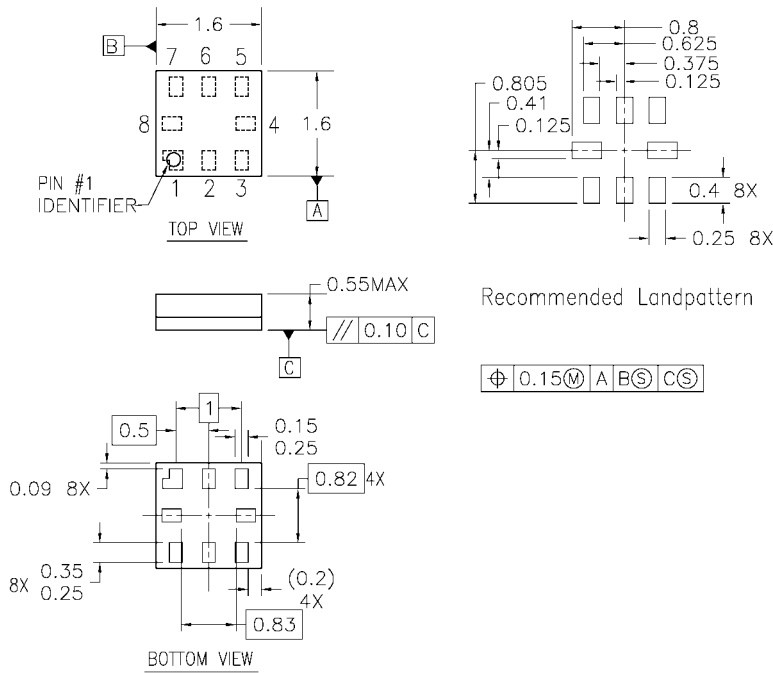
- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide  
Package Number MAB08A**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



- Notes:
1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
  2. DIMENSIONS ARE IN MILLIMETERS
  3. DRAWING CONFORMS TO ASME Y.14M-1994

MAC08AREVB

**8-Lead MicroPak, 1.6 mm Wide  
Package Number MAC08A  
(Preliminary)**

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