

FAIRCHILD
SEMICONDUCTOR™

May 2000
Revised August 2003

NC7WB66

TinyLogic® Low Voltage UHS Dual SPST Normally Open Bus Switch

General Description

The NC7WB66 is an ultra high-speed (UHS) dual single-pole/single-throw (SPST) bus switch. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance over a broad V_{CC} range. The device is specified to operate over the 1.65 to 5.5V V_{CC} operating range. The device is organized as a dual switch with independent CMOS compatible switch enable (OE) controls. When OE is HIGH, the switch is ON and Port A is connected to Port B. When OE is LOW, the switch is OPEN and a high-impedance state exists between the two ports. The enable inputs tolerate voltages up to 5.5V independent of the V_{CC} operating range.

Features

- Useful in both analog and digital applications
- Space saving US8 surface mount package
- MicroPak™ leadless package
- Typical 7Ω On Resistance @ 5V V_{CC}
- Broad V_{CC} operating range: 1.65V to 5.5V
- Rail-to-rail signal handling
- Power down high impedance control inputs
- Control inputs are overvoltage tolerant
- Control inputs are CMOS compatible

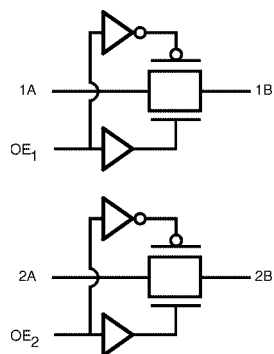
Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description	Supplied As
NC7WB66K8X	MAB08A	WB66	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3K Units on Tape and Reel
NC7WB66L8X	MAC08A	P4	8-Lead MicroPak, 1.6 mm Wide	5K Units on Tape and Reel

TinyLogic® is a registered trademark of Fairchild Semiconductor Corporation.
MicroPak™ is a trademark of Fairchild Semiconductor Corporation.



Logic Symbol



Pin Descriptions

Pin Names	Description
A	Switch Port A
B	Switch Port B
OE	Control Input

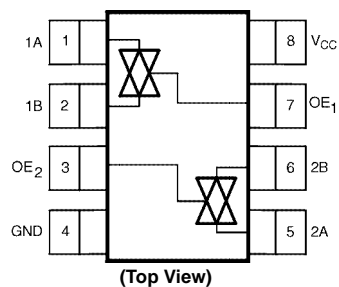
Function Table

Switch Enable Input (OE)	Function
L	Disconnect
H	B Connected to A

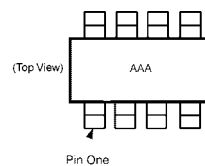
H = HIGH Logic Level

L = LOW Logic Level

Connection Diagrams



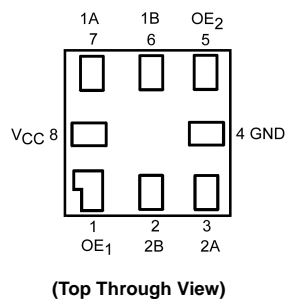
Pin One Orientation Diagram



AAA represents Product Code Top Mark - see ordering code

Note: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Pad Assignments for MicroPak



Absolute Maximum Ratings^(Note 1)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Switch Voltage (V_S)	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage (V_{IN}) (Note 2)	-0.5V to +7.0V
DC Input Diode Current	
@ (I_{IK}) $V_{IN} < 0V$	-50 mA
DC Switch Output Current (I_{OUT})	±128 mA
DC V_{CC} or Ground Current (I_{CC}/I_{GND})	±100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Junction Lead Temperature	
under Bias (T_J)	+150°C
Junction Lead Temperature (T_L)	
(Soldering, 10 Seconds)	+260°C
Power Dissipation (P_D) @ +85°C	
SC70-6	250 mW

Recommended Operating Conditions^(Note 3)

Supply Voltage (V_{CC})	1.65V to 5.5V
Control Input Voltage (V_{IN})	0V to 5.5V
Switch Input Voltage (V_{IN})	0V to V_{CC}
Switch Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
Control Input $V_{CC} = 1.65V-2.7V$	0 ns/V to 20 ns/V
Control Input $V_{CC} = 3.0V-3.6V$	0 ns/V to 10 ns/V
Control Input $V_{CC} = 4.5V-5.5V$	0 ns/V to 5 ns/V
Thermal Resistance (θ_{JA})	250°C/W

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min		
V _{IH}	HIGH Level Input Voltage	1.65–1.95	0.75 V _{CC}		0.75 V _{CC}		V	
		2.3–5.5	0.7 V _{CC}		0.7 V _{CC}			
V _{IL}	LOW Level Input Voltage	1.65–1.95	0.25 V _{CC}		0.25V _{CC}		V	
		2.3–5.5	0.3 V _{CC}		0.3 V _{CC}			
I _{IN}	Input Leakage Current	0–5.5	±0.1		±1.0		μA	0 ≤ V _{IN} ≤ 5.5V
I _{OFF}	Switch OFF Leakage Current	1.65–5.5	±0.1		±1.0		μA	0 ≤ A, B ≤ V _{CC}
R _{ON}	Switch ON Resistance (Note 4)	4.5	6	10	10		Ω	V _I = 0V, I _O = 30 mA
			7	13.5	13.5			V _I = 2.4V, I _O = -30 mA
			6	10	10			V _I = 4.5V, I _O = -30 mA
		3.0	7.5	15	15		Ω	V _I = 0V, I _O = 24 mA
			8.5	15	15			V _I = 3V, I _O = -24 mA
		2.3	9	20	20		Ω	V _I = 0V, I _O = 8 mA
			10.5	20	20			V _I = 2.3V, I _O = -8 mA
		1.65	12.5	30	30		Ω	V _I = 0V, I _O = 4 mA
			17	30	30			V _I = 1.65V, I _O = -4 mA
		I _{CC}	Quiescent Supply Current All Channels ON or OFF	5.5	1		10	
	Analog Signal Range	V _{CC}	0	V _{CC}	0	V _{CC}	V	
RRange	ON Resistance over	4.5	8	15	15		Ω	I _O = -30 mA, 0 ≤ V _I ≤ V _{CC}
	Signal Range	3.0	15	30	30			I _O = -24 mA, 0 ≤ V _I ≤ V _{CC}
	(Note 4)(Note 5)	2.3	45	75	75			I _O = -8 mA, 0 ≤ V _I ≤ V _{CC}
		1.65	150	275	275			I _O = -4 mA, 0 ≤ V _I ≤ V _{CC}
ΔR _{ON}	ON Resistance Match	4.5	0.2				Ω	I _O = -30 mA, V _I = 3.15
	Between Channels	3.0	0.2					I _O = -24 mA, V _I = 2.1
	(Note 4)(Note 7)	2.3	0.5					I _O = -8 mA, V _I = 1.6
		1.65	0.6					I _O = -4 mA, V _I = 1.15

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = +25°C			T _A = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
R _{flat}	ON Resistance Flatness (Note 4)(Note 5)(Note 6)	4.5		2.5	6		6		I _O = -30 mA, 0 ≤ V _I ≤ V _{CC}
		3.0		8	17.5		17.5		I _O = -24 mA, 0 ≤ V _I ≤ V _{CC}
		2.3		33	60		60		I _O = -8 mA, 0 ≤ V _I ≤ V _{CC}
		1.65		135	250		250		I _O = -4 mA, 0 ≤ V _I ≤ V _{CC}

Note 4: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 5: Guaranteed by design.

Note 6: Flatness is defined as the difference between the minimum and maximum value of ON resistance over the specified range of conditions.

Note 7: $\Delta R_{ON} = R_{ON \text{ max}} - R_{ON \text{ min}}$ measured at identical V_{CC}, temperature and voltage levels.

AC Electrical Characteristics

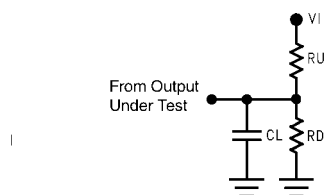
Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions	Figure Number
			Min	Typ	Max			
t _{PHL} , t _{PLH}	Propagation Delay Bus to Bus (Note 8)	4.5–5.5		0.35	1.0	ns	V _I = OPEN C _L = 50 pF, R _U = R _D = 500Ω	Figures 2, 1
		3.0–3.6		0.7	1.5			
		2.3–2.7		1.1	2.5			
		1.65–1.95		2.0	4.0			
t _{PZL} , t _{PZH}	Output Enable Time Turn on Time	4.5–5.5	0.8	2.0	3.2	ns	V _I = 0V for t _{PZH} V _I = 2 × V _{CC} for t _{PZL} C _L = 50 pF, R _U = R _D = 500Ω	Figures 2, 1
		3.0–3.6	1.2	2.5	3.9			
		2.3–2.7	1.5	3.2	5.6			
		1.65–1.95	2.5	5.7	10			
t _{PLZ} , t _{PHZ}	Output Disable Time Turn Off Time	4.5–5.5	0.8	2.6	4.1	ns	V _I = 0V for t _{PHZ} V _I = 2 × V _{CC} for t _{PLZ} C _L = 50 pF, R _U = R _D = 500Ω	Figures 2, 1
		3.0–3.6	1.5	3.4	5.0			
		2.3–2.7	2.0	4.2	6.9			
		1.65–1.95	3.0	6.2	10.5			

Note 8: This parameter is guaranteed by design. The switch contributes no propagation delay other than the RC delay of the On resistance of the switch and the 50 pF load capacitance.

Capacitance

Symbol	Parameter	Typ	Max	Units	Conditions	Figures
C _{IN}	Control Pin Input Capacitance	2.5		pF	V _{CC} = 0V	
C _{I/O} (OFF)	Switch Port Off Capacitance	5		pF	V _{CC} = 5.0V	Figure 3
C _{I/O} (ON)	Switch Port Capacitance when Switch is Enabled	10		pF	V _{CC} = 5.0V	Figure 4

AC Loading and Waveforms



Input driven by 50Ω source terminated in 50Ω
 C_L includes load and stray capacitance.
 Input PRR = 1.0 MHz; $t_w = 500$ ns

FIGURE 1. AC Test Circuit

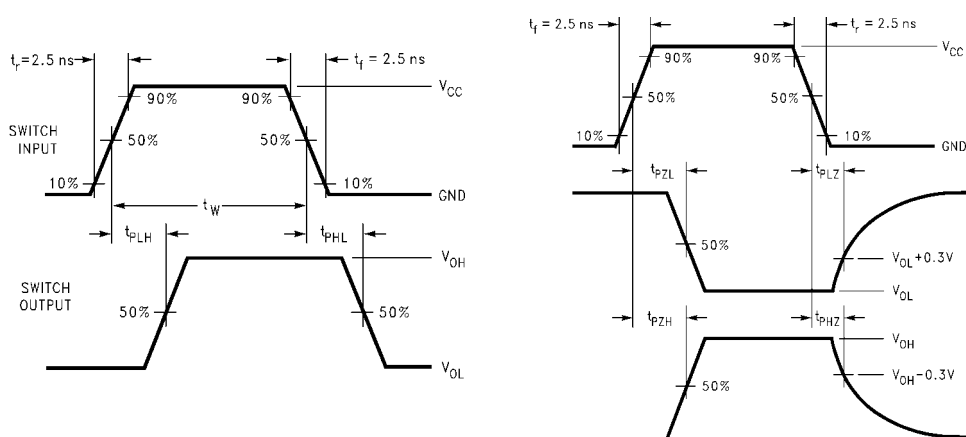


FIGURE 2. AC Waveforms

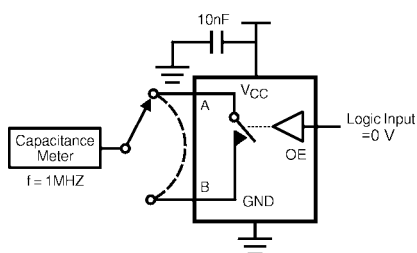


FIGURE 3. Channel Off Capacitance

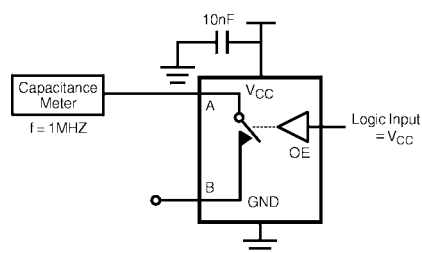


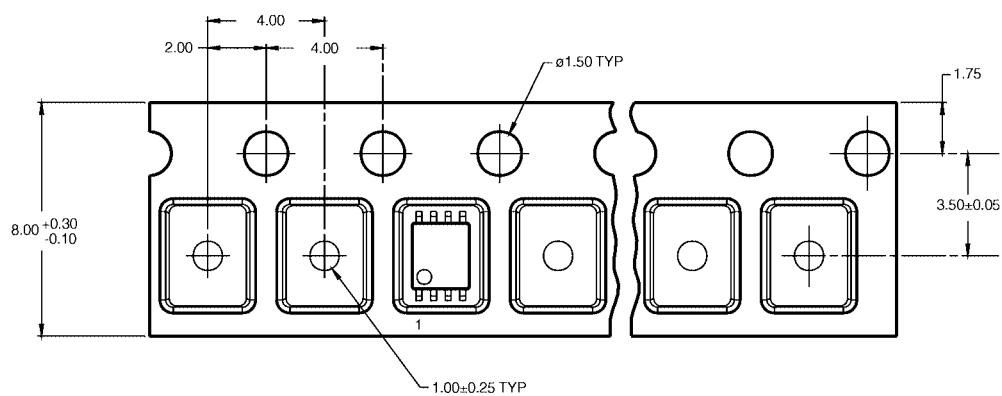
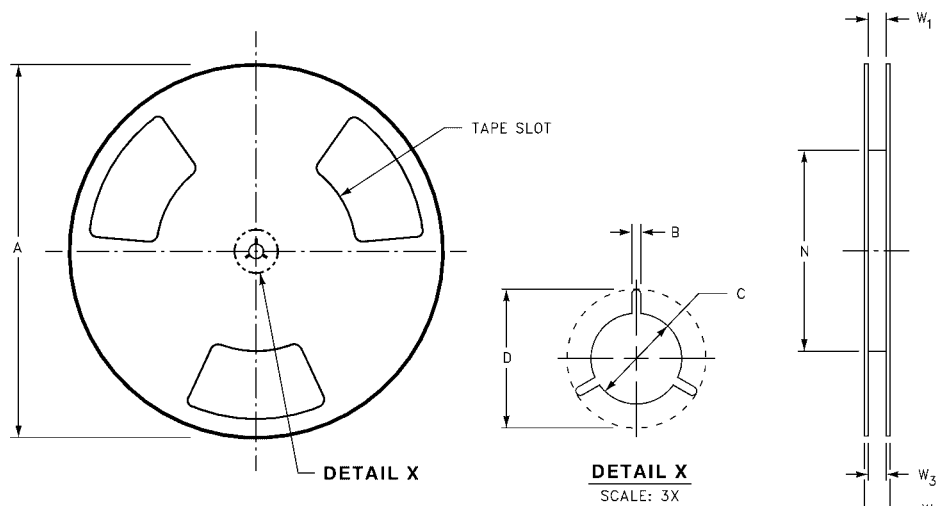
FIGURE 4. Channel On Capacitance

Tape and Reel Specification

TAPE FORMAT

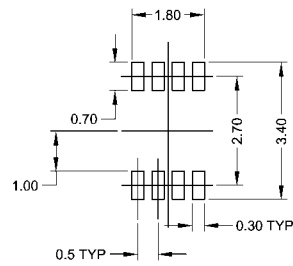
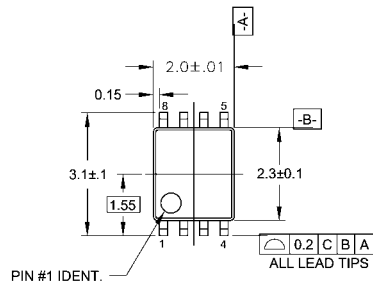
Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)

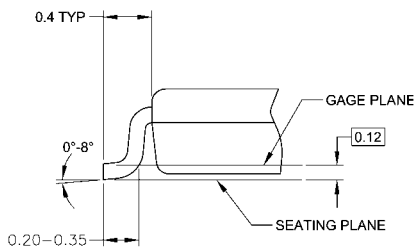
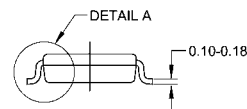
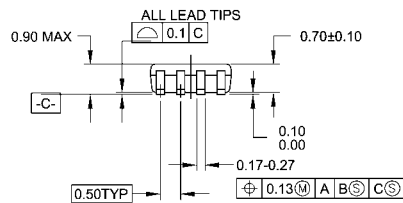
**REEL DIMENSIONS** inches (millimeters)

Type Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/–0.000 (8.40 + 1.50/–0.00)	0.567 (14.40)	W1 + 0.078/–0.039 (W1 + 2.00/–1.00)

Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



DETAIL A

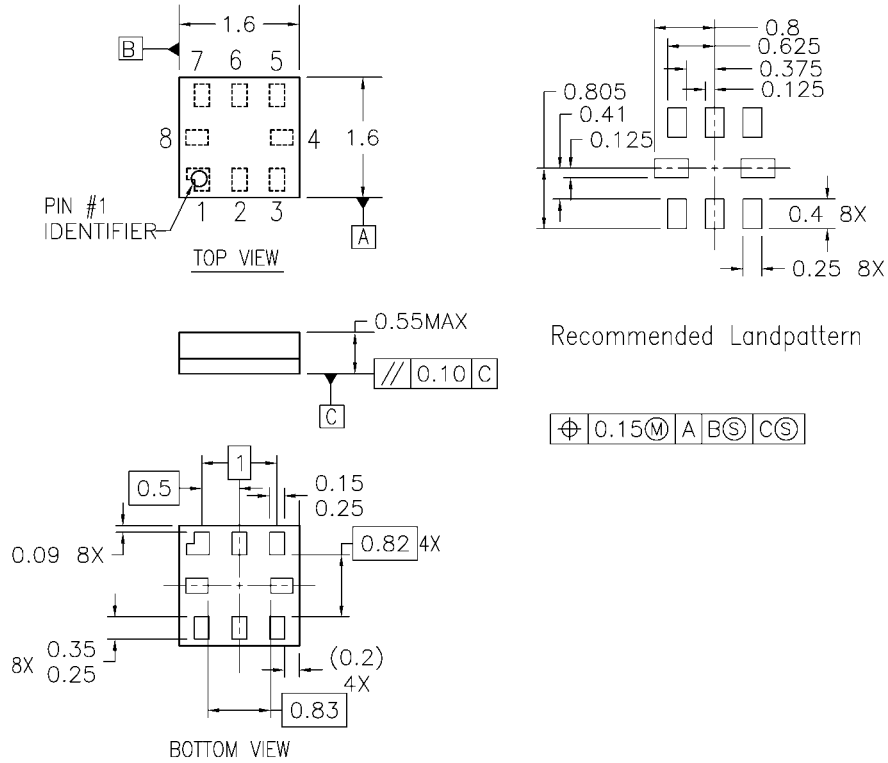
NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-187
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide
Package Number MAB08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE REGISTRATION WITH JEDEC IS ANTICIPATED
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994

MAC08AREVB

8-Lead MicroPak, 1.6 mm Wide
Package Number MAC08A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com