Preliminary

CAT24WC256

256K-Bit I²C Serial CMOS E²PROM

FEATURES

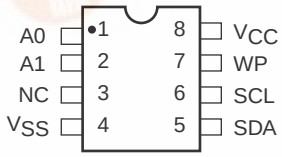
- 1MHz I²C Bus Compatible*
- 1.8 to 6 Volt Operation
- Low Power CMOS Technology
- 64-Byte Page Write Buffer
- Self-Timed Write Cycle with Auto-Clear
- Commercial, Industrial and Automotive Temperature Ranges
- Write Protect Feature
  – Entire Array Protected When WP at V_{IH}
- 100,000 Program/Erase Cycles
- 100 Year Data Retention
- 8-Pin DIP or 8-Pin SOIC

DESCRIPTION

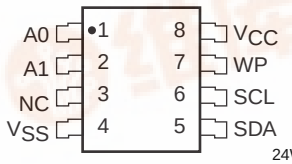
The CAT24WC256 is a 256K-bit Serial CMOS E²PROM internally organized as 32,768 words of 8 bits each. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24WC256 features a 64-byte page write buffer. The device operates via the I²C bus serial interface and is available in 8-pin DIP or 8-pin SOIC packages.

PIN CONFIGURATION

DIP Package (P)



SOIC Package (K)

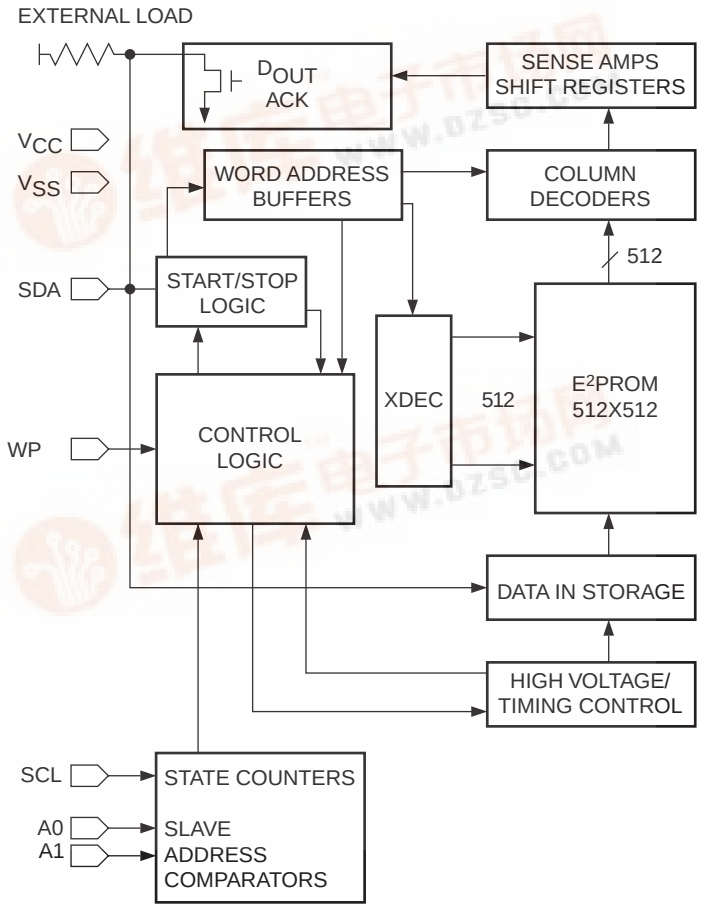


24WC256 F01

PIN FUNCTIONS

Pin Name	Function
A0, A1	Address Inputs
SDA	Serial Data/Address
SCL	Serial Clock
WP	Write Protect
V_{CC}	+1.8V to +6.0V Power Supply
V_{SS}	Ground
NC	No Connect

BLOCK DIAGRAM



24WC256 F02

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –55°C to +125°C

Storage Temperature ..... –65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... –2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N_{END}(3)	Endurance	100,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T_{DR}(3)	Data Retention	100		Years	MIL-STD-883, Test Method 1008
V_{ZAP}(3)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(3)(4)	Latch-up	100		mA	JEDEC Standard 17

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

		Limits				
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
I_{CC1}	Power Supply Current - Read			1	mA	f_{SCL} = 100 KHz V_{CC}=5V
I_{CC2}	Power Supply Current - Write			3	mA	f_{SCL} = 100KHz V_{CC}=5V
I_{SB}(5)	Standby Current			0	µA	V_{IN} = GND or V_{CC} V_{CC}=5V
I_{LI}	Input Leakage Current			1	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	–1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage (V_{CC} = +3.0V)			0.4	V	I_{OL} = 3.0 mA
V_{OL2}	Output Low Voltage (V_{CC} = +1.8V)			0.5	V	I_{OL} = 1.5 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (SCL, WP, A0, A1)	6	pF	V_{IN} = 0V

Note:
(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.
(2) Output shorted for no more than one second. No more than one output shorted at a time.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.
(5) Standby current (I_{SB}) = 0 µA (<900 nA).

A.C. CHARACTERISTICS

V_{CC} = +1.8V to +6V, unless otherwise specified
Output Load is 1 TTL Gate and 100pF

Read & Write Cycle Limits

Symbol	Parameter	V_{CC}=1.8V - 6.0V		V_{CC}=2.5V - 6.0V		V_{CC}=3.0V - 5.5V		
		Min.	Max.	Min.	Max.	Min.	Max.	Units
F_{SCL}	Clock Frequency		100		400		1000	kHz
t_{AA}	SCL Low to SDA Data Out and ACK Out	0.1	3.5	0.05	0.9	0.05	0.55	µs
t_{BUF}(2)	Time the Bus Must be Free Before a New Transmission Can Start	4.7		1.2		0.5		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		0.6		0.25		µs
t_{LOW}	Clock Low Period	4.7		1.2		0.6		µs
t_{HIGH}	Clock High Period	4.0		0.6		0.4		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.0		0.6		0.25		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		ns
$t_{SU:DAT}$	Data In Setup Time	100		100		100		ns
t_R(2)	SDA and SCL Rise Time		1.0		0.3		0.3	µs
t_F(2)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		0.6		0.25		µs
t_{DH}	Data Out Hold Time	100		50		50		ns
t_{WR}	Write Cycle Time		10		10		5	ms

Power-Up Timing (2)(3)

Symbol	Parameter	Max.	Units
t_{PUR}	Power-Up to Read Operation	1	ms
t_{PUW}	Power-Up to Write Operation	1	ms

Note:
(1) AC measurement conditions:
RL (connects to V_{CC}): $0.3V_{CC}$ to $0.7\ V_{CC}$
Input rise and fall times: ≤ 50ns
Input and output timing reference voltages: $0.5\ V_{CC}$
(2) This parameter is tested initially and after a design or process change that affects the parameter.
(3) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

FUNCTIONAL DESCRIPTION

The CAT24WC256 supports the I^2C Bus data transmission protocol. This Inter-Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT24WC256 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

PIN DESCRIPTIONS

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

WP: Write Protect

This input, when tied to GND, allows write operations to the entire memory. When this pin is tied to Vcc, the entire memory is write protected. When left floating, memory is unprotected.

A0, A1: Device Address Inputs

These pins are hardwired or left connected. When hardwired, up to four CAT24WC256's may be addressed on a single bus system. When the pins are left unconnected, the default values are zero.

Figure 1. Bus Timing

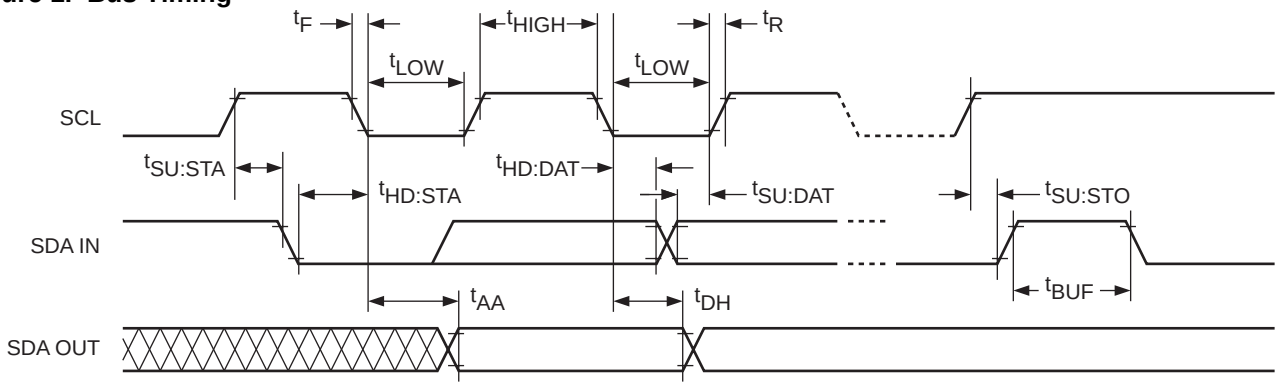


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Figure 2. Write Cycle Timing

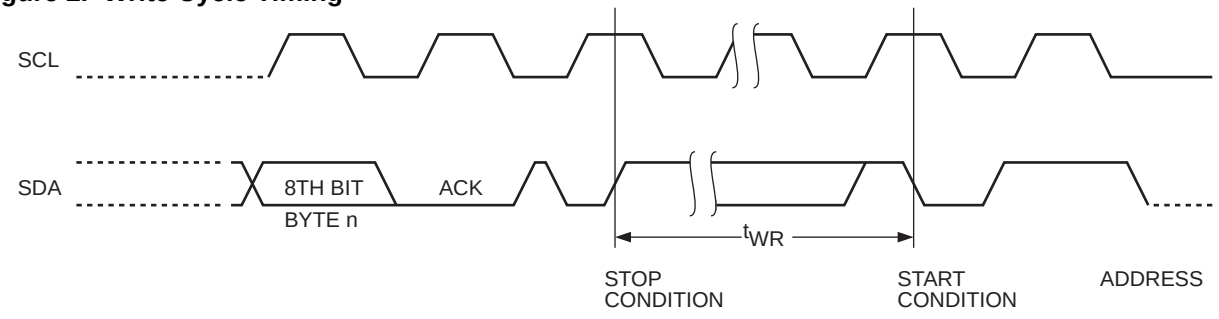

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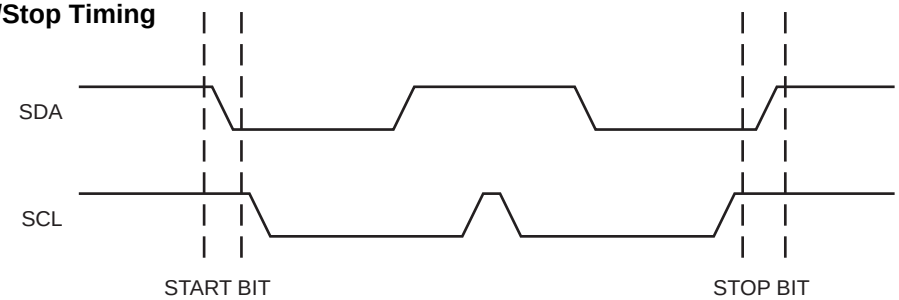
Figure 3. Start/Stop Timing



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I²C BUS PROTOCOL

The features of the I²C bus protocol are defined as follows:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24WC256 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master sends the address of the particular slave device it is requesting. The five most significant bits of the 8-bit slave address are fixed as 10100(Fig. 5). The CAT24WC256 uses the next two bits as address bits. The address bits A1 and A0 allow as many as four devices on the same bus. These bits must compare to their hardwired input pins. The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24WC256 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24WC256 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24WC256 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24WC256 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24WC256 will continue to transmit data. If no acknowledge is sent by the Master, the device

Figure 4. Acknowledge Timing

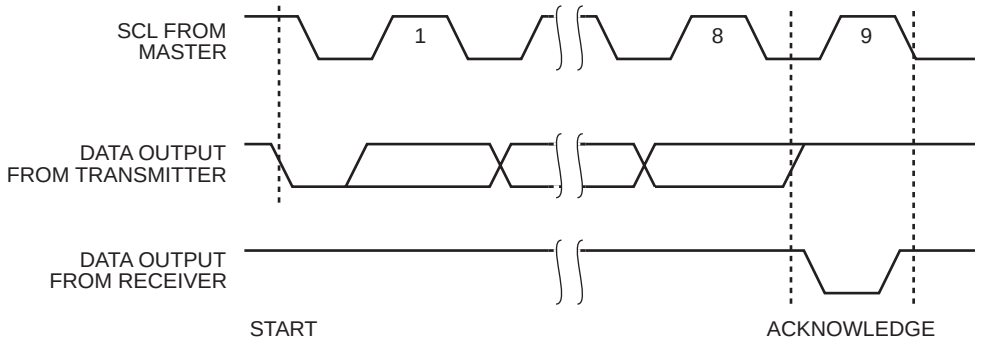

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Figure 5. Slave Address Bits

1	0	1	0	0	A1	A0	R/$\overline{W}$

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terminates data transmission and waits for a STOP condition.

WRITE OPERATIONS

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two 8-bit address words that are to be written into the address pointers of the CAT24WC256. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the addressed memory location. The CAT24WC256 acknowledges once more and the Master generates the STOP condition. At this time, the device begins an internal programming cycle to nonvolatile memory. While the cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24WC256 writes up to 64 bytes of data, in a single write cycle, using the Page Write operation. The page write operation is initiated in the same manner as the byte write operation, however instead of terminating after the initial byte is transmitted, the Master is allowed to send up to 63 additional bytes. After each byte has been transmitted, CAT24WC256 will respond with an acknowledge, and internally increment the six low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than 64 bytes before sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

When all 64 bytes are received, and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the CAT24WC256 in a single write cycle.

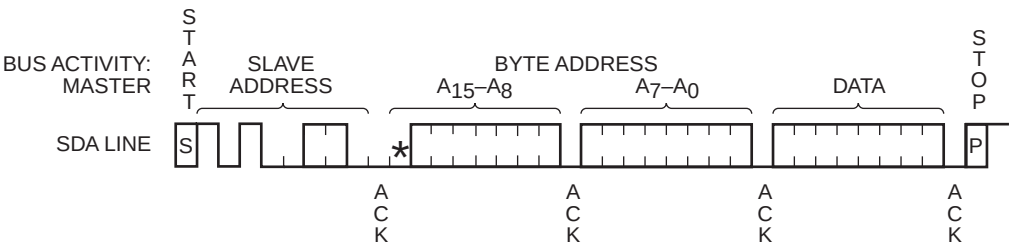
Acknowledge Polling

Disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, CAT24WC256 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If CAT24WC256 is still busy with the write operation, no ACK will be returned. If CAT24WC256 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the memory array. If the WP pin is tied to V_{CC}, the entire memory array is protected and becomes read only. The CAT24WC256 will accept both slave and byte addresses, but the memory location accessed is protected from programming by the device's failure to send an acknowledge after the first byte of data is received.

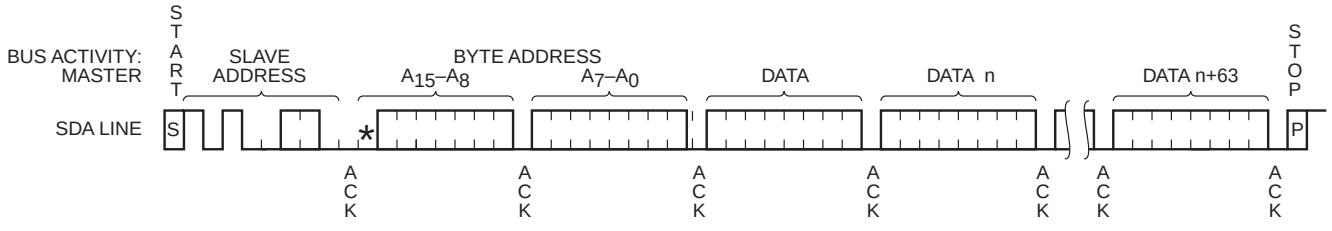
Figure 6. Byte Write Timing



*=Don't Care Bit

24WC256 F08

Figure 7. Page Write Timing



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READ OPERATIONS

The READ operation for the CAT24WC256 is initiated in the same manner as the write operation with one exception, that R/$\overline{W}$ bit is set to one. Three different READ operations are possible: Immediate/Current Address READ, Selective/Random READ and Sequential READ.

Immediate/Current Address Read

The CAT24WC256's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=E (where E=32767), then the counter will 'wrap around' to address 0 and continue to clock out data. After the CAT24WC256 receives its slave address information (with the R/$\overline{W}$ bit set to one), it issues an acknowledge, then transmits the 8 bit byte requested. The master device does not send an acknowledge, but will generate a STOP condition.

Selective/Random Read

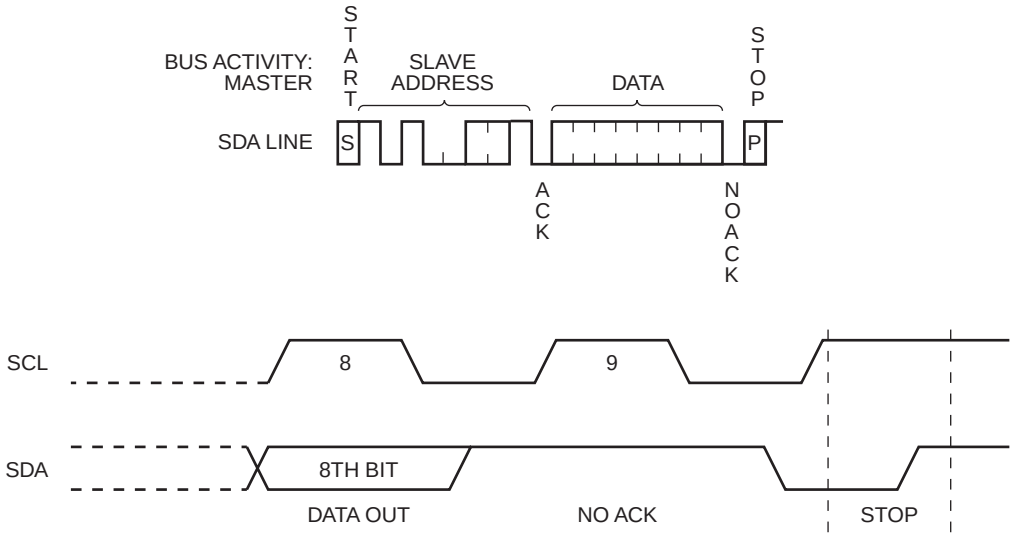
Selective/Random READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte addresses of the location it wishes to read. After CAT24WC256 acknowledges, the Master device sends the START condition and the slave address again, this time with the R/$\overline{W}$ bit set to one. The CAT24WC256 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the Immediate Address READ or Selective READ operations. After the CAT24WC256 sends the initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24WC256 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation will terminate when the Master fails to respond with an acknowledge, thus sending the STOP condition.

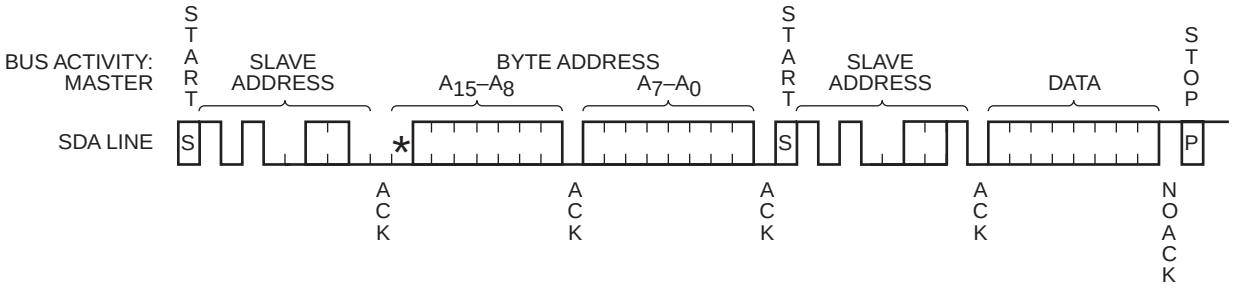
The data being transmitted from CAT24WC256 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24WC256 address bits so that the entire memory array can be read during one operation. If more than E (where E=32767) bytes are read out, the counter will 'wrap around' and continue to clock out data bytes.

Figure 8. Immediate Address Read Timing



24WC256 F10

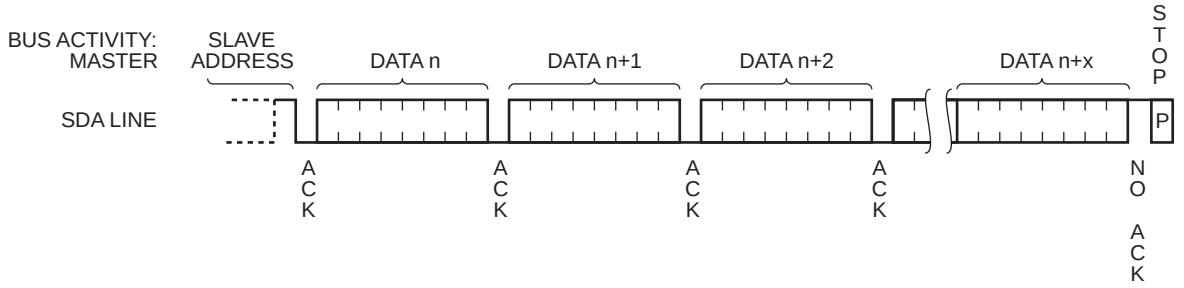
Figure 9. Selective Read Timing



*=Don't Care Bit

24WC256 FIG. 11

Figure 10. Sequential Read Timing



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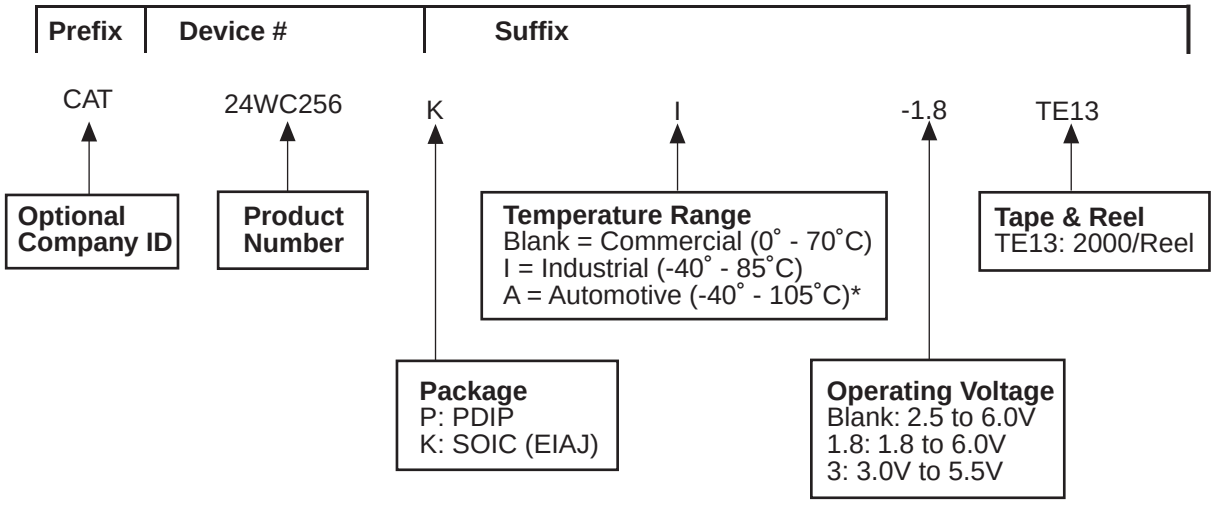
ORDERING INFORMATION



* -40˚ to +125˚C is available upon request

24WC256 FIG. 13

Notes:
(1) The device used in the above example is a 24WC256KI-1.8TE13 (SOIC, Industrial Temperature, 1.8 Volt to 6 Volt Operating Voltage, Tape & Reel)