

# LIFO/FIFO Buffer Register

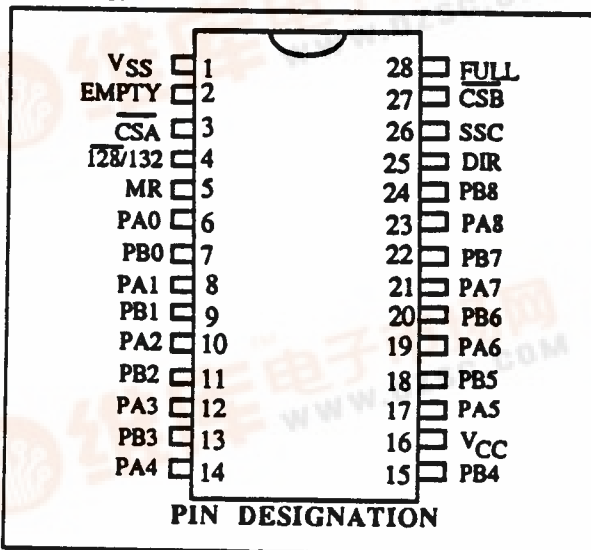
# WD1510-00,-01,-02

## FEATURES

- Word length selectable: 128 or 132
- 9 bit word width
- DC to 650 KHz (-00), 1 MHz (-01), 1.5 MHz (-02)
- Empty and full flags
- Three-state data lines
- 5-volt only
- No external clocks required
- TTL compatible on all inputs and outputs
- 28 pin plastic or ceramic dip
- Cascadable with WD1511 support chip
- Fully asynchronous dual port operation

## DESCRIPTION

The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.



## OPERATION

The WD1510 contains a 132 x 9 buffer which may be programmed for 128 x 9 operation. Setting the 128/132 pin to a Logic 0, enables the EMPTY and FULL lines to be activated when 128 bytes are read or written. When the 128/132 line is set to a Logic 1 or left open, the 132 byte operation is enabled. This line contains an internal pull-up resistor of approximately 5KΩ.

When the Master Reset Line (pin 5) is set to a Logic 1, all internal counters are reset and the EMPTY Flag is set. Prior to reading or writing data, the DIRECTION Line (pin 25) must be set to select the desired operation:

DIR	PORT A	PORT B
1	WRITE	READ
0	READ	WRITE

To operate the device in the FIFO mode, both Ports must be used. If the DIRECTION Line is set to a logic 1, then data is written into Port A and read out of Port B. Reading/Writing to the two ports can be done asynchronously.

In the LIFO mode only one port is used. For example, if using Port A, the DIRECTION Line is set to a Logic 1 to enter data, and is reset to a Logic 0 to read data.

Reading or writing is performed by setting the appropriate CS (Chip Select) Line to a Logic 0. After the specified hold time has expired, data may be entered or read on the rising edge of CSA or CSB. In a Read mode, data is valid as long a CS remains active. Both Ports return to the high impedance state when CS is returned to a Logic 1.

The EMPTY Line (Pin 2) and the FULL Line (Pin 28) are used as status or interrupt lines to determine the status of the buffer. When both EMPTY and FULL are at a Logic 0, the buffer contains 1 thru 127 bytes (128/132 = 0) or 1 thru 132 bytes (128/132 = 1).

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## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

$V_{CC}$  with respect to  $V_{SS}$  (Ground) .....+7V  
 Max Voltage on any Pin with respect to  $V_{SS}$  .....-0.5V to +7V  
 Operating Temperature ..... 0°C to 70°C

### Storage Temperature

Plastic .....- 55° C to + 125° C  
 Ceramic .....- 65° C to + 150° C

### OPERATING CHARACTERISTICS (DC)

$T_A = 0^\circ\text{C TO } 70^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{CC} = +5\text{V} \pm 2.5\text{V}$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$I_{LI}$	Input Leakage			10	$\mu\text{A}$	$V_{IN} = V_{CC}$
$I_{LO}$	Output Leakage			10	$\mu\text{A}$	$V_{OUT} = V_{CC}, V_{SS}$
$V_{IH}$	Input High Voltage	2.2			V	
$V_{IL}$	Input Low Voltage			0.8	V	
$V_{OH}$	Output High Voltage	2.4			V	$I_O = -100 \mu\text{A}$
$V_{OL}$	Output Low Voltage			.4	V	$I_O = 1.6\text{mA}$
$I_{CC}$	Power Supply Current		125	200	mA	All outputs open

## A.C. TIMING CHARACTERISTICS

$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{SS} = 0\text{V}$ ,  $V_{CC} = +5\text{V} \pm 2.5\text{V}$ ,  $V_{OH} = 2.0\text{V}$ ,  $V_{OL} = 0.8\text{V}$ .

SYMBOL	CHARACTERISTICS	WD1510-00*		WD1510-01*		WD1510-02*	
		MIN	MAX	MIN	MAX	MIN	MAX
$T_{MR}$	Master Reset Time	400		250		250	
$T_{DV}$	Data Valid from CS		550		350		300
$T_{DD}$	Data Delay from CS		110		85		60
$T_{DH}$	Data Hold from CS	150		100		80	
$T_{DIR}$	DIR Setup Time	1500		1000		834	
$T_{EV}$	EMPTY Valid from CS		550		350		250
$T_{FV}$	FULL Valid from CS		550		350		250
$T_{CSL}$	CS Pulse Width Low	600		500		417	
$T_{CSH}$	CS Pulse Width High	600		500		417	
$T_{CY}$	CS Cycle Time	1540		1000		834	
$T_{DS}$	Data Setup Time	80		50		50	
$F_{MAX}$	Data Transfer Rate		.65		1.0		1.5

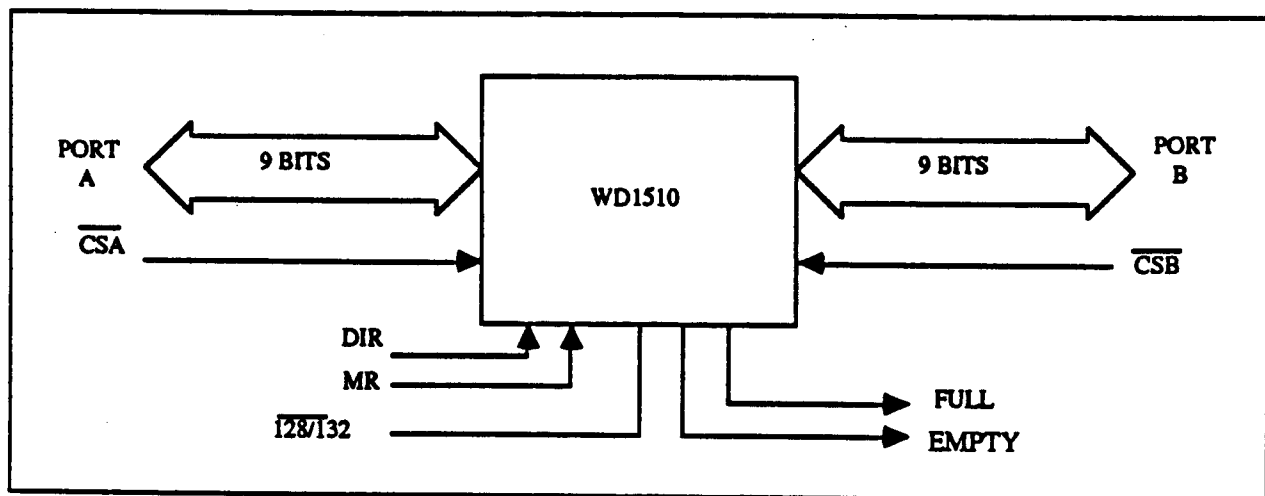
\*All values are in nanoseconds with the exception of  $F_{MAX}$ -MHz.

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# LIFO/FIFO Buffer Register

## PIN DESCRIPTION

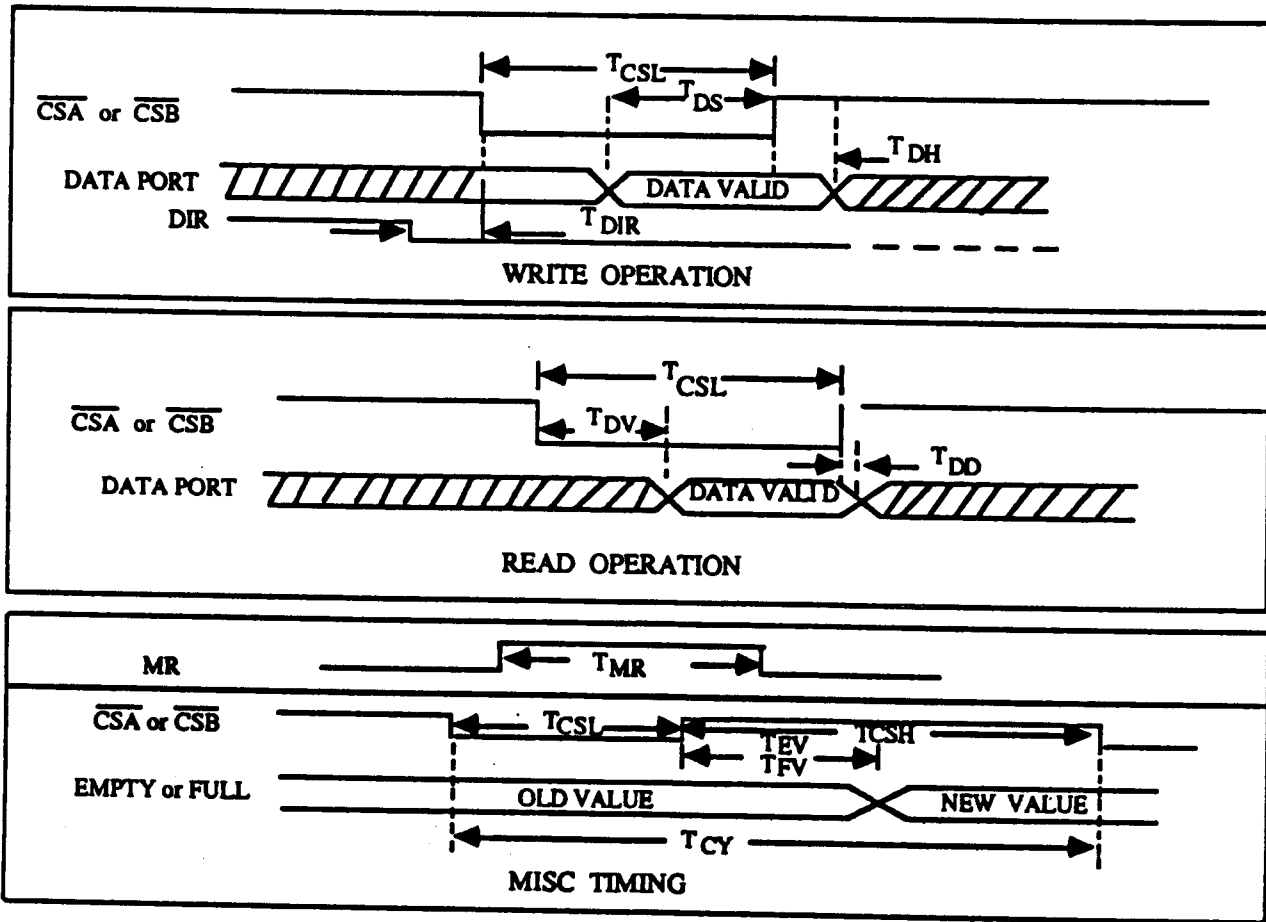
PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	$\overline{\text{CSA}}$	Used to select Port A for either a Read or Write operation
4	128 OR 132	$\overline{\text{128/132}}$	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14,17,19,21,23	PORT A DATA LINES	PA0-BA8	Bidirectional DATA Port for reading or writing
7,9,11,13,15,18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing
16	V <sub>CC</sub>	V <sub>CC</sub>	+5 volts $\pm$ .25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from.
26	NO CONNECTION	NC	No connection (not for customer use).
27	CHIP SELECT PORT B	$\overline{\text{CSB}}$	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data



BLOCK DIAGRAM

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# LIFO/FIFO Buffer Register



**CAPACITANCE**  
 $T_A = 25^\circ\text{C}$ ;  $V_{CC} = \text{GND} = 0\text{V}$

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$C_{IN}$	Input Capacitance		6	10	pF	$f_C = 1\text{ MHz}$ Unmeasured pins returned to GND. $V_{CC} = 5.0\text{V}$
$C_{I/O}$	I/O Capacitance		15	20	pF	
$C_L$	Load Capacitance		50		pF	

## WD1510 CAPACITANCE LEVELS

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