

DATA SHEET

74LV109

Dual JK flip-flop with set and reset;
positive-edge trigger

Product specification
Supersedes data of 1997 Jun 06
IC24 Data Handbook

1998 Apr 20

Dual JK flip-flop with set and reset; positive-edge trigger

74LV109

FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between $V_{CC} = 2.7$ V and $V_{CC} = 3.6$ V
- Typical V_{OLP} (output ground bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^\circ\text{C}$
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at $V_{CC} = 3.3$ V, $T_{amb} = 25^\circ\text{C}$
- Output capability: standard
- I_{CC} category: flip-flops

DESCRIPTION

The 74LV109 is a low-voltage Si-gate CMOS device that is pin and function compatible with 74HC/HCT109.

The 74LV109 is a dual positive-edge triggered JK-type flip-flop featuring individual J, K inputs, clock (CP) inputs, set (\bar{S}_D) and reset (\bar{R}_D) inputs; also complementary Q and \bar{Q} outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The JK design allows operation as a D-type flip-flop by tying the J and K inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

QUICK REFERENCE DATA

$GND = 0$ V; $T_{amb} = 25^\circ\text{C}$; $t_r = t_f \leq 2.5$ ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|--------------------------------------|----------------|------|
| t_{PHL}/t_{PLH} | Propagation delay nCP to nQ, n \bar{Q} n \bar{S}_D to nQ, n \bar{Q} n \bar{R}_D to nQ, n \bar{Q} | $C_L = 15$ pF; $V_{CC} = 3.3$ V | 14 12 12 | ns |
| | f_{max} | | 77 | MHz |
| C_I | Input capacitance | | 3.5 | pF |
| C_{PD} | Power dissipation capacitance per flip-flop | $V_I = GND$ to V_{CC} ¹ | 20 | pF |

NOTE:

- CPD is used to determine the dynamic power dissipation (P_D in μW)

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; C_L = output load capacitance in pF;

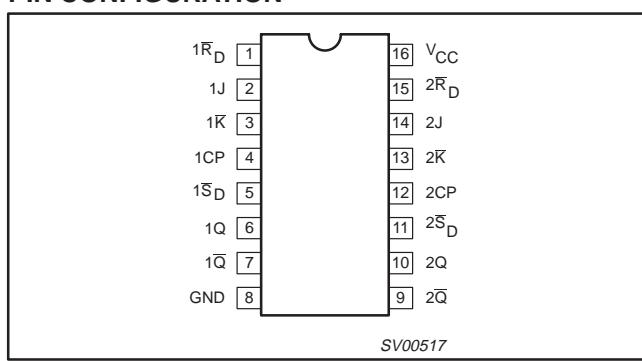
f_o = output frequency in MHz; V_{CC} = supply voltage in V;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|-----------------------------|-------------------|-----------------------|---------------|-------------|
| 16-Pin Plastic DIL | -40°C to +125°C | 74LV109 N | 74LV109 N | SOT38-4 |
| 16-Pin Plastic SO | -40°C to +125°C | 74LV109 D | 74LV109 D | SOT109-1 |
| 16-Pin Plastic SSOP Type II | -40°C to +125°C | 74LV109 DB | 74LV109 DB | SOT338-1 |
| 16-Pin Plastic TSSOP Type I | -40°C to +125°C | 74LV109 PW | 74LV109PW DH | SOT403-1 |

PIN CONFIGURATION



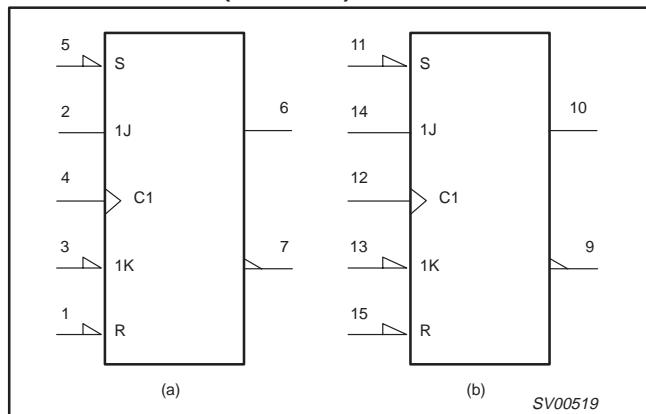
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|--------------|-----------------------------------|---|
| 1, 15 | 1R _D , 2R _D | Asynchronous reset input (active LOW) |
| 2, 14, 3, 13 | 1J, 2J, 1K, 2K | Synchronous inputs; flip-flops 1 and 2 |
| 4, 12 | 1CP, 2CP | Clock input (LOW-to-HIGH, edge-triggered) |
| 5, 11 | 1SD, 2SD | Asynchronous set inputs (active LOW) |
| 6, 10 | 1Q, 2Q | True flip-flop outputs |
| 7, 9 | 1Q-bar, 2Q-bar | Complement flip-flop outputs |
| 8 | GND | Ground (0 V) |
| 16 | V _{CC} | Positive supply voltage |

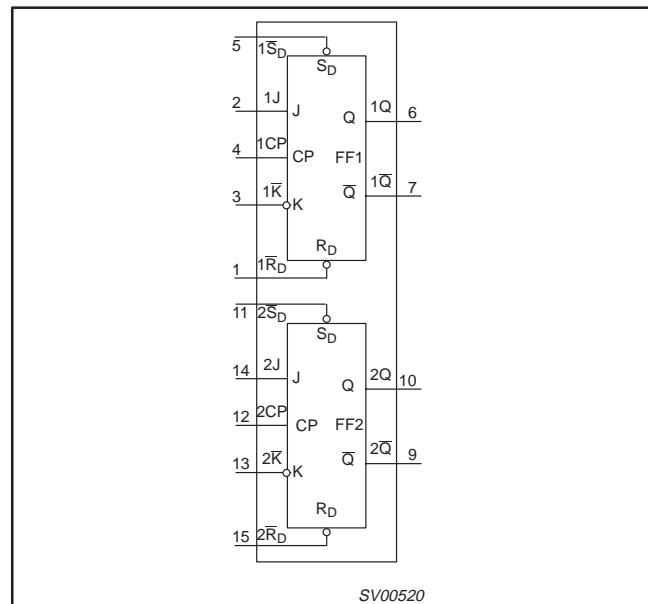
Dual JK flip-flop with set and reset; positive-edge trigger

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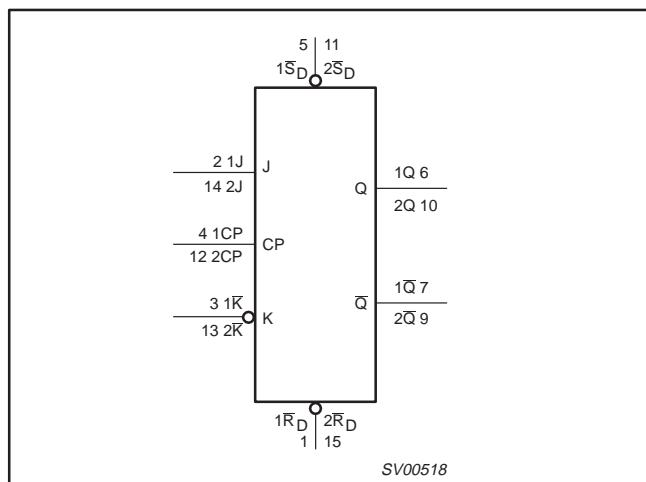
LOGIC SYMBOL (IEEE/IEC)



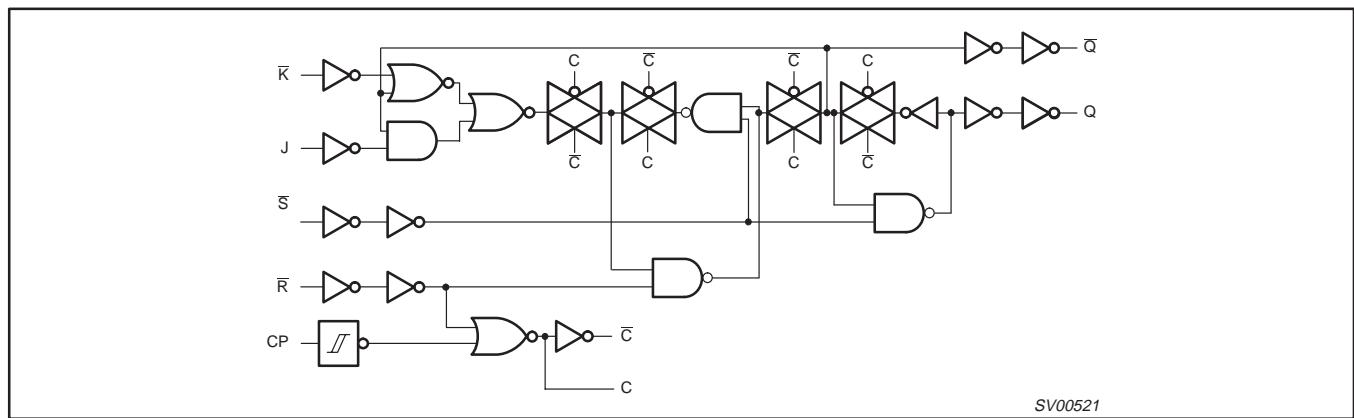
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



LOGIC DIAGRAM



Dual JK flip-flop with set and reset; positive-edge trigger

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FUNCTION TABLE

| OPERATING MODES | INPUTS | | | | | OUTPUTS | |
|--------------------|-----------------|-----------------|-----|----|----|---------|-----|
| | nS _D | nR _D | nCP | nJ | nK | nQ | nQ̄ |
| Asynchronous set | L | H | X | X | X | H | L |
| Asynchronous reset | H | L | X | X | X | L | H |
| Undetermined | L | L | X | X | X | H | H |
| Toggle | H | H | ↑ | h | I | q̄ | q |
| Load "0" (reset) | H | H | ↑ | I | I | L | H |
| Load "1" (set) | H | H | ↑ | h | h | H | L |
| Hold "no change" | H | H | ↑ | I | h | q | q̄ |

NOTES:

H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition

L = LOW voltage level

I = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition

q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition.

X = don't care

↑ = LOW-to-HIGH CP transition

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | TYP. | MAX | UNIT |
|---------------------------------|---|--|-------------|-------------|-------------------|------|
| V _{CC} | DC supply voltage | See Note 1 | 1.0 | 3.3 | 3.6 | V |
| V _I | Input voltage | | 0 | — | V _{CC} | V |
| V _O | Output voltage | | 0 | — | V _{CC} | V |
| T _{amb} | Operating ambient temperature range in free air | See DC and AC characteristics | -40 -40 | | +85 +125 | °C |
| t _r , t _f | Input rise and fall times except for Schmitt-trigger inputs | V _{CC} = 1.0V to 2.0V V _{CC} = 2.0V to 2.7V V _{CC} = 2.7V to 3.6V | — — — | — — — | 500 200 100 | ns/V |

NOTE:

1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 3.6V.ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0V).

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|--|-------------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +4.6 | V |
| ±I _{IK} | DC input diode current | V _I < -0.5 or V _I > V _{CC} + 0.5V | 20 | mA |
| ±I _{OK} | DC output diode current | V _O < -0.5 or V _O > V _{CC} + 0.5V | 50 | mA |
| ±I _O | DC output source or sink current — standard outputs | -0.5V < V _O < V _{CC} + 0.5V | 25 | mA |
| ±I _{GND} , ±I _{CC} | DC V _{CC} or GND current for types with — standard outputs | | 50 | mA |
| T _{stg} | Storage temperature range | | -65 to +150 | °C |
| P _{TOT} | Power dissipation per package — plastic DIL — plastic mini-pack (SO) — plastic shrink mini-pack (SSOP and TSSOP) | for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K | 750 500 400 | mW |

NOTE:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | | | UNIT | |
|------------------|---|--|----------------|------------------|------|-----------------|------|------|--|
| | | | -40°C to +85°C | | | -40°C to +125°C | | | |
| | | | MIN | TYP ¹ | MAX | MIN | MAX | | |
| V _{IH} | HIGH level Input voltage | V _{CC} = 1.2 V | 0.9 | | | 0.9 | | V | |
| | | V _{CC} = 2.0 V | 1.4 | | | 1.4 | | | |
| | | V _{CC} = 2.7 to 3.6 V | 2.0 | | | 2.0 | | | |
| V _{IL} | LOW level Input voltage | V _{CC} = 1.2 V | | | 0.3 | | 0.3 | V | |
| | | V _{CC} = 2.0 V | | | 0.6 | | 0.6 | | |
| | | V _{CC} = 2.7 to 3.6 V | | | 0.8 | | 0.8 | | |
| V _{OH} | HIGH level output voltage; all outputs | V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA | | 1.2 | | | | V | |
| | | V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA | 1.8 | 2.0 | | 1.8 | | | |
| | | V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA | 2.5 | 2.7 | | 2.5 | | | |
| | | V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; -I _O = 100µA | 2.8 | 3.0 | | 2.8 | | | |
| V _{OH} | HIGH level output voltage; STANDARD outputs | V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; -I _O = 6mA | 2.40 | 2.82 | | 2.20 | | V | |
| V _{OL} | LOW level output voltage; all outputs | V _{CC} = 1.2 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA | | 0 | | | | V | |
| | | V _{CC} = 2.0 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA | | 0 | 0.2 | | 0.2 | | |
| | | V _{CC} = 2.7 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA | | 0 | 0.2 | | 0.2 | | |
| | | V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = 100µA | | 0 | 0.2 | | 0.2 | | |
| V _{OL} | LOW level output voltage; STANDARD outputs | V _{CC} = 3.0 V; V _I = V _{IH} or V _{IL} ; I _O = 6mA | | 0.25 | 0.40 | | 0.50 | V | |
| I _I | Input leakage current | V _{CC} = 3.6 V; V _I = V _{CC} or GND | | | 1.0 | | 1.0 | µA | |
| I _{CC} | Quiescent supply current; flip-flops | V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0 | | | 20.0 | | 80 | µA | |
| ΔI _{CC} | Additional quiescent supply current per input | V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V | | | 500 | | 850 | µA | |

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

AC CHARACTERISTICS

GND = 0V; t_f = t_f ≤ 2.5ns; C_L = 50pF; R_L = 1kΩ

| SYMBOL | PARAMETER | WAVEFORM | CONDITION | LIMITS | | | | | UNIT |
|------------------------------------|--|----------|---------------------|---------------|------------------|-----|----------------|-----|------|
| | | | | -40 to +85 °C | | | -40 to +125 °C | | |
| | | | V _{CC} (V) | MIN | TYP ¹ | MAX | MIN | MAX | |
| t _{PHL} /t _{PLH} | Propagation delay nCP to nQ, n \bar{Q} | Figure 1 | 1.2 | | 90 | | | | ns |
| | | | 2.0 | | 31 | 58 | | 70 | |
| | | | 2.7 | | 23 | 43 | | 51 | |
| | | | 3.0 to 3.6 | | 18 ² | 34 | | 41 | |
| t _{PLH} | Propagation delay n \bar{S}_D to nQ | Figure 2 | 1.2 | | 55 | | | | ns |
| | | | 2.0 | | 19 | 36 | | 44 | |
| | | | 2.7 | | 14 | 26 | | 33 | |
| | | | 3.0 to 3.6 | | 10 ² | 21 | | 26 | |

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AC CHARACTERISTICS (Continued)

GND = 0V; $t_r = t_f \leq 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 1\text{K}\Omega$

| SYMBOL | PARAMETER | WAVEFORM | CONDITION | LIMITS | | | | | UNIT |
|-----------|---|----------|--------------------|-----------------|------------------|-----|----------------|-----|------|
| | | | | -40 to +85 °C | | | -40 to +125 °C | | |
| | | | $V_{CC}(\text{V})$ | MIN | TYP ¹ | MAX | MIN | MAX | |
| t_{PHL} | Propagation delay $n\bar{S}_D$ to $n\bar{Q}$ | Figure 2 | 1.2 | 75 | | | | | ns |
| | | | 2.0 | 26 | 46 | | | 60 | |
| | | | 2.7 | 19 | 36 | | | 44 | |
| | | | 3.0 to 3.6 | 17 ² | 29 | | | 35 | |
| t_{PLH} | Propagation delay $n\bar{R}_D$ to nQ | Figure 2 | 1.2 | 75 | | | | | ns |
| | | | 2.0 | 26 | 46 | | | 60 | |
| | | | 2.7 | 19 | 36 | | | 44 | |
| | | | 3.0 to 3.6 | 15 ² | 29 | | | 35 | |
| t_W | Clock pulse width HIGH or LOW | Figure 1 | 1.2 | 70 | | | | | ns |
| | | | 2.0 | 24 | 44 | | | 54 | |
| | | | 2.7 | 18 | 33 | | | 40 | |
| | | | 3.0 to 3.6 | 13 ² | 26 | | | 32 | |
| t_W | Set or reset pulse width HIGH or LOW | Figure 2 | 2.0 | 34 | 12 | | 41 | | ns |
| | | | 2.7 | 25 | 9 | | 30 | | |
| | | | 3.0 to 3.6 | 20 | 7 ² | | 24 | | |
| t_{rem} | Removal time $n\bar{S}_D, n\bar{R}_D$ to nCP | Figure 2 | 2.0 | 34 | 9 | | 41 | | ns |
| | | | 2.7 | 25 | 6 | | 30 | | |
| | | | 3.0 to 3.6 | 20 | 5 ² | | 24 | | |
| | | | 1.2 | 35 | | | | | |
| t_{su} | Set-up time $nJ, n\bar{K}$ to CP | Figure 1 | 2.0 | 24 | 12 | | 29 | | ns |
| | | | 2.7 | 18 | 9 | | 21 | | |
| | | | 3.0 to 3.6 | 14 | 7 ² | | 17 | | |
| | | | 1.2 | 30 | | | | | |
| t_h | Hold time $nJ, n\bar{K}$ to nCP | Figure 1 | 2.0 | 22 | 10 | | 26 | | ns |
| | | | 2.7 | 16 | 8 | | 19 | | |
| | | | 3.0 to 3.6 | 13 | 6 ² | | 15 | | |
| | | | 1.2 | -5 | | | | | |
| f_{max} | Maximum clock pulse frequency | Figure 1 | 2.0 | 5 | -2 | | 5 | | MHz |
| | | | 2.7 | 5 | -1 | | 5 | | |
| | | | 3.0 to 3.6 | 5 | 0 ² | | 5 | | |
| | | | 2.0 | 14 | 40 | | 12 | | |
| | | | 2.7 | 19 | 58 | | 16 | | |
| | | | 3.0 to 3.6 | 24 | 70 ² | | 20 | | |

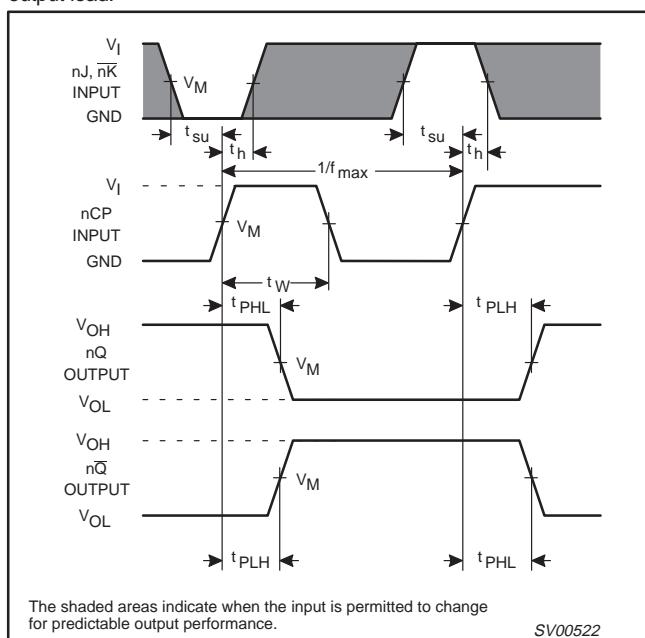
NOTES:

1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25^\circ\text{C}$
2. Typical values are measured at $V_{CC} = 3.3\text{ V}$.

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AC WAVEFORMS

 $V_M = 1.5 \text{ V}$ at $V_{CC} \geq 2.7 \text{ V}$; $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$; V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

SV00522

Figure 1. Clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ and nK to nCP set-up, the nCP to nJ, nK hold times and the maximum clock pulse frequency.

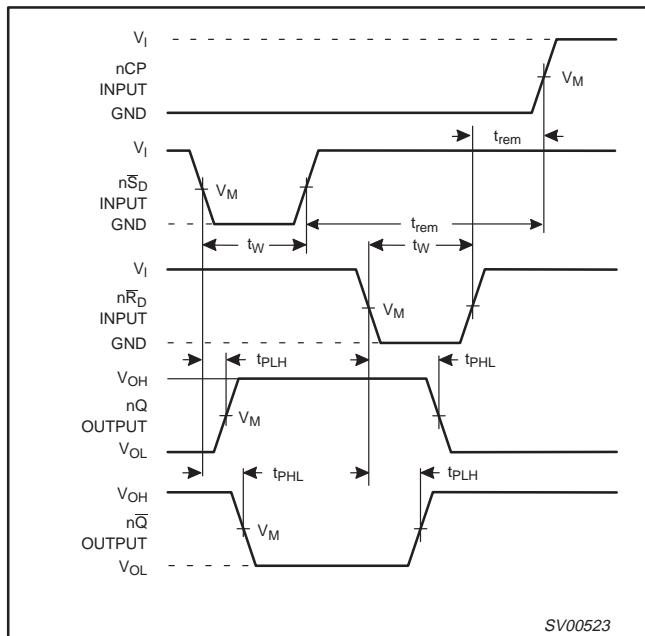
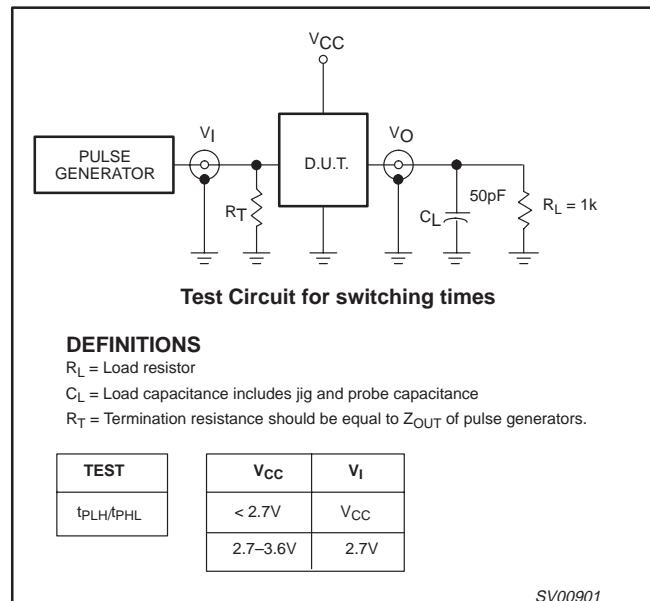


Figure 2. Set (nSD) and reset (nRD) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nRD, nSD to nCP removal time.

TEST CIRCUIT



Test Circuit for switching times

DEFINITIONS

 R_L = Load resistor C_L = Load capacitance includes jig and probe capacitance R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| TEST | |
|------------------|--|
| $t_{PLH}t_{PHL}$ | |

| V_{CC} | V_I |
|----------|----------|
| < 2.7V | V_{CC} |
| 2.7–3.6V | 2.7V |

SV00901

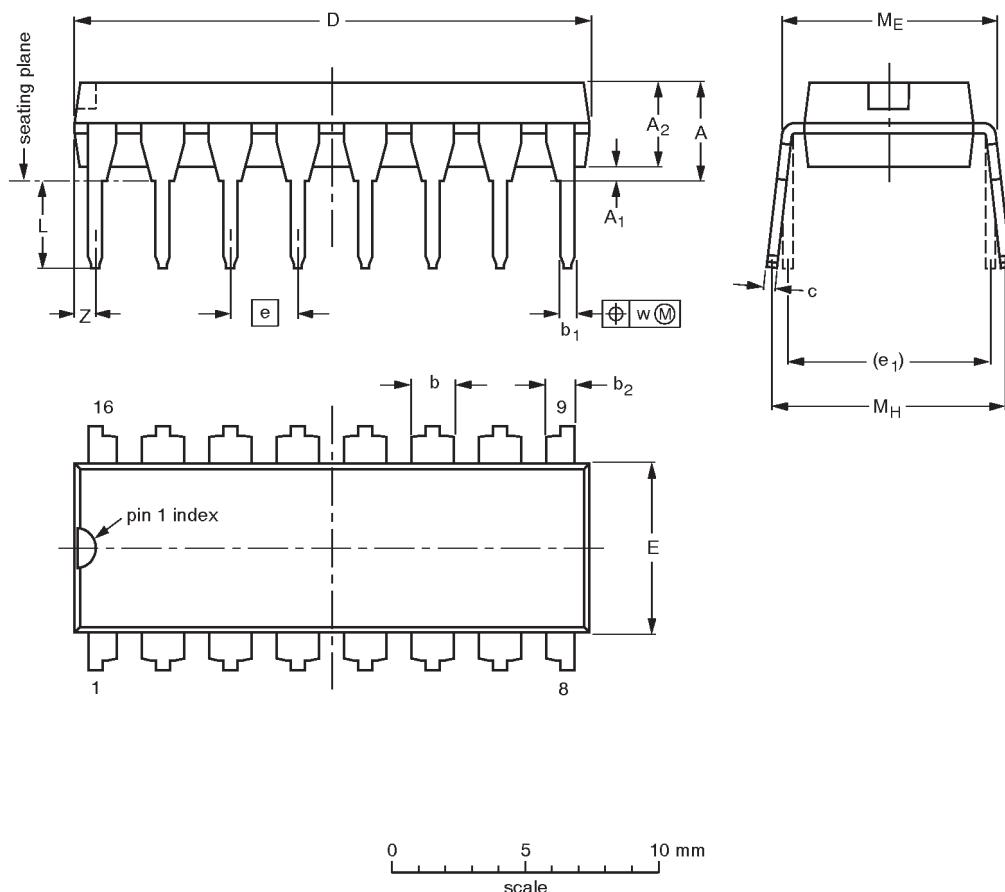
Figure 3. Load circuitry for switching times.

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ min. | A ₂ max. | b | b ₁ | b ₂ | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | L | M _E | M _H | w | Z ⁽¹⁾ max. |
|--------|-----------|------------------------|------------------------|----------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|-------|--------------------------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.30 | 0.53 0.38 | 1.25 0.85 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.020 | 0.13 | 0.068 0.051 | 0.021 0.015 | 0.049 0.033 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.10 | 0.30 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.030 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

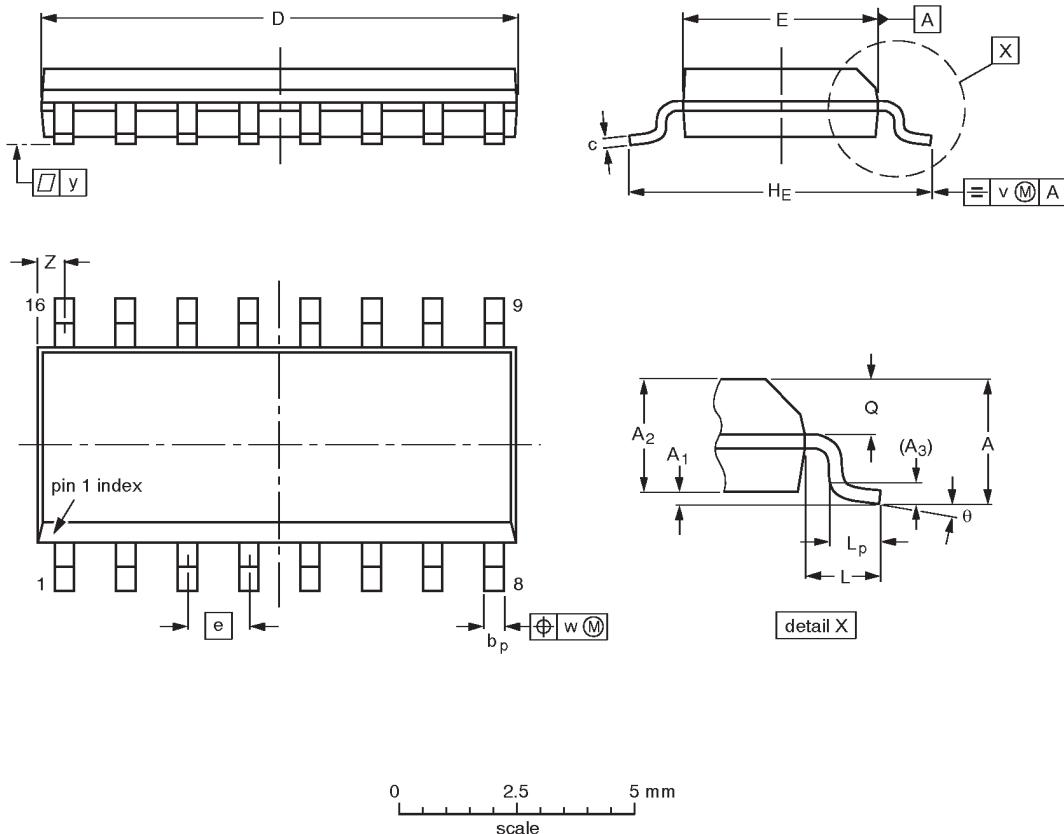
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|-------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT38-4 | | | | | | 92-11-17 95-01-14 |

Dual JK flip-flop with set and reset; positive-edge trigger

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|--------|-----------|------------------|----------------|----------------|----------------|------------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 10.0 9.8 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.0098 0.0039 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0098 0.0075 | 0.39 0.38 | 0.16 0.15 | 0.050 | 0.24 0.23 | 0.041 | 0.039 0.016 | 0.028 0.020 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

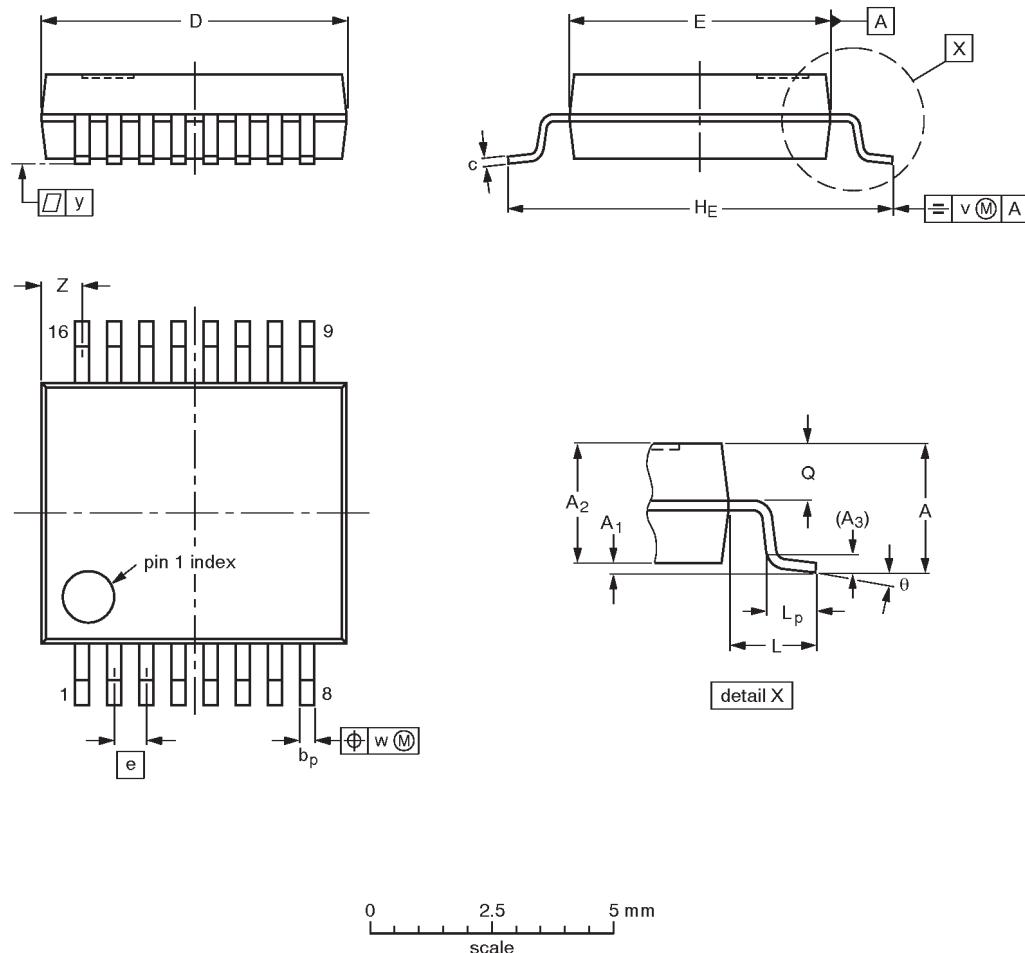
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|----------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT109-1 | 076E07S | MS-012AC | | | | 91-08-13 95-01-23 |

Dual JK flip-flop with set and reset; positive-edge trigger

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SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | z ⁽¹⁾ | θ |
|------|-------------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 0.05 | 0.21 1.65 | 1.80 | 0.25 | 0.38 0.25 | 0.20 0.09 | 6.4 6.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 1.00 0.55 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

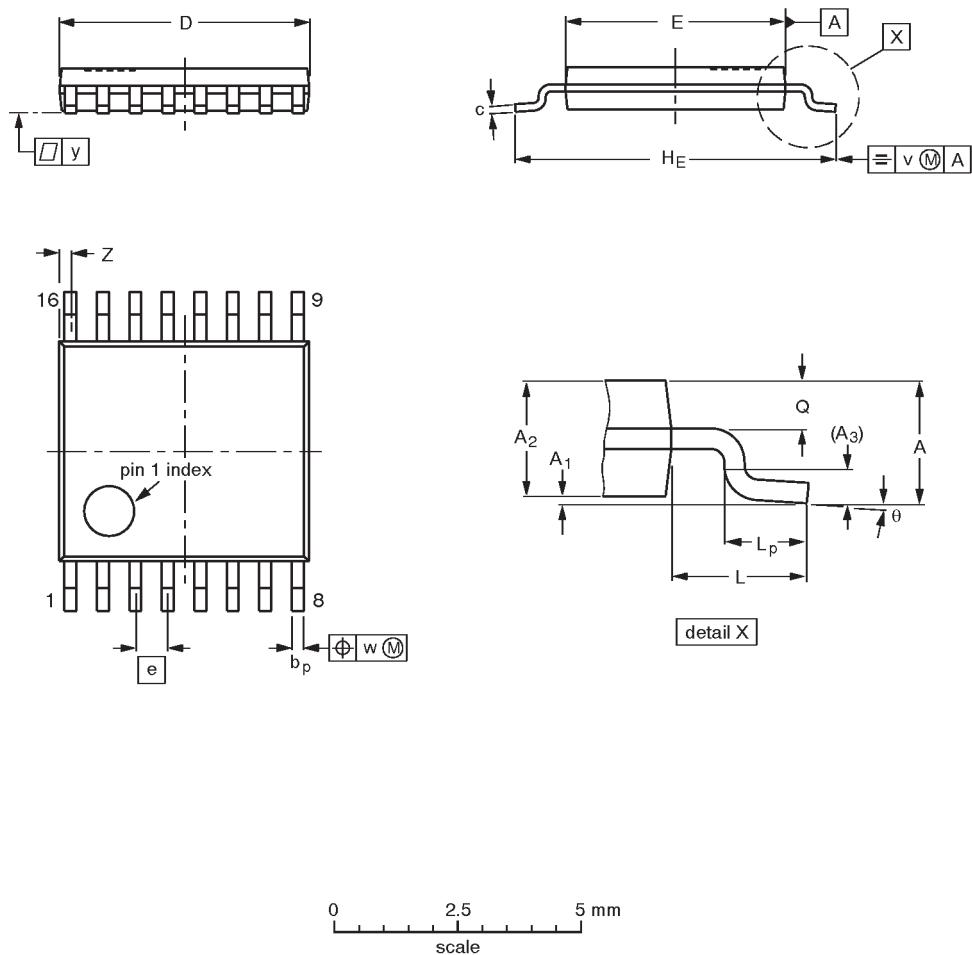
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|----------|------|--|------------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT338-1 | | MO-150AC | | | | 94-01-14 95-02-04 |

Dual JK flip-flop with set and reset; positive-edge trigger

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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.10 0.05 | 0.15 0.80 | 0.95 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.40 0.06 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | EUROPEAN PROJECTION | ISSUE DATE |
|--------------------|------------|--------|------|------------------------|-----------------------|
| | IEC | JEDEC | EIAJ | | |
| SOT403-1 | | MO-153 | | | -94-07-12 95-04-04 |

Dual JK flip-flop with set and reset; positive-edge trigger

74LV109

DEFINITIONS

| Data Sheet Identification | Product Status | Definition |
|----------------------------------|------------------------|--|
| <i>Objective Specification</i> | Formative or in Design | This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice. |
| <i>Preliminary Specification</i> | Preproduction Product | This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product. |
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