

# DATA SHEET

**74LVT240**

**ABT octal inverting buffer (3-State)**

Product specification  
Supersedes data of 1994 May 16  
IC23 Data Handbook

1998 Feb 19

## 3.3V Octal inverting buffer (3-State)

## 74LVT240

### FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Power-up 3-State
- Live insertion/extraction permitted
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model.

### DESCRIPTION

The LVT240 is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V.

This device is an octal inverting buffer that is ideal for driving bus lines. The device features two Output Enables ( $1\overline{OE}$ ,  $2\overline{OE}$ ), each controlling four of the 3-State outputs.

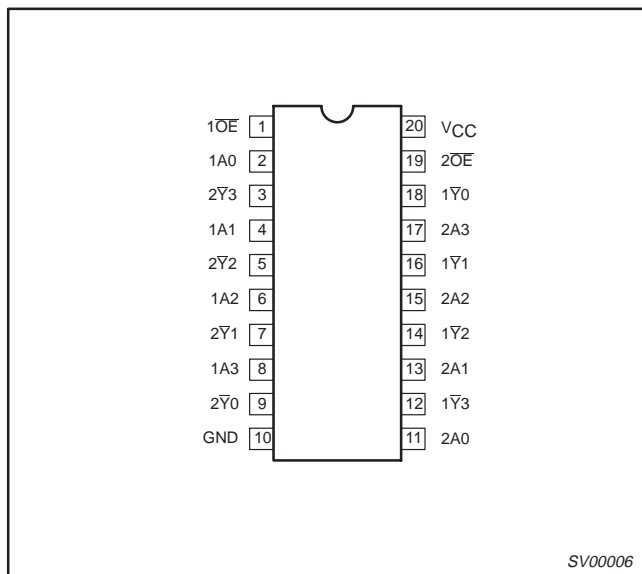
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$ ; $\text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nAx to nYx	$C_L = 50\text{pF}$ ; $V_{CC} = 3.3\text{V}$	2.5 2.6	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V}$ or $3.0\text{V}$	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V}$ or $3.0\text{V}$	8	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6\text{V}$	0.12	mA

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic SOL	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT240 D	74LVT240 D	SOT163-1
20-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT240 DB	74LVT240 DB	SOT339-1
20-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	74LVT240 PW	74LVT240PW DH	SOT360-1

### PIN CONFIGURATION



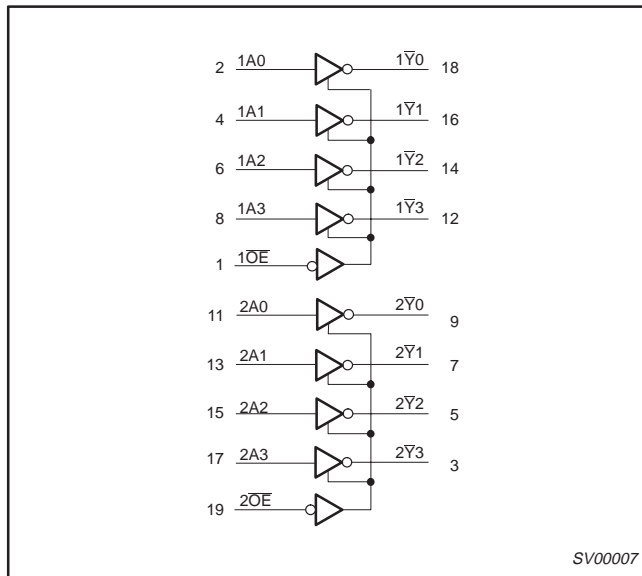
### PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	1A0 – 1A3	Data inputs
11, 13, 15, 17	2A0 – 2A3	Data inputs
18, 16, 14, 12	1Y0 – 1Y3	Data outputs
9, 7, 5, 3	2Y0 – 2Y3	Data outputs
1, 19	$1\overline{OE}$ , $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	$V_{CC}$	Positive supply voltage

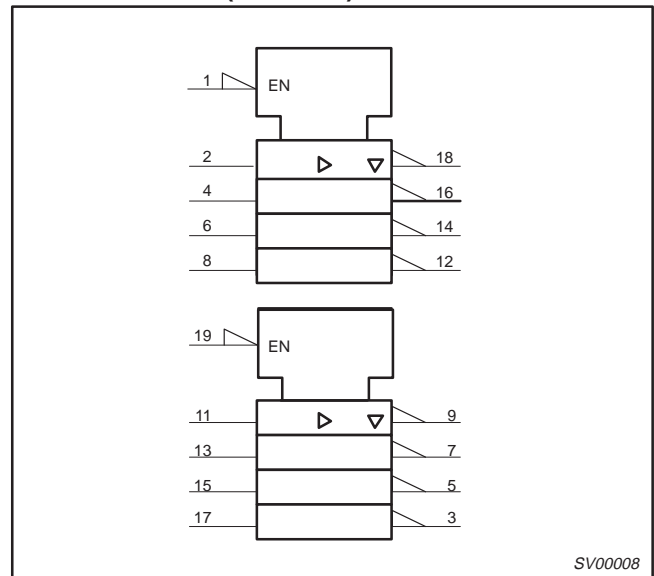
# 3.3V Octal inverting buffer (3-State)

74LVT240

## LOGIC SYMBOL



## LOGIC SYMBOL (IEEE/IEC)



## FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nAx	nYx
L	L	H
L	H	L
H	X	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "Off" state

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +4.6	V
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

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74LVT240

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	2.7	3.6	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Low-level Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
Δt/Δv	Input transition rise or fall rate; outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T <sub>amb</sub> = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7V; I <sub>I</sub> = -18mA		0.9	-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> -0.2	V <sub>CC</sub> -0.1		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -8mA	2.4	2.5		V
		V <sub>CC</sub> = 3V; I <sub>OH</sub> = -32mA	2	2.2		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100μA		0.1	0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA		0.3	0.5	
		V <sub>CC</sub> = 3V; I <sub>OL</sub> = 16mA		0.25	0.4	
		V <sub>CC</sub> = 3V; I <sub>OL</sub> = 32mA		0.3	0.5	
		V <sub>CC</sub> = 3V; I <sub>OL</sub> = 64mA		0.4	0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V		1	10	μA
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	±0.1	±1	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>	Data pins <sup>4</sup>	0.1	1	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0		-1	-5	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		1	±100	μA
I <sub>HOLD</sub>	Bus Hold current A inputs <sup>NO TAG</sup>	V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V	75	150		μA
		V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V	-75	-150		
		V <sub>CC</sub> = 0V to 3.6V; V <sub>CC</sub> = 3.6V	±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		60	125	μA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> = ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care		±1	±100	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 3.6V; V <sub>O</sub> = 3.0V		1	5	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 3.6V; V <sub>O</sub> = 0.5V		-1	-5	μA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.12	0.19	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		3	12	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>NO TAG</sup>		0.12	0.19	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3.0 to 3.6V; One input at V <sub>CC</sub> -0.6V; Other inputs at V <sub>CC</sub> or GND		0.1	0.2	mA

## NOTES:

- All typical values are at T<sub>amb</sub> = 25°C.
- This is the increase in supply current for each input at V<sub>CC</sub> -0.6V.
- This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 10% a transition time of 100μsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C, only.
- Unused pins at V<sub>CC</sub> or GND
- I<sub>CCZ</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

# 3.3V Octal inverting buffer (3-State)

74LVT240

## AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ;  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

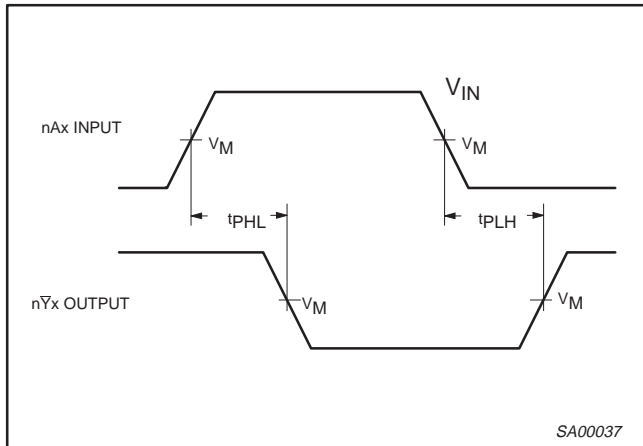
SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$			$V_{\text{CC}} = 2.7\text{V}$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nAx to nYx	1	1 1	2.5 2.5	4.3 4.3	5.2 5.0	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to High and Low level	2	1 1	3.7 3.1	5.2 5.2	6.3 6.7	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from High and Low level	2	2 1.6	3.4 3.2	5.6 5.1	6.3 5.6	ns

**NOTE:**

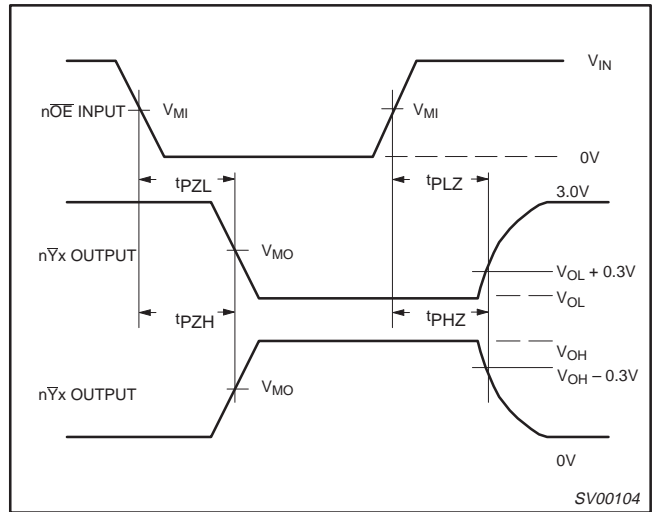
1. All typical values are at  $V_{\text{CC}} = 3.3\text{V}$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

## AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND}$  to  $2.7\text{V}$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays

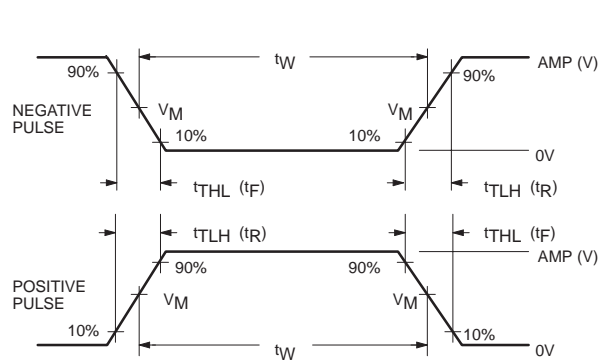
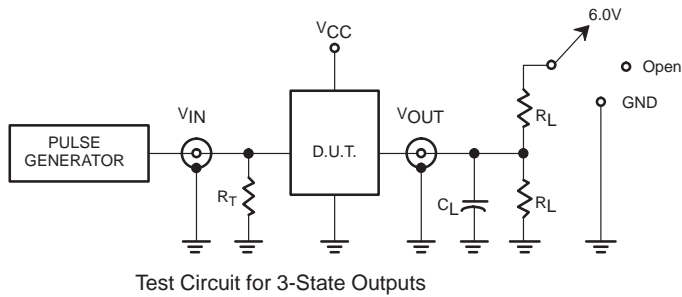


Waveform 2. 3-State Output Enable and Disable Times

# 3.3V Octal inverting buffer (3-State)

# 74LVT240

## TEST CIRCUIT AND WAVEFORMS



### SWITCH POSITION

TEST	SWITCH
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6V
$t_{PHZ}/t_{PZH}$	GND

### DEFINITIONS

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.

$C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

$R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_W$	$t_R$	$t_F$
74LVT	2.7V	$\leq 10MHz$	500ns	$\leq 2.5ns$	$\leq 2.5ns$

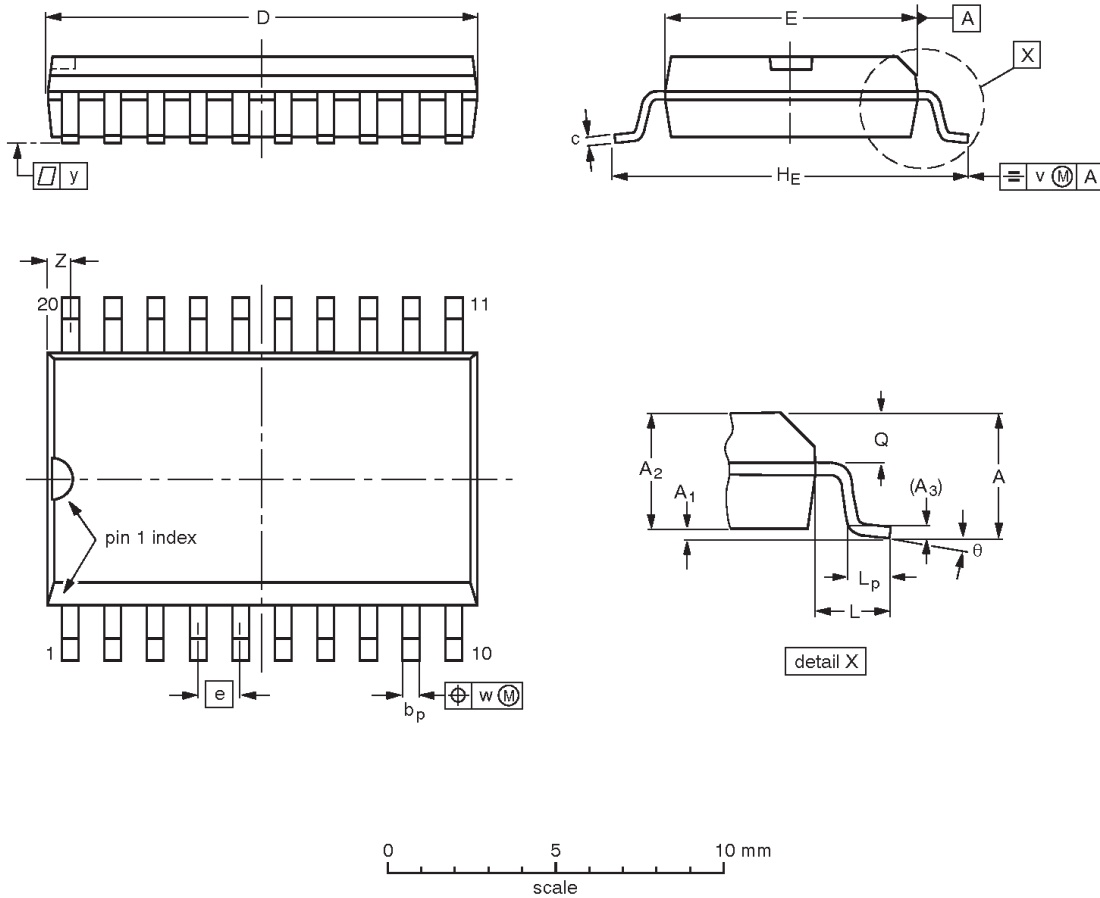
SV00092

# 3.3V Octal inverting buffer (3-State)

# 74LVT240

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	$\theta$
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

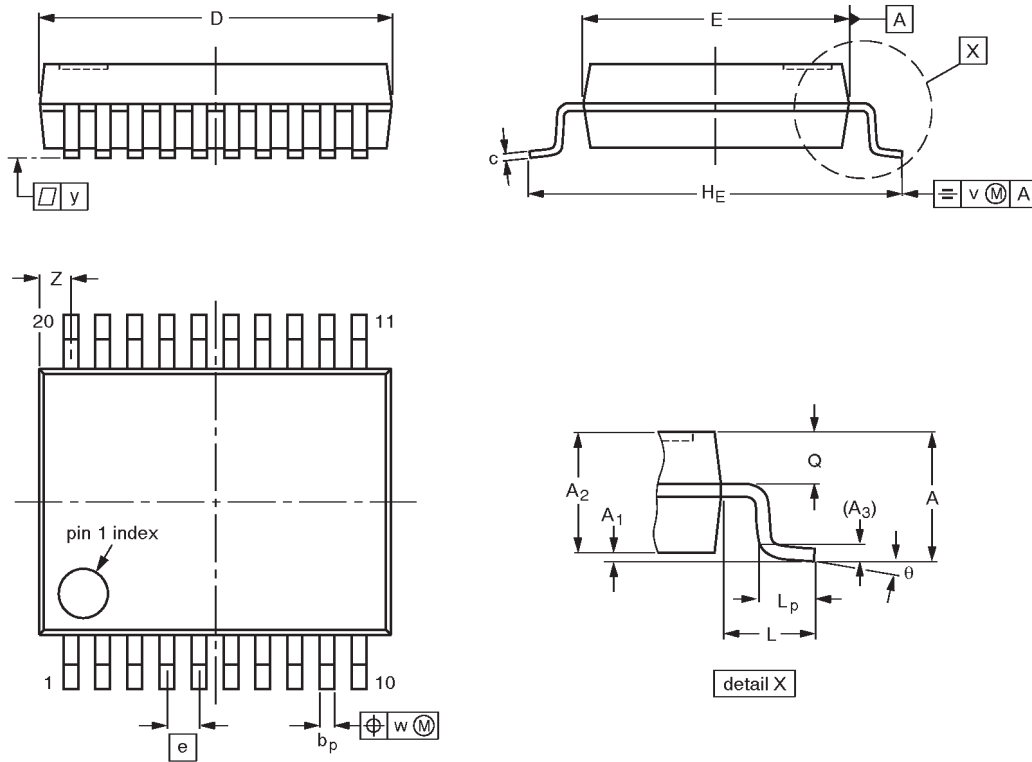
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

# 3.3V Octal inverting buffer (3-State)

# 74LVT240

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

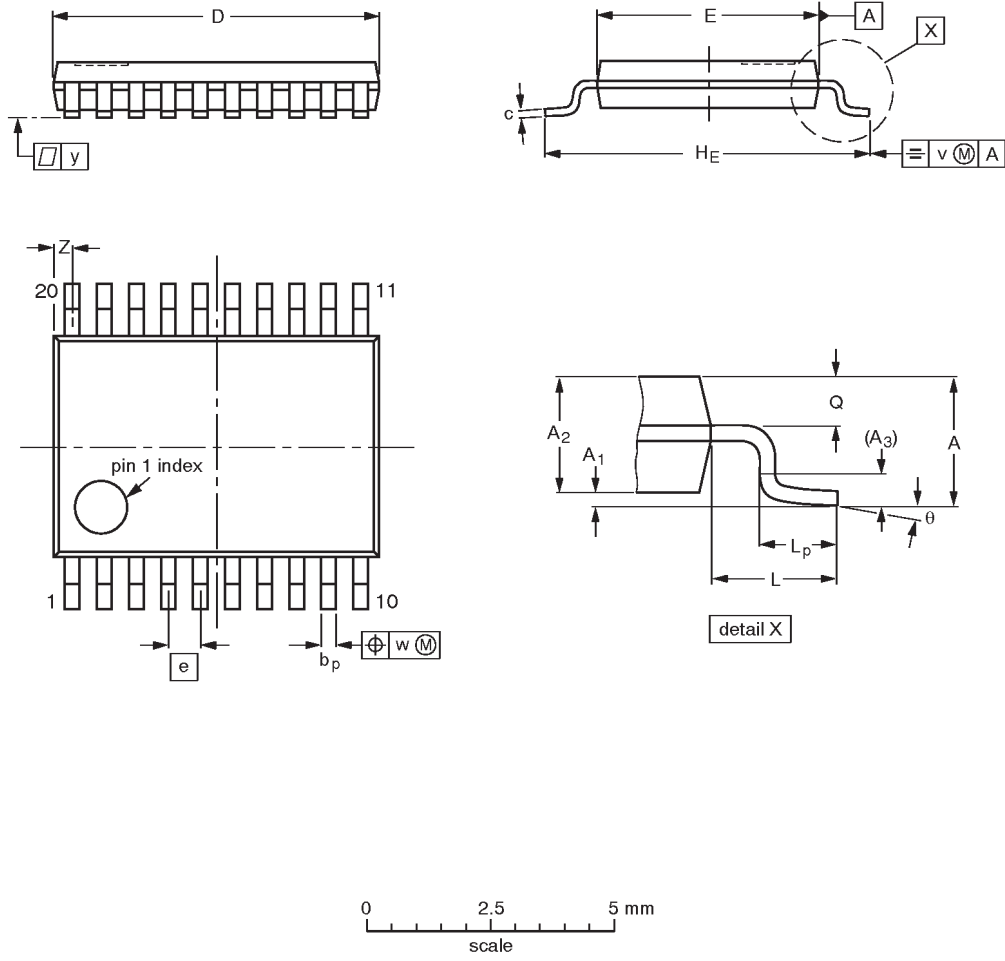
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

# 3.3V Octal inverting buffer (3-State)

# 74LVT240

**TSSOP20:** plastic thin shrink small outline package; 20 leads; body width 4.4 mm

**SOT360-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16- 95-02-04

## 74LVT240

**Data sheet status**

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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