WM8733

102dB Stereo DAC

Product Preview, July 2000, Rev 1.3

DESCRIPTION

WM8733 is a high performance stereo DAC designed for use in portable audio equipment, video CD players and similar applications. It comprises selectable normal or I^2S compatible serial data interfaces for 16 to 24-bit inputs, high performance digital filters, and sigma-delta output DACs, achieving an 102dB signal-to-noise ratio.

The device is available in a 14-pin SOIC package that offers selectable mute and de-emphasis functions using a minimum of external components.

Low supply voltage operation and low current consumption are valuable features, particularly for use in portable equipment.

Additional modes consist of a powerdown option and the possibility of generating separate differential left and right outputs for applications demanding higher performance.

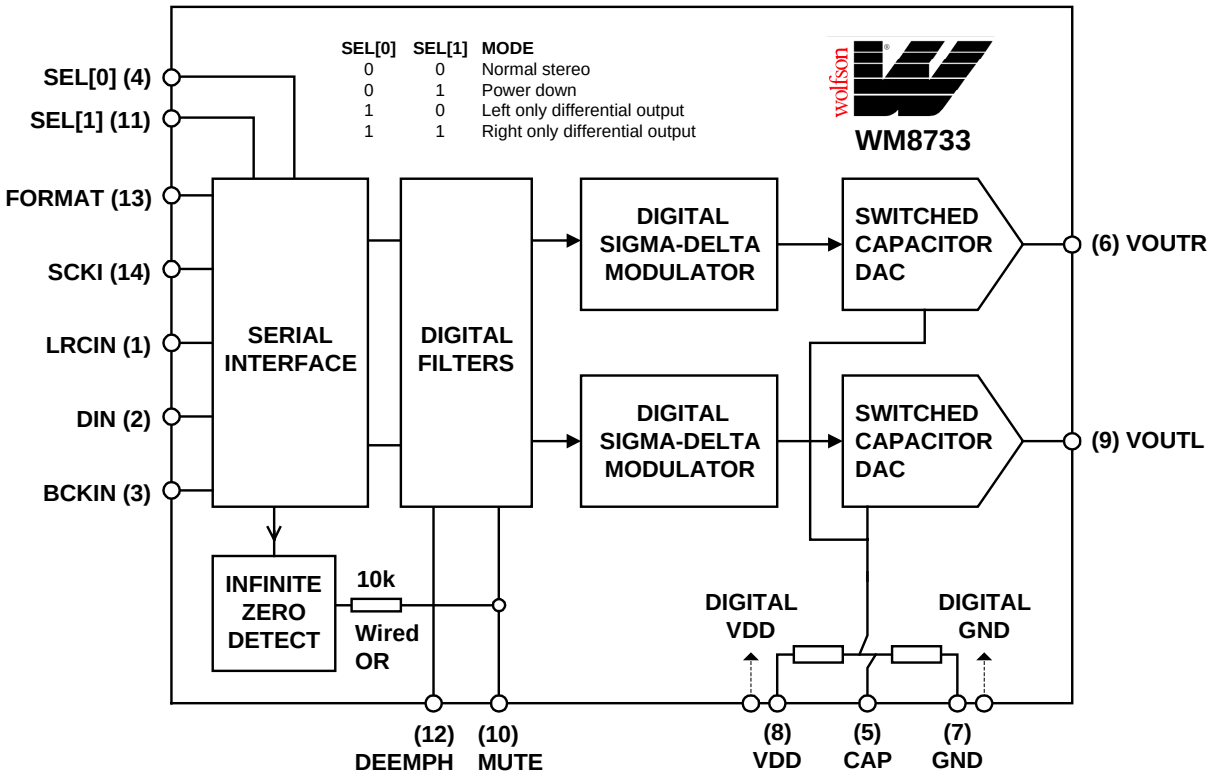
FEATURES

- **High tolerance to clock jitter**
- **Compatible with PCM1733**
- **Distortion > 90dB, SNR > 102dB, dynamic range performance > 100dB**
- **Stereo DAC with input sampling from 8kHz to 96kHz**
- **Additional mute feature and high performance differential modes**
- **Normal or I^2S compatible data format**
- **Sigma-delta design with 64x oversampling**
- **System clock 256fs or 384fs or 512fs**
- **Supply range 3V to 5V**
- **Analogue voltage output to drive 2kΩ load**
- **14-pin SOIC package**

APPLICATIONS

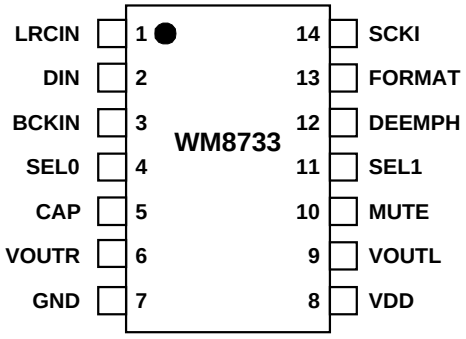
- **High performance consumer audio**

BLOCK DIAGRAM



WOLFSON MICROELECTRONICS LTD.
Lutton Court, Bernard Terrace, Edinburgh, EH8 9NX, UK
Tel: +44 (0) 131 667 9386
Fax: +44 (0) 131 667 5176
Email: sales@wolfson.co.uk
http://www.wolfson.co.uk

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
XWM8733ED	-25 to +85°C	14-pin SOIC

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Supply voltage	-0.3V	+7.0V
Reference input		VDD+0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature	-65°C	+150°C
Lead temperature (soldering, 10 seconds)		+260°C
Lead temperature (soldering, 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply range	VDD		-10%	3.0 to 5.0	+10%	V
Ground	GND			0		V
Supply current		VDD = 5V		15		mA

ELECTRICAL CHARACTERISTICS

Test Characteristics

VDD = 5V, GND = 0V, T_A = +25°C, fs = 44.1kHz, SCKI = 384fs unless otherwise stated.

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels							
Input LOW level		V_{IL}				0.8	V
Input HIGH level		V_{IH}		2.0			V
Analogue Output Levels							
Output level			Into 10kohm, full scale 0dB, (5V supply)		1		V_{RMS}
			Into 10kohm, full scale 0dB, (3V supply)		0.6		V_{RMS}
Minimum resistance load			o midrail or AC coupled (5V supply)	2	10		kohms
			o midrail or AC coupled (3V supply)		10		kohms
Maximum capacitance load			5V or 3V		100		pF
Output DC level					VDD/2		V
Reference Levels							
Potential divider resistance			VDD to CAP and CAP to GND	80	100	120	kohms
Voltage at CAP					VDD/2		
DAC Circuit Specifications							
SNR (Note 1)	Stereo mode		VDD = 5V	98	102		dB
	Mono mode						dB
	Stereo mode		VDD = 3V	96	100		dB
	Mono mode						dB
THD (full scale)			0dB		0.03	0.01	%
THD+N			-60dB	-35	-40		dB
Frequency response				0		20,000	Hz
Pass band ripple					±0.25		dB
Transition band				20,000			Hz
Out of band rejection					-40		dB
Dynamic Range	Stereo mode				100		dB
	Mono mode						dB
Channel Separation					90		dB
Gain mismatch channel-to-channel					±1	±5	%FSR
Audio Data Input and System Clock Timing Information							
BCKIN pulse cycle time		t_{BCY}		100			ns
BCKIN pulse width high		t_{BCH}		50			ns
BCKIN pulse width low		t_{BCL}		50			ns
BCKIN rising edge to LRCIN edge		t_{BL}		30			ns
LRCIN rising edge to BCKIN rising edge		t_{LB}		30			ns
DIN setup time		t_{DS}		30			ns
DIN hold time		t_{DH}		30			ns
System clock pulse width high		t_{SCKIH}		13			ns
System clock pulse width low		t_{SCKIL}		13			ns

Note 1 Ratio of RMS output level with 1kHz full scale input, to the RMS output level with all zeros into the digital input, measured "A" weighted over a 20Hz to 20kHz bandwidth.

Note 2 All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LRCIN	Digital input	Sample rate clock input
2	DIN	Digital input	Serial data input
3	BCKIN	Digital input	Bit clock input
4	SEL0	Digital input	Mode select (internal pull-down)
5	CAP	Analogue output	Analogue internal reference
6	VOUTR	Analogue output	Right channel DAC output
7	GND	Supply	0V supply
8	VDD	Supply	Positive supply
9	VOUTL	Analogue output	Left channel DAC output
10	MUTE	Digital input	Soft mute control; high = muted, Z = auto mute input/output
11	SEL1	Digital input	Mode select (internal pull-down)
12	DEEMPH	Digital input	De-emphasis select; high = de-emphasis ON (44.1kHz only), (internal pull-up)
13	FORMAT	Digital input	Data input format select; 'lo' = normal, 'hi' = I^2S (internal pull-up)
14	SCKI	Digital input	System clock input (256fs or 384fs or 512fs)

DEVICE DESCRIPTION

INTRODUCTION

WM8733 is a complete high performance stereo audio 18-bit digital-to-analogue converter, including digital interpolation filter, multibit sigma-delta with dither, and switched capacitor multibit stereo DAC and output smoothing filters.

Special functions of soft mute and de-emphasis are provided, and operation using system clock of 256fs, or 384fs or 512fs is provided, selection between either clock rate being automatically controlled. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input.

An auto mute function is provided which is enabled if MUTE (pin 10) is left at high impedance. If 64 successive left and right channel data samples of value 0 are received, auto mute is achieved. This signal is wire ORed to MUTE (pin 10) via 10K resistor. If MUTE (pin 10) internally is not externally driven, the internal auto mute state is visible on this pin as a weak drive strength signal (10kΩ source).

MUTE	DESCRIPTION
0	Soft mute is OFF
Z	Auto mute is enabled
1	Soft mute is ON

Table 1 Soft Mute Control

A novel multi bit sigma-delta DAC design is used, utilising a 64x oversampling rate, to optimise signal to noise performance and offer increased clock jitter tolerance.

Internally generated midrail references are used to DC bias output signals, requiring only a single external capacitor for decoupling purposes.

The device is packaged in a small 14-pin SOIC package, offering pin compatibility with Burr Brown PCM1733, but with added functionality of a soft mute input pin, which may be left floating to enable auto mute detection, or held ‘low’ leaving the device operational.

Single 3V to 5V supplies may be used, the output amplitude scaling with absolute supply level. Low supply voltage operation and low current consumption, and the low pin count small package, make the WM8733 attractive for many consumer type applications.

DAC CIRCUITS

The WM8733 DACs are designed to allow playback of 18-bit PCM audio or similar data with high resolution and low noise and distortion. Sample rates up to 96ks/s may be used, with much lower sample rates acceptable provided that the ratio of sample rate (LRCIN) to system clock is maintained at the required 256fs, or 384fs or 512fs times.

The DACs on WM8733 are implemented using sigma-delta oversampled conversion techniques. These require that the PCM samples are digitally filtered and interpolated to generate a set of samples at a much higher rate than the input rate. This sample stream is then digitally modulated to generate a digital pulse stream that is then converted to analogue signals in a switched capacitor DAC. The advantage of this technique is that the DAC is linearised using noise shaping techniques, allowing the 16-bit resolution to be met using non-critical analogue components. A further advantage is that the high sample rate at the DAC output means that smoothing filters on the output of the DAC need only have fairly crude characteristics in order to remove the characteristic steps, or images, on the output of the DAC. In order to ensure that generation of tones characteristic to sigma-delta convertors is not a problem, dithering is used in the digital modulator, and a higher order modulator is used. The switched capacitor technique used in the DAC reduces sensitivity to clock jitter compared to switched current techniques used in other implementations.

De-emphasis of 44.1kHz signals may be applied if required.

DEEMPH	DESCRIPTION
0	De-emphasis is OFF
1	De-emphasis is ON (44.1kHz only)

Table 2 De-emphasis Control

The voltage on the CAP pin is used as the reference for the DACs, therefore the amplitude of the signals at the DAC outputs will scale with the amplitude of the voltage at the CAP. An external reference could be used to drive in on the CAP pin if desired, but a value typically of about midrail should be used for optimum performance.

The outputs of the 2 DACs are buffered out of the device by buffer amplifiers. These amplifiers will source load current of several mA and sink current up to 1.5mA, so allowing significant loads to be driven. The output source is active, the sink is Class A, i.e. fixed value, so greater loads might be driven if an external 'pull-down' resistor is connected at the output.

Typically an external low pass filter circuit will be used to remove residual sampling noise of the 64x oversampling used and if desired adjust the signal amplitude and device strength.

SERIAL DATA INTERFACE

WM8733 has serial interface formats that are fully compatible with both normal (MSB first, right-justified) and I^2S interfaces. The data format is selected with the FORMAT pin. When FORMAT is LOW, normal data format is selected. When the format is HIGH, I^2S format is selected.

If the application demands 16-bit or 20-bit data, then I^2S format may be used. Two LSBs will be lost in 20-bit mode. Normal mode will support 18-bit data applications or 16-bit packed mode applications (automatically detected).

Note: In 16-bit "packed" mode operation (exactly 32 BLCKS per LRCIN period) the data word must align exactly with LRCIN clock edges (effectively both left and right justified at the same time).

FORMAT	DESCRIPTION
0	Normal format (MSB-first, right justified)
1	I^2S format (Philips serial data protocol)

Table 3 Serial Interface Formats

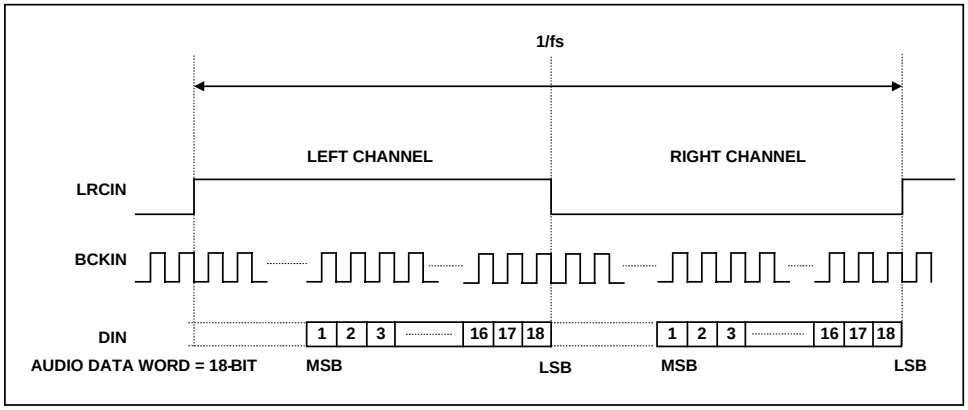


Figure 1 'Normal' Data Input Timing

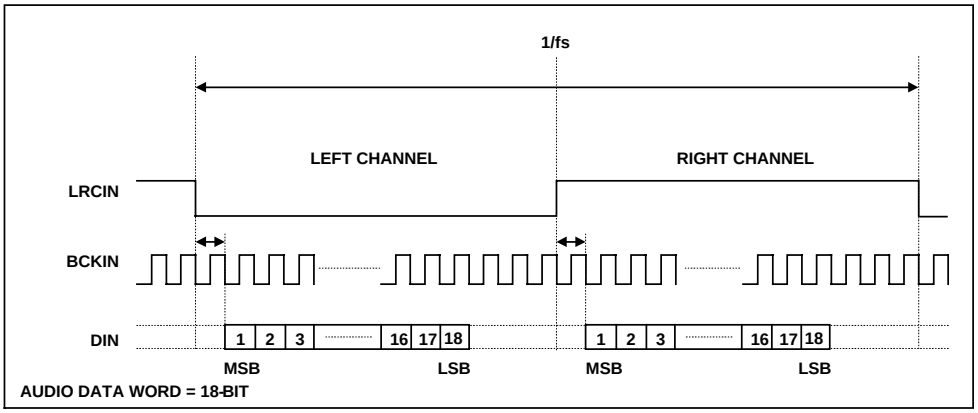


Figure 2 I^2S Data Input Timing

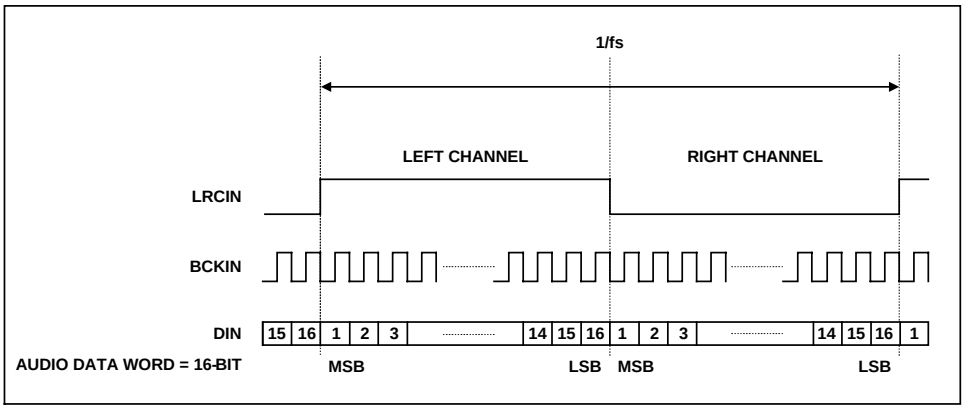


Figure 3 16-bit Normal Packed Mode

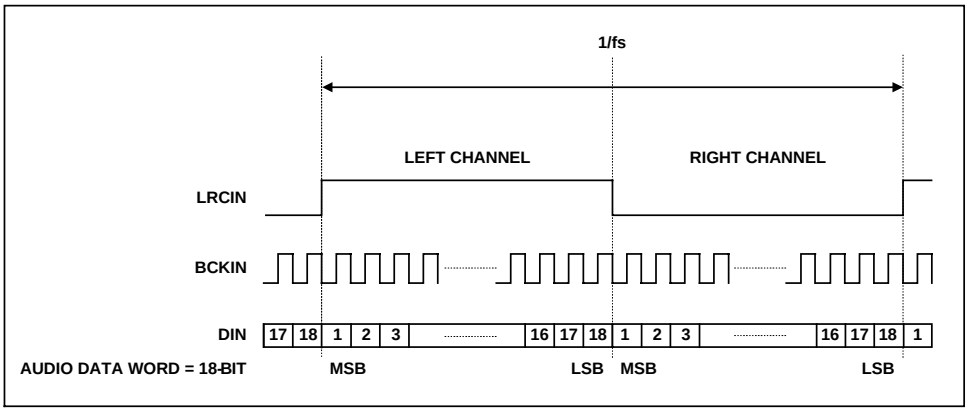


Figure 4 18-bit Normal Packed Mode

MODE SELECT PINS

The WM8733 has four possible modes.

SEL0	SEL1	MODE
0	0	Normal stereo operation
0	1	Power down
1	0	Left only differential output
1	1	Right only differential output

Table 4 Mode Select Pins

The SEL0/1 pins (pins 4 and 11) can be hard wired, or left floating as internal “pull-downs” will cause the device to operate in normal stereo mode.

SYSTEM CLOCK

The system clock is used to operate the digital filters and the noise shaping circuits. The system clock input is at pin 14 (SCKI). The frequency of WM8733's system clock should be set to 256fs or 384fs or 512fs, (where fs is the audio sampling frequency). The sample rate is typically: 32 kHz, 44.1 kHz, 48 kHz or 96kHz.

WM8733 has a system clock detection circuit that automatically determines whether the system clock being supplied is at 256fs or 384fs or 512fs. The system clock should be synchronised with LRCIN, but WM8733 is tolerant of phase differences. Severe distortion in the phase difference between LRCIN and the system clock will be detected, and cause the device to automatically resynchronise. During resynchronisation, the output of the device will either repeat the previous sample, or drop the next sample, depending on the nature of the phase slip. This will ensure minimal "click" at the analog outputs during resynchronisation.

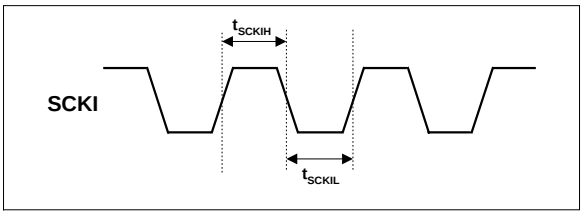


Figure 5 System Clock Timing Requirements

SAMPLING RATE (LRCIN)	SYSTEM CLOCK FREQUENCY (MHz)		
	256fs	384fs	512fs
32 kHz	8.192	12.288	16.384
44.1 kHz	11.2896	16.9340	22.5792
48 kHz	12.288	18.432	24.576
96kHz	24.576	36.864	49.152

Table 5 System Clock Frequencies Versus Sampling Rate

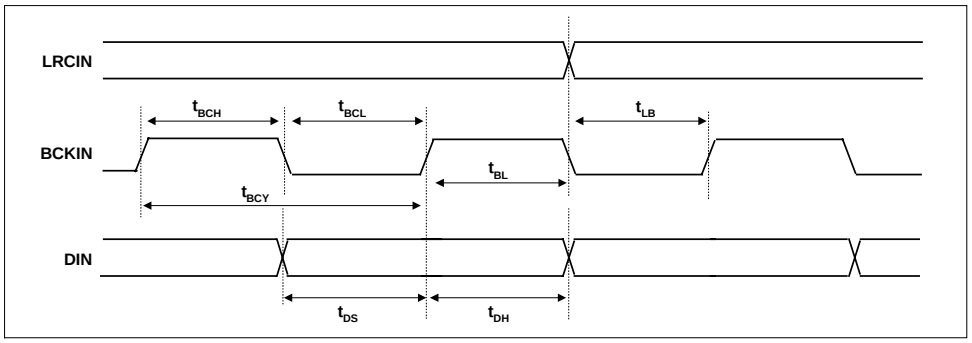


Figure 6 Audio Data Input Timing

RECOMMENDED EXTERNAL COMPONENTS

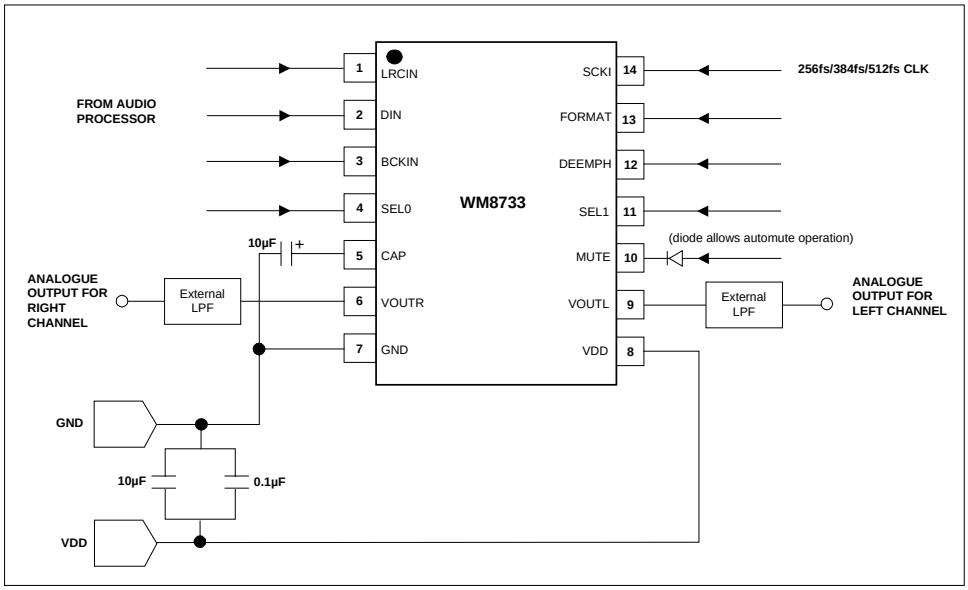


Figure 5 Applications Diagram

DETAIL OF APPLICATION DIAGRAM SHOWING THE EXTERNAL LOW POWER FILTER

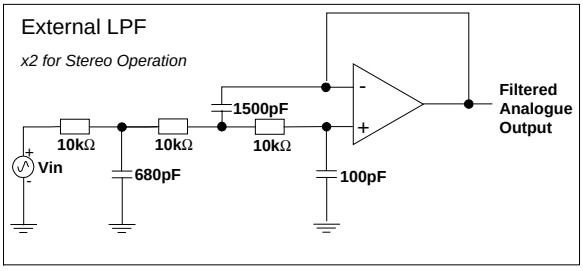
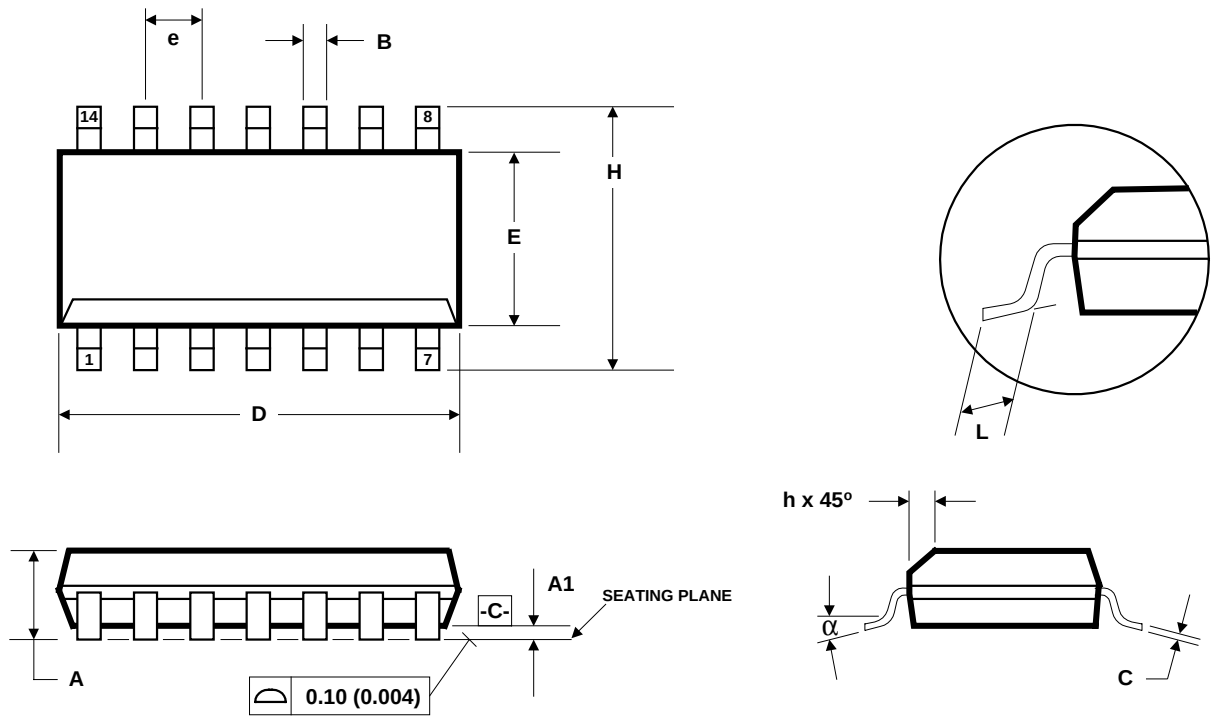


Figure 6 Third-Order Low Pass Filter (LPF) Example

An external low pass filter is recommended if the device is driving a wide band amplifier, as shown in Figure 6. In some applications, second-order or passive RC filter may be adequate.

PACKAGE DIMENSIONS

D: 14 PIN SOIC 3.9mm Wide Body **DM001.C**



Symbols	Dimensions (MM)		Dimensions (Inches)	
	MIN	MAX	MIN	MAX
A	1.35	1.75	0.0532	0.0688
A1	0.10	0.25	0.0040	0.0098
B	0.33	0.51	0.0130	0.0200
C	0.19	0.25	0.0075	0.0098
D	8.55	8.75	0.3367	0.3444
E	3.80	4.00	0.1497	0.1574
e	1.27 BSC		0.05 BSC	
H	5.80	6.20	0.2284	0.2440
h	0.25	0.50	0.0099	0.0196
L	0.40	1.27	0.0160	0.0500
α	0^o	8^o	0^o	8^o
REF:	JEDEC.95, MS-012			

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS (INCHES).
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM (0.010IN).
D. MEETS JEDEC.95 MS-012, VARIATION = AB. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.