WM9710

AC'97 Audio CODEC and Mixer with Integrated Headphone Driver

DESCRIPTION

The WM9710 is a high-quality stereo audio codec with an integrated headphone driver.

The device is compliant with the Intel AC'97 Rev 2.2 specification. It performs full-duplex 18-bit codec functions and supports variable sample rates from 8kHz to 48kHz with high signal to noise ratio. Analogue mixers are included to mix external analogue signals into the playback or record path.

The WM9710 allows designers to easily integrate phone functions with other audio functions such as MP3 playback and voice recording. Mono inputs and outputs are provided to connect to an external voice codec. The on-chip headphone driver can distinguish between a stereo headphone and mono headset, and route the signals accordingly.

Optional AC'97 features include 3D sound enhancement, primary/secondary mode operation and S/PDIF or I^2S output.

The 5-pin bi-directional AC-Link interface transfers control data, DAC and ADC words to and from the AC'97 controller. The WM9710 is fully operable on 3V or 5V or mixed 3/5V supplies, and is packaged in a leadless, chip scale QFN package with 7mm body size or 48-pin TQFP package.

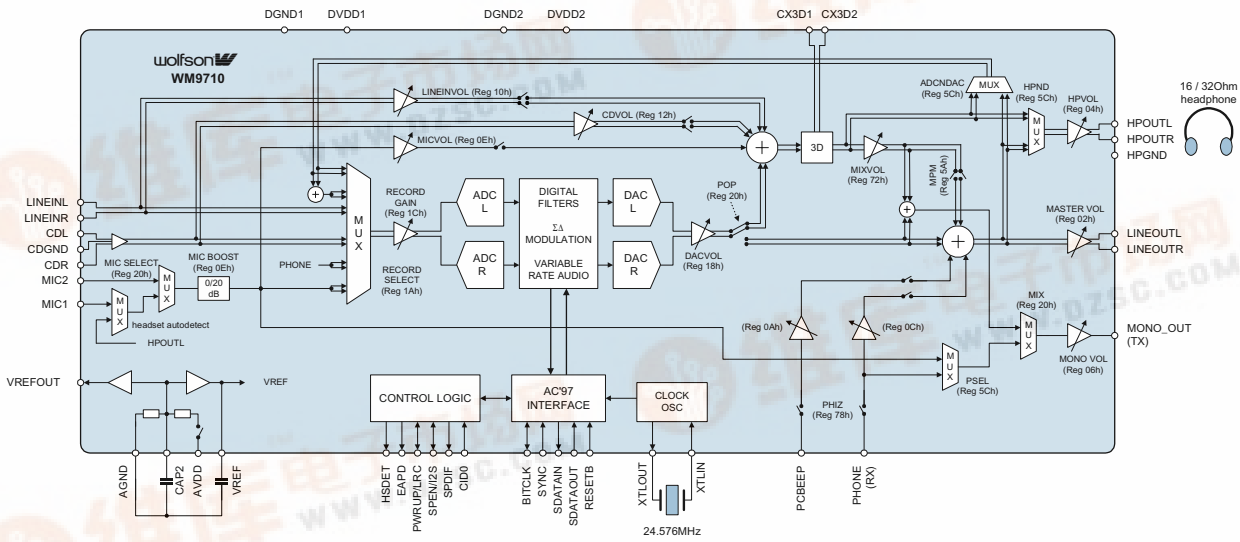
FEATURES

- AC'97 rev2.2 compliant, 18-bit stereo codec
- Integrated headphone driver
- Automatic headset detection and switching (for stereo headphones / mono phone headsets)
- Separately mixed mono output for phone TX path (also includes headphone buffer for mono earpiece)
- Multiple channel input mixer
- Mono inputs for phone RX and PCBEEP signals
- On-chip sample rate conversion, supports rates from 8kHz to 48kHz. DAC and ADC rates are fully independent.
- Optional S/PDIF or I^2S digital audio output
- 3V to 5V operation
- Each circuit block can be separately powered on or off
- Leadless 7mm × 7mm × 0.9mm QFN or 48-pin TQFP package

APPLICATIONS

- Personal Digital Assistants and 'Smartphones'
- WinCE systems

BLOCK DIAGRAM



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ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL
XWM9710EFT/V	-25 to 85°C	48-pin TQFP	MSL1
WM9710SEFT/V	-25 to 85°C	48-pin TQFP (lead free)	MSL1
XWM9710EFT/RV	-25 to 85°C	48-pin TQFP (tape and reel)	MSL1
WM9710SEFT/RV	-25 to 85°C	48-pin TQFP (lead free, tape and reel)	MSL1

DEVICE	TEMP. RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL
XWM9710EFL/V	-25 to 85°C	48-pin QFN	MSL3
WM9710SEFL/V	-25 to 85°C	48-pin QFN (lead free)	MSL3
XWM9710EFL/RV	-25 to 85°C	48-pin QFN (tape and reel)	MSL3
WM9710SEFL/RV	-25 to 85°C	48-pin QFN (lead free, tape and reel)	MSL3

Note:

Reel quantity = 2,200

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

Note:
The TQFP version is classified as MSL1 and does not require to be drybagged but will be supplied as such, labelled as MSL1.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DVSS -0.3V	DVDD +0.3V
Voltage range analogue inputs	AVDD -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body temperature (soldering 2 minutes)		+183°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD1, DVDD2		2.7		5.5	V
Analogue supply range	AVDD		2.7		5.5	V
Digital ground	DGND1, DGND2			0		V
Analogue ground	AGND, HPGND			0		V
Difference AGND to DGND – Note 1			-0.3	0	+0.3	V
Difference AVDD to DVDD – Note 2			-0.3		5.5	V

Note:

1. AGND is normally the same as DGND and HPGND
2. AVDD should be greater than or equal to DVDD

PIN CONFIGURATION

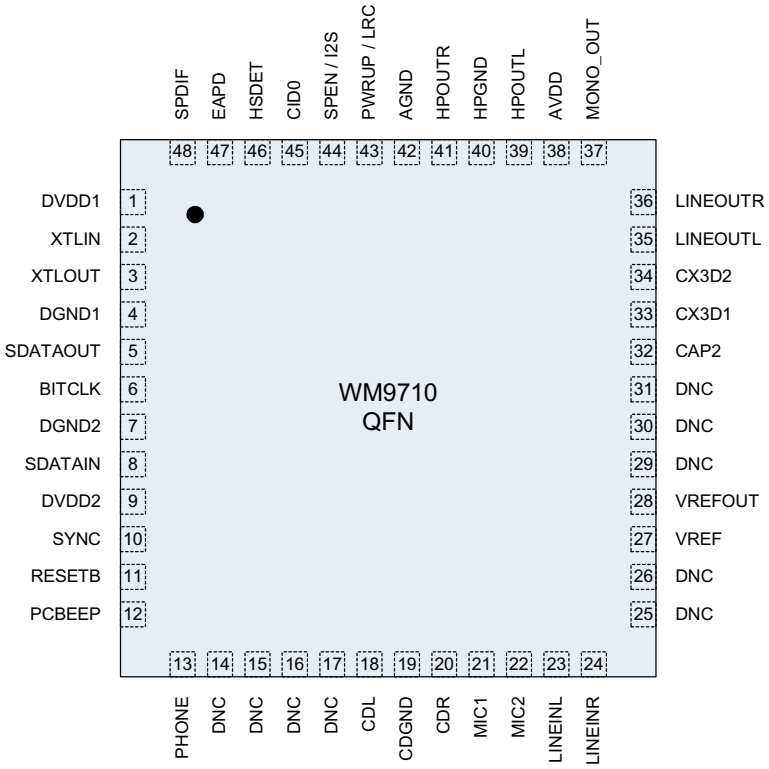


Figure 1 QFN Pinout

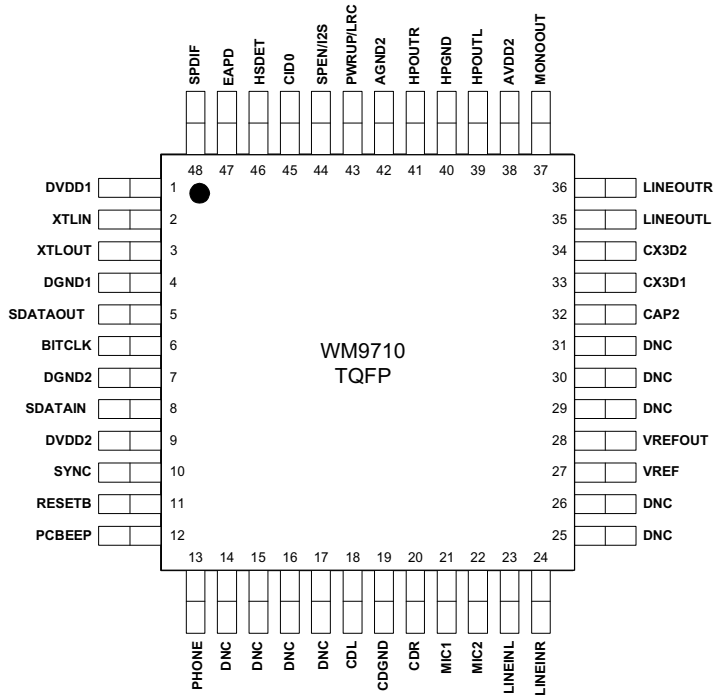


Figure 2 TQFP Pinout

PIN DESCRIPTION

PIN	48 PIN TQFP OR 48 QFN	TYPE	DESCRIPTION
1	DVDD1	Supply	Digital supply
2	XTLIN	Digital input	Clock crystal connection or clock input (if XTAL not used)
3	XTLOUT	Digital output	Clock crystal connection
4	DGND1	Supply	Digital ground
5	SDATAOUT	Digital input	Serial data input (AC-Link signal)
6	BITCLK	Digital I/O	Serial interface clock (AC-Link signal)
7	DGND2	Supply	Digital ground
8	SDATAIN	Digital output	Serial data output (AC-Link signal)
9	DVDD2	Supply	Digital supply
10	SYNC	Digital input	Serial interface sync pulse (AC-Link signal)
11	RESETB	Digital input	Reset input (active low, resets registers)
12	PCBEEP	Analogue input	PCBEEP input (mono input to mixer)
13	PHONE	Analogue input	Phone RX input (mono input to mixer)
14	DNC	Do Not Connect	Leave this pin floating
15	DNC	Do Not Connect	Leave this pin floating
16	DNC	Do Not Connect	Leave this pin floating
17	DNC	Do Not Connect	Leave this pin floating
18	CDL	Analogue input	CD Left (stereo input to mixer)
19	CDGND	Analogue input	CD input common mode reference (ground)
20	CDR	Analogue input	CD Right (stereo input to mixer)
21	MIC1	Analogue input	Microphone input 1 – also HSET detect input
22	MIC2	Analogue input	Microphone input 2
23	LINEINL	Analogue input	Line-in Left (stereo mixer input)
24	LINEINR	Analogue input	Line-in Right (stereo mixer input)
25	DNC	Do Not Connect	Leave this pin floating
26	DNC	Do Not Connect	Leave this pin floating
27	VREF	Analogue output	Internal reference (buffered CAP2)
28	VREFOUT	Analogue output	Microphone bias voltage (buffered CAP2)
29	DNC	Do Not Connect	Leave this pin floating
30	DNC	Do Not Connect	Leave this pin floating
31	DNC	Do Not Connect	Leave this pin floating
32	CAP2	Analogue I/O	Reference input/output; pulls to AVDD/2 if not overdriven
33	CX3D1	Analogue output	Output pin for 3D enhancement function
34	CX3D2	Analogue input	Input pin for 3D enhancement function
35	LINEOUTL	Analogue output	Line-out Left
36	LINEOUTR	Analogue output	Line-out Right
37	MONOOUT	Analogue output	Mono output (Phone TX or mono earpiece)
38	AVDD	Supply	Analogue supply
39	HPOUTL	Analogue output	Headphone output Left (or headset mic input if headset detect function is enabled)
40	HPGND	Supply	Headphone ground
41	HPOUTR	Analogue output	Headphone output Right
42	AGND	Supply	Analogue ground
43	PWRUP/LRC	Digital I/O	Power-up control (or LRCLK signal for I^2S output)
44	SPEN/I^2S	Digital I/O	SPDIF hardware enable pin and I^2S data output
45	CID0	Digital input	Primary/Secondary codec select (internal pull-up) Hi = Primary
46	HSDET	Digital output	Headset detect signal
47	EAPD	Digital output	External amplifier powerdown (or general purpose control output)
48	SPDIF	Digital output	S/PDIF output

ELECTRICAL CHARACTERISTICS

Test Characteristics:
AVDD = 3.3V, DVDD = 3.3V, 48kHz audio sampling, $T_A = 25^oC$, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (DVDD = 3.3V)						
Input LOW level	V_{IL}		DGND - 0.3		0.8	V
Input HIGH level	V_{IH}		2.2		DVDD + 0.3	V
Output LOW	V_{OL}	I Load = 2mA			0.10 x DVDD	V
Output HIGH	V_{OH}	I Load = -2mA	0.90 x DVDD			V
Analogue Audio I/O Levels (Input Signals on any audio inputs, Outputs on LINEOUT L, R and MONO and HPOUT L,R)						
Input level		Minimum input impedance = 10k	AGND -100mV		AVDD +100mV	V
Output level to LINEOUT L,R		Into 10kΩ load	AGND +300mV	Near rail to rail	AVDD -300mV	V
Output level to HPOUT L, HPOUTR and MONOOUT		Into 16Ω load	AGND +300mV	Near rail to rail	AVDD -300mV	V
Reference Levels						
Reference input/output	CAP2		0.47 AVDD	0.50 AVDD	0.53 AVDD	V
CAP2 impedance				75		kΩ
Mixer reference	VREF			Buffered CAP2		V
MIC reference	VREFOUT			Buffered CAP2		V
MIDBUFF current source (pins VREF and VREFOUT)		AVDD = 3.3V	5	10		mA
MIDBUFF current sink (pins VREF and VREFOUT)		AVDD = 3.3V	-5	-10		mA
AUDIO DAC to Line-out (10kΩ load)						
SNR A-weighted (Note 2)			85	91		dB
Full scale output voltage		VREF = 1.65V		0.7		Vrms
Total Harmonic Distortion + Noise	THD+N	-3dBfs input		-84 0.006	-74 0.02	dB %
PSRR		20 to 20kHz, without supply decoupling		-40		dB
AUDIO ADC						
ADC input for full scale output		VREF = 1.65V		0.7		Vrms
Signal to Noise Ratio A-weighted (Note 2)	SNR		80	86		dBfs
Total Harmonic Distortion+Noise	THD+N	-6dBfs input		-79	-72	dB
Power Supply Rejection Ratio	PSRR	20 to 20kHz, without supply decoupling		-40		dB
Digital Filter Characteristics						
Frequency response			20		19,200	Hz
Transition band			19,200		28,800	Hz
Stop band			28,800			Hz
Stop band attenuation		ADC	-74			dB
		DAC	-40			

Test Characteristics:
AVDD = 3.3V, DVDD = 3.3V, 48kHz audio sampling, $T_A = 25^oC$, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Mixer Inputs to Line-out (10kΩ load)						
Maximum input voltage			AGND	0.7	AVDD	Vrms
Maximum output voltage		on LINEOUT		0.7		Vrms
Signal to Noise Ratio A-weighted (Note 2)	SNR	CD inputs	90	92		dB
		Other inputs	82	93		
Total Harmonic Distortion + Noise -1dBfs input	THD+N	CD and LINE inputs		-87 0.0044	-77 0.014	dB %
		PHONE input		-82 0.008	-71 0.028	
		MIC1 input		-82 0.008	-71 0.028	
		MIC2 input		-90 0.003	-71 0.028	
		PCBEEP input		-78 0.013	-67 0.045	
Input impedance (CD inputs)		At any gain		15		kΩ
Input impedance (other mixer inputs)		At max gain	10	20		kΩ
		At 0db gain	50	100		kΩ
Input impedance MIC inputs		At max gain	10	20		kΩ
		At 0db gain	55	100		kΩ
Power Supply Rejection Ratio	PSRR	20 to 20kHz, without supply decoupling		-40		dB
Headphone Buffer (pins HPOUTL, HPOUR and MONOOUT)						
Maximum output voltage				0.7		Vrms
Max Output Power (Note 1)	P_O	RL = 32Ω		30		mW
		RL = 16Ω		40		mW
SNR (Note 2)		A-weighted	85	92		dB
Total Harmonic Distortion + Noise	THD+N	1kHz, R_L = 32Ω @ P_O = 10mW rms		-80 0.01		dB %
		1kHz, R_L = 32Ω@ P_O = 20mW rms		-77 0.014		dB %
		1kHz, R_L = 16Ω @ P_O = 10mW rms		-76dB 0.016		dB %
		1kHz, R_L = 16Ω@ P_O = 20mW rms		-75dB 0.018		dB %
Power Supply Rejection Ratio	PSRR	20 to 20kHz, without supply decoupling		-40		dB
Clocks						
Crystal clock				24.576		MHz
BITCLK frequency				12.288		MHz
SYNC frequency				48.0		KHz

Note:

1. Harmonic distortion on the headphone output decreases with output power – see Figure 3.
2. SNR is the ratio of 0dB signal amplitude to noise floor with no signal present (all 0s input code to DACs).
3. ADC sampling capacitance allows the user to calculate the minimum external capacitance required for a stable ADC value.

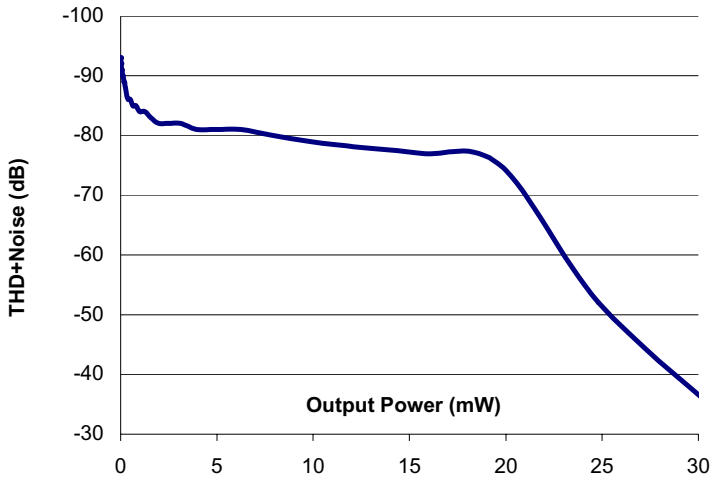


Figure 3 Distortion Versus Power on Headphone Outputs, using 32Ω Load and AVDD = HPVDD = 3.3V

POWER CONSUMPTION

MODE DESCRIPTION	PR0	PR1	PR2	PR3	PR4	PR5	PR6	EAPD	DIGITISER PD REG 78H (PRP)	RECORD MUX	CURRENT CONSUMPTION		
											AVDD (mA	DVDD (mA)	TOTAL POWER (mW)
Record and Playback													
Mic Record (note 1)	0	0	0	0	0	0	0	X	00	000L 000R	14.8	14.3	96
Other Input Record	0	0	0	0	0	0	0	X	00	001L 001R	17.7	14.3	105.6
Other Input Record PR6	0	0	0	0	0	0	1	X	00	001L 001R	16.3	14.3	101
Other Input Record PR6 and PR2	0	0	1	0	0	0	1	X	00	001L 001R	10.7	14.3	82.5
Other Input Record PR6 and PR3	0	0	0	1	0	0	1	X	00	001L 001R	0.5	14.1	48.2
Playback Only													
Low Power Playback (note 2)	1	0	1	0	0	0	0	X	00	001L 001R	5.5	11.5	56.1
Playback Only	1	0	0	0	0	0	0	X	00	001L 001R	11.1	11.5	74.6
Playback Only PR6	1	0	0	0	0	0	1	X	00	001L 001R	9.7	11.5	70
Playback Only PR6 and PR2	1	0	1	0	0	0	1	X	00	001L 001R	4.0	11.5	51.2
Playback Only PR6 and PR3	1	0	0	1	0	0	1	X	00	001L 001R	0.4	11.5	39.3
Record Only													
Mic Record (note 1)	0	1	0	0	0	0	0	X	00	000L 000R	12.9	13.3	86.5
Other Input Record	0	1	0	0	0	0	0	X	00	100L 100R	15.8	13.3	96
Other Input Record PR6	0	1	0	0	0	0	1	X	00	100L 100R	14.3	11.3	84.5
Other Input Record PR6 and PR2	0	1	1	0	0	0	1	X	00	100L 100R	7.2	13.3	67.7
Other Input Record PR6 and PR3	0	1	0	1	0	0	1	X	00	100L 100R	0.3	12.9	43.6
Power Down													
Power Down (note 3)	1	1	1	1	1	1	1	X	00	XXXL XXXR	0.0001	0.002	0.007
Pen Digitiser													
Pen Digitiser (Note 4)	1	1	1	1	0	1	1	X	11	XXXL XXXR	0.1	3.6	12.2

Notes:

1. When the ADC input mux is set to mic input to BOTH ADC channels, (SR2-0 and SL2-0 both set to '0'), one ADC is shared between both channels and the other is powered off to save current. The same digital data is output to both slots.
2. The POP bit (reg 20h) also needs to be set for this mode.
3. These values are recorded with no external clocks applied to the WM9705.
4. Pen active duty cycle is approximately 10%. Average analogue current consumption is approximately 10% of stated figure.

DETAILED TIMING DIAGRAMS

Test Characteristics:
AVDD = 3.3V, DVDD = 3.3V, AGND = 0V ……..T_A = 0°C to +70°C, unless otherwise stated.
All measurements are taken at 10% to 90% DVDD, unless otherwise stated. All the following timing information is guaranteed, not tested.

AC-LINK LOW POWER MODE

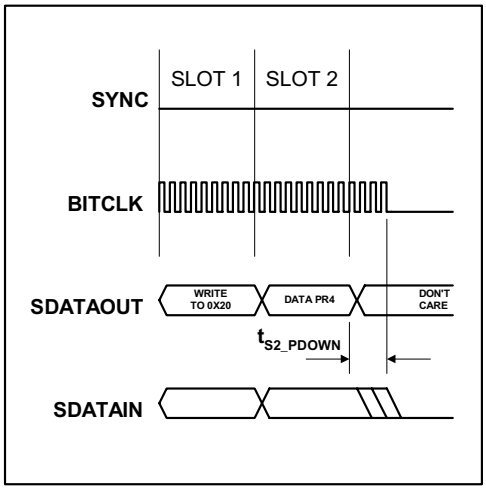


Figure 4 AC-Link Powerdown Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of slot 2 to BITCLK SDATAIN low	t_{S2_PDOWN}			1.0	µs

COLD RESET

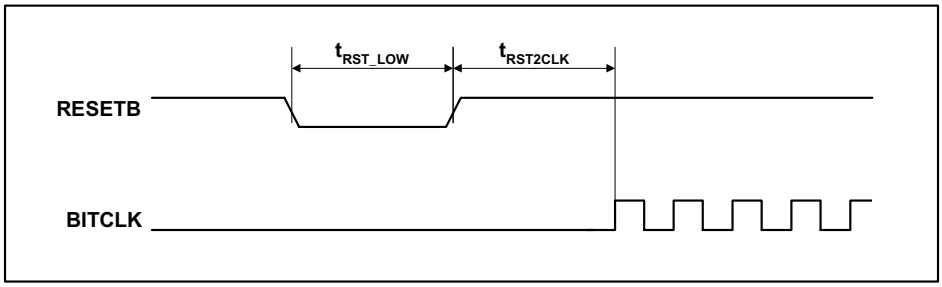


Figure 5 Cold Reset Timing

Note:
For correct operation SDATAOUT and SYNC must be held LOW for entire RESETB active low period otherwise the device may enter test mode. See AC'97 specification or Wolfson applications note WAN104 for more details.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t_{RST_LOW}	1.0			µs
RESETB inactive to BITCLK startup delay	$t_{RST2CLK}$	162.8			ns

WARM RESET

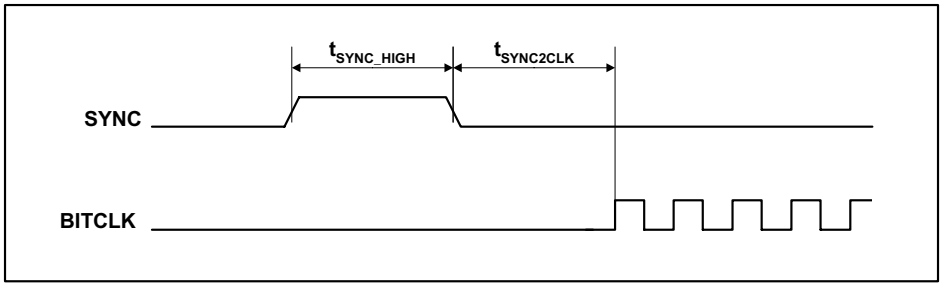


Figure 6 Warm Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC inactive to BITCLK startup delay	$t_{SYNC2CLK}$	162.4			ns

CLOCK SPECIFICATIONS

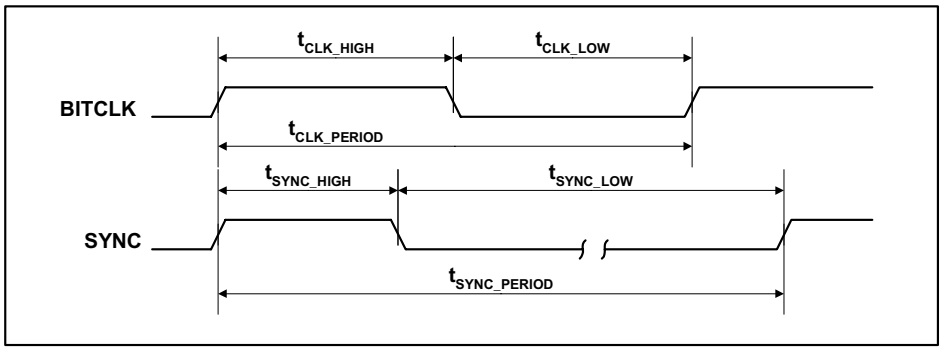


Figure 7 Clock Specifications (50pF External Load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK frequency			12.288		MHz
BITCLK period	t_{CLK_PERIOD}		81.4		ns
BITCLK output jitter				750	ps
BITCLK high pulse width (Note 1)	t_{CLK_HIGH}	36	40.7	45	ns
BITCLK low pulse width (Note 1)	t_{CLK_LOW}	36	40.7	45	ns
SYNC frequency			48.0		kHz
SYNC period	t_{SYNC_PERIOD}		20.8		µs
SYNC high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC low pulse width	t_{SYNC_LOW}		19.5		µs

Note:

Worst case duty cycle restricted to 45/55.

DATA SETUP AND HOLD (50PF EXTERNAL LOAD)

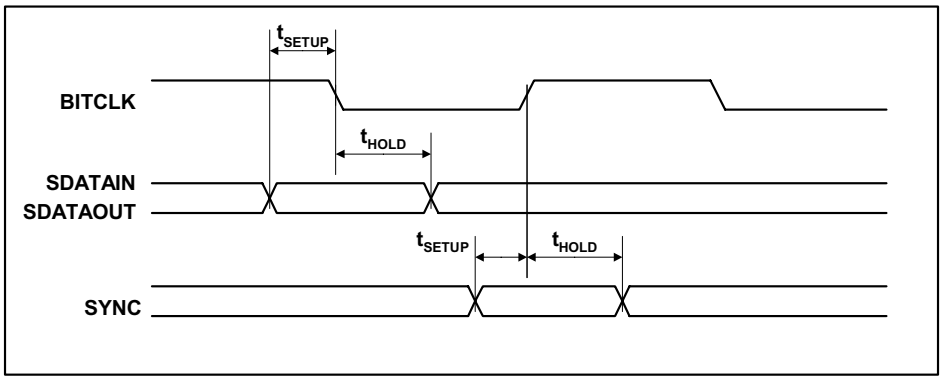


Figure 8 Data Setup and Hold (50pF External Load)

Note:

Setup and hold time parameters for SDATAIN are with respect to AC'97 Controller.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BITCLK	t_{SETUP}	10			ns
Hold from falling edge of BITCLK	t_{HOLD}	10			ns

SIGNAL RISE AND FALL TIMES

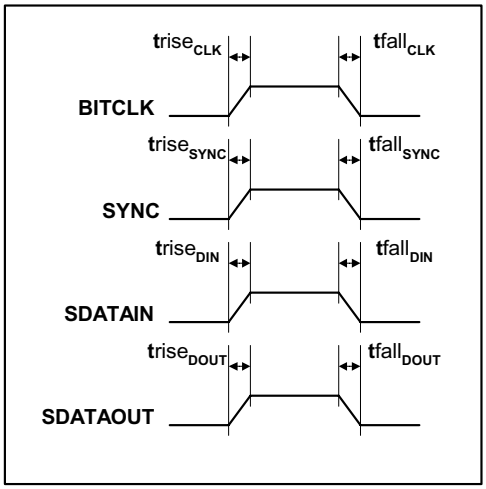


Figure 9 Signal Rise and Fall Times (50pF External Load)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK rise time	$trise_{CLK}$	2		6	ns
BITCLK fall time	$tfall_{CLK}$	2		6	ns
SYNC rise time	$trise_{SYNC}$	2		6	ns
SYNC fall time	$tfall_{SYNC}$	2		6	ns
SDATAIN rise time	$trise_{DIN}$	2		6	ns
SDATAIN fall time	$tfall_{DIN}$	2		6	ns
SDATAOUT rise time	$trise_{DOUT}$	2		6	ns
SDATAOUT fall time	$tfall_{DOUT}$	2		6	ns

DEVICE DESCRIPTION

INTRODUCTION

This specification describes the WM9710 audio codec, which is designed to be software and hardware compatible with the Intel AC'97 rev2.2 component specification. The device is a derivative of the basic AC'97 codec. Variable Rate Audio (VRA) is supported at rates defined in the Intel rev2.1 or rev2.2 specification, and a SPDIF output port is provided which may optionally be used to output the PCM DAC information to external processors.

WM9710 offers the following features:

Stereo Audio Codec with Intel specified VRA support of different audio sample rates

Optional SPDIF and I^2S audio outputs (SPDIF output may be hardware enabled so needing no driver support)

Headphone drive capability and optional auto detection of headset or headphone plug in

It is highly recommended that the Intel AC'97 rev2.2 specification be studied in parallel with this document: This specification can be downloaded from the Intel web site.

The WM9710 is fully operable on 3V or 5V or mixed 3/5V supplies, and is packaged in the industry standard 48pin TQFP package with 7mm body size.

AC'97 FEATURES

WM9710 implements the base set of AC'97 rev2.2 features, plus several enhancements:

All rev2.2 specified variable audio sample rates supported

3-D stereo enhancement feature.

Headphone support on HPOUT outputs (pins 39,41)

Primary/secondary codec operation by pin programming of CID0 pin

SPDIF audio output with rev2.2 compliant control set.

NON - AC'97 FEATURES

In addition to the AC'97 features offered, WM9710 also supports:

Headphone drive capability on MONO output, with extra signal routing switch PSEL, allowing PHONE input to be routed to MONO output

Extra switch HPND after the mixer allowing MIX without DAC signal to be output to headphone outputs, and so allowing DAC with no MIX to be output to LINE outputs.

I^2S audio output capability, in addition to SPDIF output, allowing support of an extra external audio DAC for multi-channel solutions. SPDIF output may be hardware enabled.

Option to route the stereo audio ADC output to the SPDIF and/or I^2S digital outputs

Auto-detect of headphones or headset plugged into the HPOUT headphone outputs, with internal routing of microphone signal from the headphone pin to the MIC1 input.

MPM switch allowing mix of DAC + mixer output onto MONOUT and independent mix of DAC + PHONE and/or PCBEEP onto LINEOUT or HPOUT.

Reset powerdown override – holding PWRUP/LRC (PIN 43) high in reset overrides the PR bits forcing the WM9710 into a low power mode.

3-D STEREO ENHANCEMENT

This device contains a stereo enhancement circuit, designed to optimise the listening experience when the device is used in a typical PC operating environment. That is, with a pair of speakers placed either side of the monitor with little spatial separation. This circuit creates a difference signal by differencing left and right channel playback data, then filters this difference signal using lowpass and highpass filters whose time constants are set using external capacitors connected to the CX3D pins 33 and 34. Typically the values of 100nF and 47nF set highpass and lowpass poles at about 100Hz and 1kHz respectively. This frequency band corresponds to the range over which the ear is most sensitive to directional effects.

The filtered difference signal is gain adjusted by an amount set using the 4-bit value written to Register 22h bits 3 to 0. Value 0h is disable, value Fh is maximum effect. Typically a value of 8h is optimum. The user interface would most typically use a slider type of control to allow the user to adjust the level of enhancement to suit the program material. Bit D13 3D in Register 20h is the overall 3D enable bit. The Reset Register 00h reads back the value 11000 in bits D14 to D10. This corresponds to decimal 24, which is registered with Intel as Wolfson Stereo Enhancement.

Note that the external capacitors setting the filtering poles applied to the difference signal may be adjusted in value, or even replaced with a direct connection between the pins. If such adjustments are made, then the amount of difference signal fed back into the main signal paths may be significant, and can cause large signals which may limit, distort, or overdrive signal paths or speakers. Adjust these values with care, to select the preferred acoustic effect. There is no provision for pseudo-stereo effects. Mono signals will have no enhancement applied (if the signals are in phase and of the same amplitude). Signals from the PCM DAC channels can have stereo enhancement applied. It can also be bypassed if desired. This function is enabled by setting the bit POP in Register 20h.

VARIABLE SAMPLE RATE SUPPORT

The DACs and ADCs on this device support all the recommended sample rates specified in the Intel AC'97 rev2.1 & rev2.2 specifications for audio rates. The default rate is 48kHz. If alternative rates are selected and variable rate audio is enabled (Register 2Ah, bit 0), the AC'97 interface continues to run at 48k words per second, but data is transferred across the link in bursts such that the net sample rate selected is achieved. It is up to the AC'97 Revision 2.1/2 compliant controller to ensure that data is supplied to the AC link, and received from the AC link, at the appropriate rate.

Variable rates are selected by writing to registers 2Ch (DAC) and 32h (ADC). ADC and DAC rates may be set independently, with left and right channels always at the same rate. The device supports on demand sampling. That is, when the DAC signal processing circuits need another sample, a sample request is sent to the controller which must respond with a data sample in the next frame it sends. For example, if a rate of 24kHz is selected, on average the device will request a sample from the controller every other frame, for each of the stereo DACs. Note that if an unsupported rate is written to one of the rate registers, the rate will default to the nearest rate supported. The Register will then respond, when interrogated, with the supported rate the device has defaulted to.

The WM9710 clocks will scale automatically dependent upon the MCLK frequency, where MCLK is not equal to 24.576MHz. With a 24MHz clock the BCLK frequency expected will be 12MHz and the sampling frequency (SYNC0 expected is BCLK/256 = 46.875kHz.

AUDIO SAMPLE RATE	CONTROL VALUE D15-D0
8000	1F40
11025	2B11
16000	3E80
22050	5622
32000	7D000
44100	AC44
48000	BB80

Table 1 Variable Sample Rates Supported

SPDIF OR I²S DIGITAL AUDIO DATA OUTPUT

The WM9710 SPDIF output may be enabled in hardware by holding pin 44 (SPEN) high when RESETB is taken high, or by writing to the SPDIF control bit in register 2Ah. If SPDIF pin 48 is pulled high at start-up by a weak pull-up (e.g. 100k), then SPDIF capability bit in register 28h is set to '0', i.e. no SPDIF capability. This allows for stuffing options, so that when SPDIF external components are not provided, the driver will see 'no SPDIF capability' and 'grey out' the relevant boxes in the control panel.

Additionally the digital audio may be output in I^2S format using pin 44 (SPEN) as the data output, and outputting a frame clock or LRCLK onto pin 43. The data is clocked onto pin 44 using the regular BITCLK at 256fs, which would also then be used as the MCLK if the data is taken to an external DAC. Operation in this mode is selected by setting bit I^2S in register 5Ch. A 64fs bitclk is also available and can be output on SPDIF by setting bit I2S64 in register 74h. Note that I^2S operation is only supported for 48kHz operation. Hardware selection of SPDIF operation by pulling pin SPEN 'hi' is compatible with I^2S operation, provided a weak pull-up (circa 100k) was used to hold SPEN high at start-up. The SPEN pin becomes I^2S data output pin when I^2S is enabled, and the weak pull-up on this pin is overdriven.

For both SPDIF and I^2S modes the data that is output may be sent from the WM9710 via the AC link in the same slots as normal DAC data or may be sent in different slots. The output slots that contain the SPDIF/I^2S data are selected by bits SPSA[1:0] in register 2Ah. WM9710 is compliant with AC'97 rev2.2 specification with regard to slot mapping; therefore the default mode of operation is to output SPDIF or I^2S data from the next data slots available after the audio data slots currently in use. Alternatively if required, data may be mapped from any of the available slots by selection using SPSA bits. The following table shows the default slot mapping for audio DACs and SPDIF/I^2S data: (further details in the register description section later).

SPEN STATE AT START-UP	CODEC ID (PIN 45 STRAPPING)	AUDIO DAC SLOT DEFAULT	SPDIF OR I^2S DATASLOT DEFAULT
'lo' (rev2.2 compliant)	'hi' = ID = 0 = primary	Slots 3 & 4 - front channels	Slots 7 & 8
'lo' (rev2.2 compliant)	'lo' = ID = 1 = secondary	Slots 7 & 8 – surround	Slots 6 & 9
'hi' (WM proprietary)	'hi' = ID = 0 = primary	Slots 3 & 4 - front channels	Slots 3 & 4
'hi' (WM proprietary)	'lo' = ID = 1 = secondary	Slots 7 & 8 – surround	Slots 3 & 4

Table 2 DAC and SPDIF Slot Mapping Defaults

However, an exception to the rev2.2 mapping table is made when SPDIF operation is enabled using the SPEN hardware enable pin (being held high at start-up): in this case SPDIF data is immediately output from the DAC primary slots 3 & 4. This allows for driver-less SPDIF operation, where the SPDIF or I^2S output is simply the data contained in the main audio DAC channels. Channel status and control bits output along with the SPDIF data are as set in the SPDIF control register 3Ah. If required SPDIF data channel slot mapping may be then changed by setting SPSA bits as required. See tables 18, 19 and 20 for further details.

A mode is provided where the output from the ADC is sent out as the SPDIF or I^2S data as above, rather than the data sent to the DACs over the AC link. This mode is enabled by setting bit ADCO in register 5Ch. ADC data continues to be sent via the AC link to the controller as normal.

WM9710 supports SPDIF and I^2S data only at the default 48kHz frame rate. Writing to SPSR bits in register 3Ah any value other than the default 48kHz rate will result in a fail to write, with the 48kHz value being returned on subsequent reads of these values.

PRIMARY/SECONDARY ID SUPPORT

WM9710 supports operation as either a primary or a secondary codec. Configuration of the device as either a primary or as a secondary, is selected by tying the CID0 pin 45 on the package. Fundamentally, a device identified as a primary (ID = 0, CID0 = 'hi') produces BITCLK as an output, whereas a secondary (any other ID) must be provided with BITCLK as an input. This has the obvious implication that if the primary device on an AC link is disabled, the secondary devices cannot function. The AC'97 Revision 2.2 specification defines that the CID0 pin has inverting sense, and are provided with internal weak pull ups. Therefore, if no connections are made to the CID0 pin, then the pin pull hi and an ID = 0 is selected, i.e. primary. External connect to ground (with pull-down from 0 to 10kΩ) will select codec ID = '1'.

PIN 45 CID0	ID SELECTED	PRIMARY OR SECONDARY	BITCLK
NC or pull-up	0	Primary	Output
Ground	1	Secondary	Input

Table 3 Codec ID Selection

HEADPHONE DRIVE AND HEADSET AUTODETECT

Headphone drive capability is provided on HPOUT (pins 39 and 41) and on MONOOUT (pin 37).

Headphones of impedance typically from 16Ω upwards may be connected to these pins. AC coupling with an appropriately sized capacitor is recommended for removal of the mid-rail DC pedestal present on these outputs. AC'97 rev2.2 specification recommends 32Ω headphones; if a headphone is connected for use as a headset, where the stereo ear-pieces are driven in parallel, then each capsule must be of minimum 32Ω impedance.

In many applications it is desirable to be able to connect either a stereo headphone to the headphone output pins, or a mono headset, comprising ear-piece(s) and a microphone. The microphone signal is sent via the tip connected wire of the typical 3-wire jack. In this event it is desirable to be able to auto-detect the connection of either the headphone or the headset (with microphone). The main characteristic of the headset and microphone compared to the headphone is that the microphone impedance is typically much higher than the headphone capsule (assuming a typical moving coil headphone). Because of this it is possible to connect a weak pull-up to the tip connection of the headphone jack.

When a headphone is connected the low impedance to ground of the headset pulls down the DC level to near ground. If a headset with microphone is plugged in, the high impedance of the microphone does not pull down the DC level on the tip connection, the DC on this pin now rising to near positive supply. This change in DC level is detected, so allowing detection of change from headphone to microphone, (or nothing plugged in of course). When this event is detected, the headphone amplifier that drives the tip connection is turned off, and the signal on this pin is routed instead to the MIC1 input as a microphone input.

This auto-detect comparator is enabled by setting bit HSCMP. The pull-up current is enabled by setting bit MPUEN in register 5Ch and also toggles the interrupt signal on the HSDET pin. When bit HSDT is set the mic1 input is connected to a comparator with a threshold set at mid-rail. When the comparator output is low, then the headphone driver is enabled. When the comparator output goes high (that is the pull-up current multiplied by the external impedance to ground on the mic1 pin is greater than mid-rail), the headphone amplifier is turned off and the mic1 signal is taken internally from the headphone output pin (39).

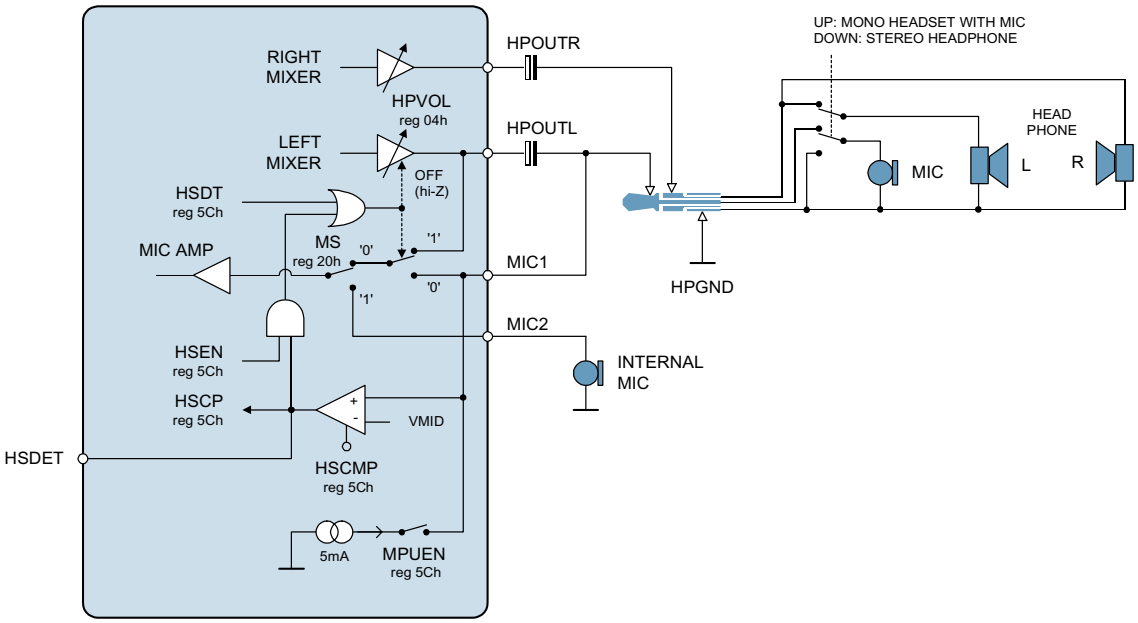


Figure 10 Headset Autodetect

Figure 10 shows this function schematically. The output signal from the comparator is accessible by reading bit HSCP in register 5Ch. Auto detect may be used by setting HSEN bit, or external control by using the HSDT bit which is an over-ride that forces the headset tri-state and microphone path switching function to occur.

This function would allow, for example, a stereo headphone to be used that had a microphone in the connecting lead, and a switch. The switch changes the headphone into a mono headset with microphone connected via the tip connection on the jack. If used in a product such as an MP3 capable phone it would allow the user to switch from headphone use to headset use by simply switching a single switch in the headphone cable, so at the same time answering or initiating telephone calls. It may also be possible to use the pull-up current to provide so called 'phantom power' to dynamic microphones with appropriate choice of microphone.

DATA SLOT MAPPING

DAC data and SPDIF data sent to the device, ADC data sent from the device, can be optionally mapped into alternative slots under control of slot mapping bits located as follows:

SLOT MAPPING DATA TYPE	CONTROL BITS	REGISTER LOCATION
DAC data	DSA[1,0]	28h
SPDIF data	SPSA[1,0]	2Ah
ADC data	ASS[1,0]	5Ch (non-AC'97 feature)

Table 4 Data Slot Mapping Control

Default values and functional behavior are further described in the Serial Interface Register Map description. DAC slot mapping defaults are in Table 2.

AC-LINK DIGITAL SERIAL INTERFACE PROTOCOL

A digital interface has been provided to control the WM9710 and transfer data to and from it. This serial interface is compatible with the Intel AC'97 specification.

The main control interface functions are:

- Control of analogue gain and signal paths through the mixer
- Bi-directional transfer of ADC and DAC words to and from AC'97 controller
- Selection of power-down modes

The WM9710 incorporates a 5-pin digital serial interface that links it to the AC'97 controller. AC-link is a bi-directional, fixed rate, serial PCM digital stream. It handles multiple input and output audio streams, as well as control register accesses employing a time division multiplexed (TDM) scheme. The AC-link architecture divides each audio frame into 12 outgoing and 12 incoming data streams, each with 20-bit sample resolution. With a minimum required DAC and ADC resolution of 16-bits, AC'97 may also be implemented with 18 or 20-bit DAC/ADC resolution, given the headroom that the AC-link architecture provides. The WM9710 provides support for 18-bit audio operation.

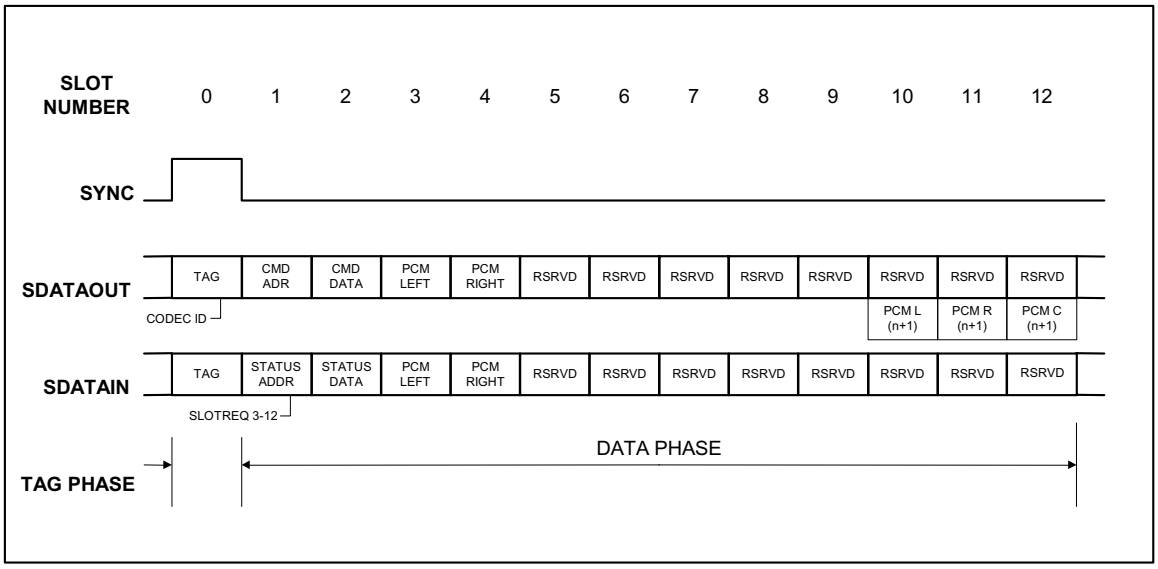


Figure 9 AC'97 Standard Bi-Directional Audio Frame

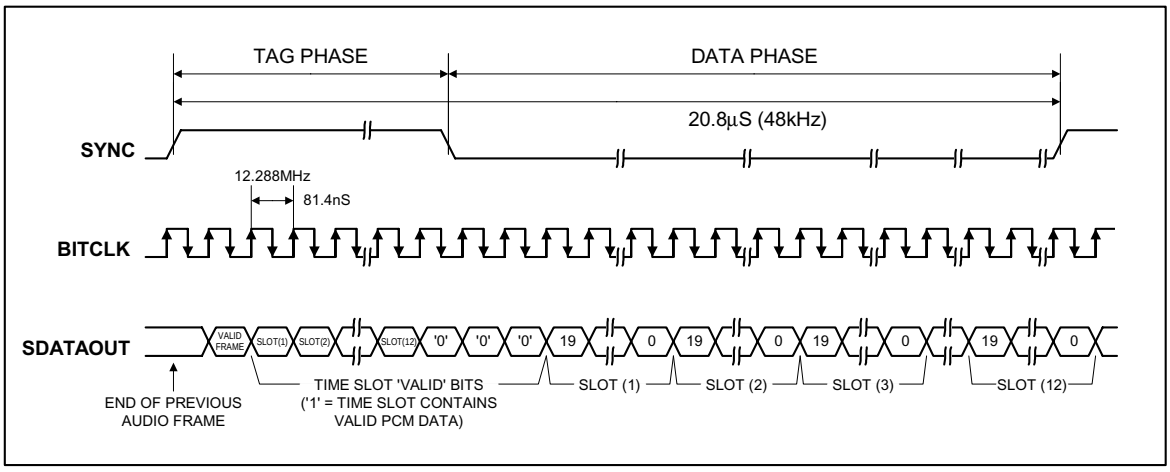


Figure 10 AC-link Audio Output Frame

The datastreams currently defined by the AC'97 specification include:

PCM playback - 2 output slots	2-channel composite PCM output stream
PCM record data - 2 input slots	2-channel composite PCM input stream
Control - 2 output slots	Control Register write port
Status - 2 input slots	Control Register read port
Optional modem line codec output - 1 output slot	Modem line codec DAC input stream
Optional modem line codec input – 1 input slot	Modem line codec ADC output stream
Optional dedicated microphone input - 1 input slot	Dedicated microphone input stream in support of stereo AEC and/or other voice applications.

Synchronisation of all AC-link data transactions is signalled by the WM9710 controller. The WM9710 drives the serial bit clock onto AC-link, which the AC'97 controller then qualifies with a synchronisation signal to construct audio frames.

SYNC, fixed at 48kHz, is derived by dividing down the serial clock (BITCLK). BITCLK, fixed at 12.288MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BITCLK. The receiver of AC-link data, (WM9710 for outgoing data and AC'97 controller for incoming data), samples each serial bit on the falling edges of BITCLK.

The AC-link protocol provides for a special 16-bit time slot (slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A 1 in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is tagged invalid, it is the responsibility of the source of the data, (the WM9710 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0s during that slot's active time.

SYNC remains high for a total duration of 16 BITCLKs at the beginning of each audio frame.

The portion of the audio frame where SYNC is high is defined as the Tag Phase. The remainder of the audio frame where SYNC is low is defined as the Data Phase. Additionally, for power savings, all clock, sync, and data signals can be halted. This requires that the WM9710 be implemented as a static design to allow its Register contents to remain intact when entering a power savings mode.

PLAY MASTER VOLUME REGISTERS (INDEX 02H, 04H AND 06H)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), Register 04h controls the stereo headphone out, and Register 06h controls the mono volume output. Each step corresponds to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

ML4 to ML0 is for left channel level, MR4 to MR0 is for the right channel and MM4 to MM0 is for the mono out channel.

Support for the MSB of the volume level is not provided by the WM9710. If the MSB is written to, then the WM9710 detects when that bit is set and sets all 4 LSBs to 1s. Example: If the driver writes a 1xxxxx the WM9710 interprets that as x11111. It will also respond when read with x11111 rather than 1xxxxx, the value written to it. The driver can use this feature to detect if support for the 6th bit is there or not.

The default value of both the mono and the stereo registers is 8000h (1000 0000 0000 0000), which corresponds to 0dB gain with mute on.

MUTE	MX4...MX0	FUNCTION
0	0 0000	0dB attenuation
0	0 0001	1.5dB attenuation
0	1 1111	46.5dB attenuation
1	x xxxx	∞dB attenuation

Table 5 Volume Register Function

The Headphone out has an additional 6dB boost, selectable by setting HPB in register 74h.

PC BEEP REGISTER (INDEX 0AH)

This controls the level for the PC-beep input. Each step corresponds to approximately 3dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB.

WM9710 defaults to the PC-beep path being muted, so an external speaker should be provided within the PC to alert the user to power on self-test problems.

MUTE	PV3...PV0	FUNCTION
0	0000	0dB attenuation
0	1111	45dB attenuation
1	xxxx	∞dB attenuation

Table 6 PC-beep Register Function

ANALOGUE MIXER INPUT GAIN REGISTERS (INDEX 0CH - 18H AND 72H)

This controls the gain/attenuation for each of the analogue inputs and mixer PGA. Each step corresponds to approximately 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞dB. Note that the gain for the VID and AUX input channels is fixed at 0dB. Writes to the gain control bits for these channels are ignored, and the value of readback for these registers is always the default, with the exception of the mute bit 15 which may be written to and read from.

The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0dB gain with mute on.

MUTE	GX4...GX0	FUNCTION
0	00000	+12dB gain
0	01000	0dB gain
0	11111	-34.5dB gain
1	xxxxx	-∞dB gain

Table 7 Mixer Gain Control Register Function

REGISTER 0EH (MIC VOLUME REGISTER)

This has an extra bit that is for a 20dB boost. When bit 6 is set to 1 the 20dB boost is on. The default value is 8008h, which corresponds to 0dB gain with mute on.

RECORD SELECT CONTROL REGISTER (INDEX 1AH)

Used to select the record source independently for right and left (see Table 8). The default value is 0000h, which corresponds to Mic in. Setting Bit ADCNDAC in Register 5Ch selects a stereo mix WITHOUT DAC when (5 x 2 – 5 x 0) is 5.

SR2 TO SR0	RIGHT RECORD SOURCE	SL2 TO SL0	LEFT RECORD SOURCE
0	Mic	0	Mic
1	CD in (R)	1	CD in (L)
3	Line in (R)	4	Line in (L)
4	Stereo mix (R)	5	Stereo mix (L)
5	Mono mix	6	Mono mix
6	Phone	7	Phone

Table 8 Record Select Register Function

RECORD GAIN REGISTERS (INDEX 1CH)

1Ch sets the stereo input record gain with each step corresponding to 1.5dB. The MSB of the register is the mute bit. When this bit is set to 1, the level for both channels is set at -∞dB.

The default value is 8000h, which corresponds to 0dB gain with mute on.

MUTE	GX3...GX0	FUNCTION
0	1111	+22.5dB gain
0	0000	0dB gain
1	xxxxx	-∞dB gain

Table 9 Record Gain Register Function

GENERAL PURPOSE REGISTER (INDEX 20H)

This register is used to control several miscellaneous functions of the WM9710.

Below is a summary of each bit and its function. Only the POP, 3D, MIX, MS and LPBK bits are supported by the WM9710. The MS bit controls the Mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements. The function default value is 0000h which is all off.

BIT	FUNCTION
POP	PCM out path and mute, 0 = pre-3D, 1 = post-3D
3D	3D stereo enhancement on/off, 1 = on
MIX	Mono output select 0 = Mix, 1 = Mic
MS	Mic select 0 = Mic1, 1 = Mic2
LPBK	ADC/DAC loopback mode

3D CONTROL REGISTER (INDEX 22H)

This register is used to control the centre and/or depth of the 3D stereo enhancement function built into the AC'97 component. Only the depth bits DP0 to 3 have effect in the WM9710.

DP3…DP0	DEPTH
0	0%
1	
-	
8	Typical value
-	
15	100%

Table 10 3D Control Register

POWERDOWN CONTROL/STATUS REGISTER (INDEX 26H)

This read/write register is used to program power-down states and monitor subsystem readiness. The lower half of this register is read only status, a 1 indicating that the subsection is ready. Ready is defined as the subsection able to perform in its nominal state. When this register is written the bit values that come in on AC-link will have no effect on read bits 0- 7.

When the AC-link Codec Ready indicator bit (SDATAIN slot 0, bit 15) is a 1 it indicates that the AC-link and the WM9710 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any, are ready.

Note that the normal default condition of WM9710 when RESETB is applied is 'all active'. However, if pin 43 (PWRUP/LRC) is pulled 'hi' during RESETB active, all PR bits are overridden and the device enters a low power mode. This allows a low power standby mode to be entered without writing to the device, a condition that is desirable for example, if batteries are changed in a PDA. The state of pin 43 is latched on the rising edge of RESETB and if the pin is 'hi' then the WM9710 will remain in low power mode until register 26h is written to.

READ BIT	FUNCTION
REF	VREFs up to nominal level
ANL	Analogue mixers, etc ready
DAC	DAC section ready to accept data
ADC	ADC section ready to transmit data

Table 11 Powerdown Status Register Function

The Powerdown modes are as follows. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADCs and DACs only. PR6 powers down just the stereo Line Level output headphone amps on pins 39/41.

The WM9710 also includes a low power DAC to headphone mode, whereby resetting PR1and PR6 enables the DAC and the path from the DAC to HPOUTL/R without having to power up the main mixer (PR2). The POP bit (reg 20h) also needs to be set for this mode. The headphone amplifier on the MONO output pin in not powered down by PR6, rather by PR2 or alternatively may be enabled by setting MONOEN in register 74h.

WRITE BIT	FUNCTION
PR0	PCM in ADCs and input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analogue mixer Powerdown (VREF still on)
PR3	Analogue mixer Powerdown (VREF off)
PR4	Digital interface (AC-link) Powerdown (external clock off)
PR5	Internal clock disable
PR6	HP amp Powerdown
EAPD	External amplifier Powerdown

Table 12 Powerdown Control Register Function

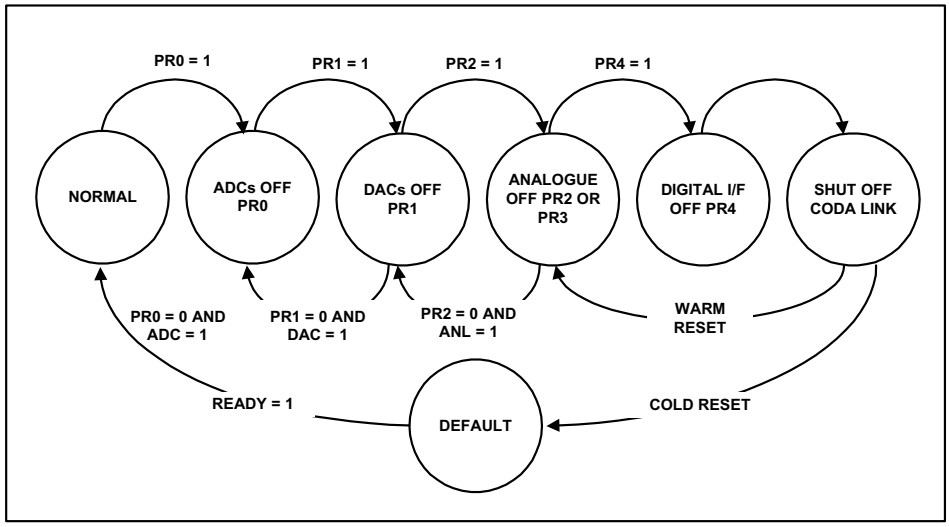


Figure 11 An Example of the WM9710 Powerdown/Powerup Flow

Figure 11 illustrates one example procedure to do a complete Powerdown of the WM9710. From normal operation sequential writes to the Powerdown Register are performed to Powerdown the WM9710 a piece at a time. After everything has been shut off (PR0 to PR3 set), a final write (of PR4) can be executed to shut down the WM9710's digital interface (AC-link).

The part will remain in sleep mode with all its registers holding their static values. To wake up the WM9710, the AC'97 controller will send a pulse on the sync line issuing a warm reset. This will restart the WM9710's digital interface (resetting PR4 to 0). The WM9710 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers, as a cold reset will set them to their default states. When a section is powered back on, the Powerdown Control/Status Register (index 26h) should be read to verify that the section is ready (i.e. stable) before attempting any operation that requires it.

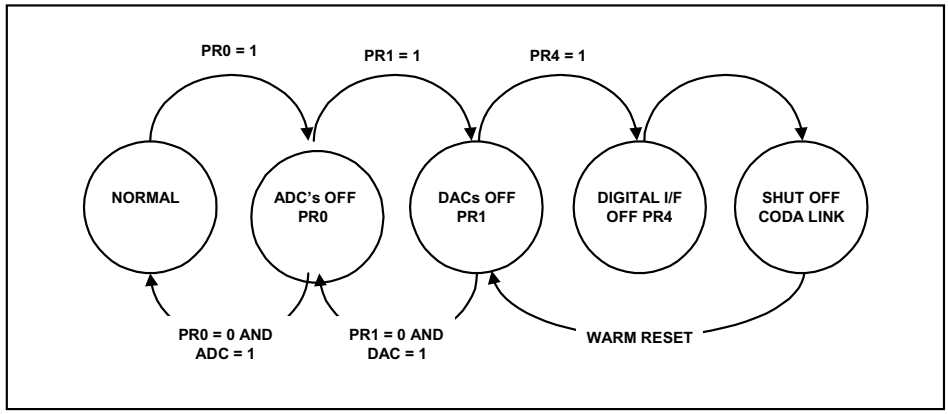


Figure 12 The WM9710 Powerdown Flow with Analogue Still Active

Figure 12 illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINEIN source) through WM9710 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analogue mixer is never shut down.

Note that in order to go into ultimate low power mode, PR4 and PR5 are required to be set which turns off the oscillator circuit. Asserting SYNC resets the PR4 and PR5 bit and re-starts the oscillator in the same way as the AC link is restarted.

REGISTER 28H – EXTENDED AUDIO ID

The Extended Audio ID register is a read only register that identifies which extended audio features are supported (in addition to the original AC'97 features identified by reading the reset register at index 00h). A non zero value indicates the feature is supported.

DATA BIT	FUNCTION	VALUE
VRA	Variable rate audio support	1
DRA	Double rate audio support	0
SPDIF	SPDIF transmitter supported	'1' = supported
VRM	Variable rate Mic ADC support	0
DSA0	DAC slot mapping control	See table below
DSA1	DAC slot mapping control	See table below
CDAC	Centre DAC support	0
SDAC	Surround DAC support	0
LDAC	LFE DAC support	0
AMAP	Slot mapping support for Codec ID	1
REV0	Revision number	1
REV1	Revision number	0
ID0	Codec configuration – pin 45 value	0 (Inverse of level at pin 45)
ID1	Codec configuration – fixed in WM9710	0

Table 13 Extended Audio ID Register

DSA1, DSA0	DAC SLOT MAPPING
00	Slots 3 & 4
01	Slots 7 & 8
10	Slots 6 & 9
11	Slots 10 & 11

Table 14 DAC Slot Mapping

DAC slot mapping to slots 7 and 8 or slots 6 and 9 cannot be used in variable rate mode (VRA=1) for sample rates other than 48kHz.

REGISTER 2AH – EXTENDED AUDIO STATUS AND CONTROL REGISTER

The Extended Audio Status and Control Register is a read/write register that provides status and control of the extended audio features. Note that SPDIF slot mapping default varies according to codec pin configuration. See Table 2.

DATA BIT	FUNCTION	READ/WRITE
VRA	Enables variable rate audio mode	Read/write
SPDIF	SPDIF transmitter enable	Read/write
SPSA0	SPDIF slot assignment	Read/write
SPSA1	SPDIF slot assignment	Read/write
SPCV	SPDIF validity bit	Read

Table 15 Extended Audio Status and Control Register

SPSA0, SPSA1	SPDIF SLOT MAPPING
00	Slots 3 & 4
01	Slots 7 & 8
10	Slots 6 & 9
11	Slots 10 & 11

Table 16 SPDIF Slot Mapping

REGISTER 2Ch AND 32h – AUDIO SAMPLE RATE CONTROL REGISTERS

These registers are read/write registers that are written to, to select alternative sample rates for the audio PCM converters. Default is the 48kHz rate. Note that only Revision 2.2 recommended rates are supported by the WM9710, selection of any other unsupported rates will cause the rate to default to the nearest supported rate, and the supported rate value to be latched and so read back. Sample rate is entered in binary form to the appropriate register.

REGISTERS 3AH – SPDIF CONTROL REGISTER

Register 3Ah is a read/write register that controls SPDIF functionality and manages bit fields propagated as channel status (or sub-frame in the V case). With the exception of V, this register should only be written to when the SPDIF transmitter is disabled (SPDIF bit in register 2Ah is '0'). Once the desired values have been written to this register, the contents should be read back to ensure that the sample rate in particular is supported, then SPDIF validity bit SPCV in register 2Ah should be read to ensure the desired configuration is valid. Only then should the SPDIF enable bit in register 2Ah be set. This ensures that control and status information start up correctly at the beginning of SPDIF transmission. WM9710 only supports an SPDIF sample rate of 48kHz.

CONTROL BIT	FUNCTION
PRO	Professional; '0' indicates consumer, '1' indicates professional
AUDIB	Non-audio; '0' indicates data is PCM, '1' indicates non-PCM format (eg DD or DTS)
COPY	Copyright; '0' indicates copyright is not asserted, '1' indicates copyright
PRE	Pre-emphasis; '0' indicates not pre-emphasis, '1' indicates 50/15us pre-emphasis
CC[6-0]	Category code; programmed as required by user
L	Generation level; programmed as required by user
V	Validity bit; '0' indicates frame valid, '1' indicates frame not valid

Table 17 SPDIF Control Register

VENDOR SPECIFIC REGISTERS (INDEX 5Ah - 7Ah)

These registers are vendor specific. Do not write to these registers unless the Vendor ID register has been checked first to ensure that the controller knows the source of the AC '97 component.

MIXER MUTE PATH (INDEX 5AH)

Bit 4 (MPM) is used to disable the path between the main input mixer and the lineout mixer. Setting this bit to 1, breaks the connection and allows the following combinations:

DAC + PHONE + PCBEEP to line out / headphone out

When writing to this register all bits (except MPM) must be written as a 0 or device function can not be guaranteed.

VENDOR SPECIFIC MODE CONTROL (INDEX 5CH)

Register 5Ch is a vendor specific control register used to control the function of non-AC'97 specified functions. This register defaults to all special features 'disabled' i.e. All zeros.

CONTROL BIT	FUNCTION
AMUTE	Indicates automute has been detected in the audio DAC (all '0' data) – read only
HSCP	Headset detect comparator output – read only
MPUEN	Mic pull up enable
MHPZ	Mono headphone tristate enable
PSEL	PHONE to MONO path switch enable
HSDT	Overrides Headset detect comparator, forcing left headphone amp to tristate
HSEN	Headset auto-detect enable
HPND	Headphone with no DAC enable
AMEN	Automute enable bit
I^2S	I^2S data output enable
ADCNDAC	ADC no DAC path enable
ADCO	ADC to SPDIF and/or I^2S output
HPF	ADC high pass filter disable;
HSCMP	Headset comparator enable bit
ASS1	ADC slot map control
ASS0	ADC slot map control

Table 18 Vendor Specific Control Register 5Ch

AMUTE indicates automute state has been detected. This is a read-only bit. 1 = automute detected.

HSCP is a read only bit, indicating headset detected. It is the output from the headset autodetect comparator. 0 = headset detected.

MPUEN enables a 5mA (typ) pull up current on the MIC1 input pin, which when a headset microphone of high impedance is plugged in, causes the MIC1 pin to pull up to above Vmid, and be detected. 1 = enable.

MHPZ tristates the MONO headphone driver output buffer. 1 = tristate.

PSEL enables the switch from PHONE input to MONO output; see block diagram. 1 = enable.

HSDT overrides the headset auto-detect comparator, forcing the left headphone output to tristate and the HPLOUTL pin to be used as a headset microphone input path to the mic1 preamplifier input. 1 = autodetect comparator override.

HSEN enables headset auto-detect function. HSCMP enables the headset detect comparator. 1 = enable.

HPND enables the switch which outputs only the analog mixer output to the HPHONE outputs, without the DAC signal being summed in. See block diagram. 1 = enable.

AMEN enables the DAC automute function, which detects zero data on both dac channels and auto-mutes the outputs under this condition. 1 = enable.

Bit I^2S enables I^2S output, sending an LRCLK to pin 43 (PWRUP/LRC) and I^2S data to the SPEN/I^2S pin (pin 44). BITCLK is used to clock out the data. Only 48kHz data is supported. 1 = enable.

ADCNDAC selects input to the ADC from before the point where the DAC signal is summed in. 1 = select.

Bit ADCO is used to select data from the internal ADCs to be output as SPDIF or I^2S data on these pins rather than the data from the selected AC link slot. 1 = select.

HPF turns off the digital high pass filter in the ADC output when set to '1'.

ASS1, ASS0 are ADC slot mapping control bits. See table below. Default is slots 3 and 4.

ASS1, ASS0	ADC SLOT MAPPING (L/R)
00	Slots 3 & 4
01	Slots 7 & 8
10	Slots 6 & 9
11	Slots 10 & 11

Table 19 ADC Slot Mapping Control

VENDOR SPECIFIC GAIN CONTROL REGISTER (INDEX 72H)

This register controls the gain and mute functions applied to the mixer path. This PGA is not accommodated in the Intel specification, but is required in order to allow the option of simultaneous recording of the mixer output and playback of DAC signals. The function is as for the other mixer PGA's. However, the default value of the register is not-muted. If it is not used it will be transparent to the user. Normally this reigster would be used in collaboration with bit ADCNDAC in register 5Ch, allowing recording of the analog mix, manipulation in the digital domain by an external DSP, then playback through the DACs on the WM9710.

VENDOR SPECIFIC ADDITIONAL FUNCTIONALITY (INDEX 74H)

HPB boosts the headphone output by 6dB. 1 = 6dB boost enabled.

I2S64 enables a 64fs bitclk output on SPDIF for i^2s data output. 1 = enabled.

MONOEN enables the mono output independently of PR2 (MIXER Powerdown). This allows the DAC to MONOUT path to be powered up by resetting PR1 and setting MONOEN while the Mixer is powered down (PR2 set), providing a lower power mode when the mixer function is not required.

VENDOR SPECIFIC ADDITIONAL FUNCTIONALITY (INDEX 78H)

The PHIZ bit in register 78h enables the PHONE and PCBEEP input pins. By default, these pins are disconnected from the audio mixer (PHIZ=0). All other bits in register 78h should be set to 0 at all times. When PHIZ=0, PHONE and PCBEEP are high impedance inputs.

BIT	FUNCTION
PHIZ	PHONE and PCBEEP input enable; 0 = disabled, 1 = enabled

VENDOR ID REGISTERS (INDEX 7CH & 7EH)

These registers are for specific vendor identification if so desired. The ID method is Microsoft's Plug and Play Vendor ID code. The first character of that ID is F7 to F0, the second character S7 to S0, and the third T7 to T0. These three characters are ASCII encoded. The REV7 to REV0 field is for the Vendor Revision number. In the WM9710 the vendor ID is set to WML5.

Wolfson is a registered Microsoft Plug and Play vendor.

SERIAL INTERFACE REGISTER MAP

The following table shows the function and address of the various control bits that are loaded and read through the serial interface.

Reg	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6150h
02h	Master volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	HPHONE volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master volume mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PCBEEP volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV2	PV0	X	8000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line in volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM out volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Rec select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Rec gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	DP1	DP0	0000h
26h	Power/down control status	APD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Ext'd audio ID	ID1	ID0	X	X	REV1	REV0	AMAP	LDAC	SDAC	CDAC	DSA1	DSA0	VRM	SPDIF	DRA	VRA	0605h
2Ah	Ext'd audio stat/ctrl	X	X	X	X	X	SPCV	X	X	X	X	SPSA1	SPSA0	X	SPDIF	X	VRA	0000h
2Ch	Audio DAC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	Audio ADC rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
3Ah	SPDIF control	V	0	1	0	L	CC6	CC5	CC4	CC3	CC2	CC1	CC0	PRE	COPY	UDIB	PRO	2000h
5Ah	Mixer Path Mute	0	0	0	0	0	0	0	0	0	0	0	MPM	0	0	0	0	0000h
5Ch	Add. Function control	AMUTE	HSCP	PUEN	MHPZ	PSEL	HSEN	HSDT	HPND	AMEN	I²S	ADCN DAC	ADCO	HPF	HS CMP	ASS1	ASS0	0000h
72h	Front mixer volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	0808h
74h	Add. Function	X	X	X	X	X	X	X	X	X	X	X	X	HPB	I2S64	X	MONOEN	0000h
78h	Add. Function	0	0	0	0	0	0	0	0	0	PHIZ	0	0	0	0	0	0	0000h
7Ch	Vendor ID1	F7	F6	F5	F4	F3	F2	F1	F0	S7	S6	S5	S4	S3	S2	S1	S0	574Dh
7Eh	Vendor ID2	T7	T6	T5	T4	T3	T2	T1	T0	Rev7	Rev6	Rev5	Rev4	Rev3	Rev2	Rev1	Rev0	4C05h

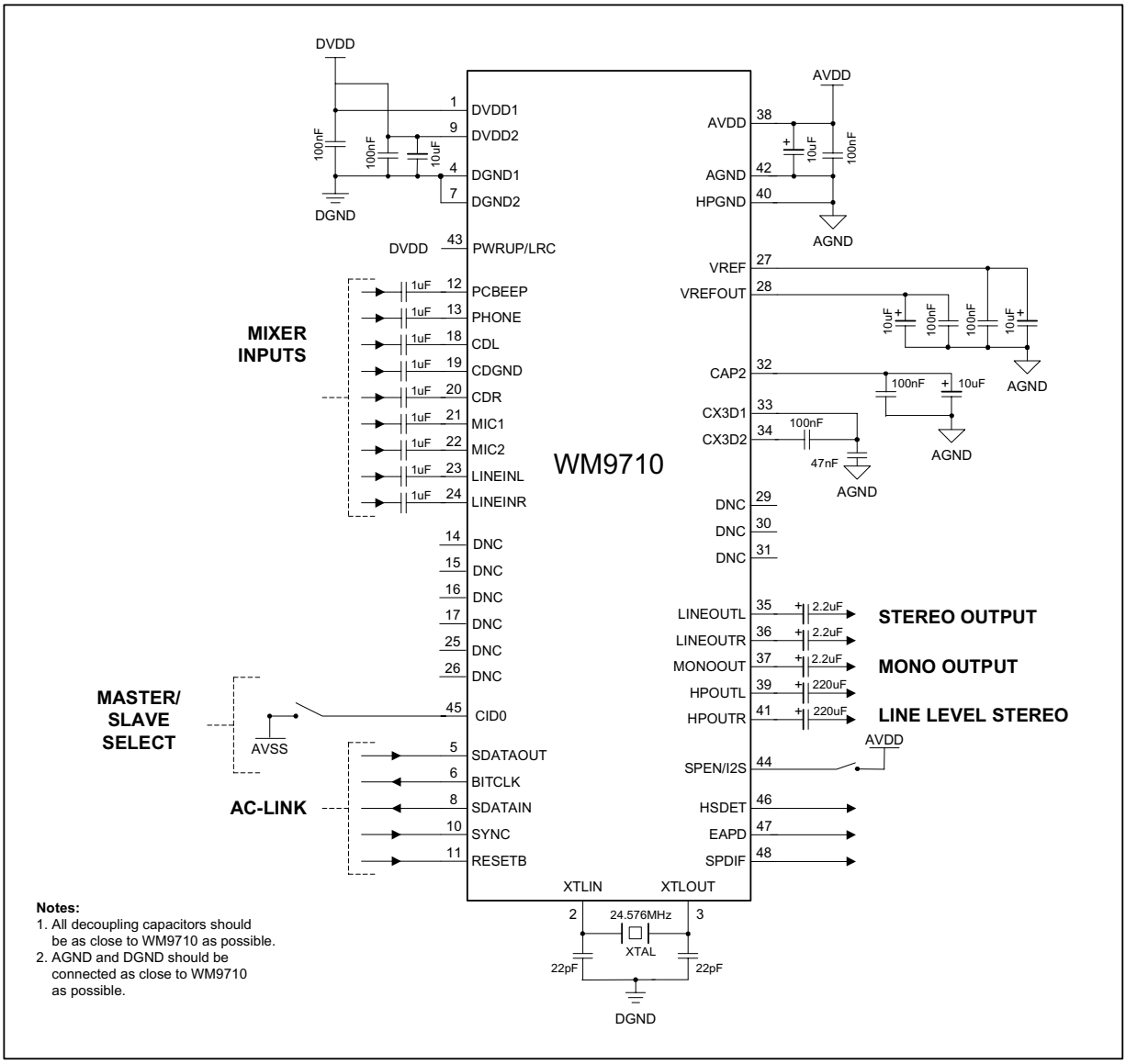
Table 20 Serial Interface Register Map Description

Note:

1. Default values of register 28h and 2Ah depend on whether the device is a primary or secondary, and whether SPDIF capability is enabled by pulling pin 44 SPEN high. The conditions shown are for a primary codec with SPDIF capability.

2. When writing to register 5Ah all bits except MPM (bit 4) must be written as 0, otherwise device function can not be guaranteed.

RECOMMENDED EXTERNAL COMPONENTS

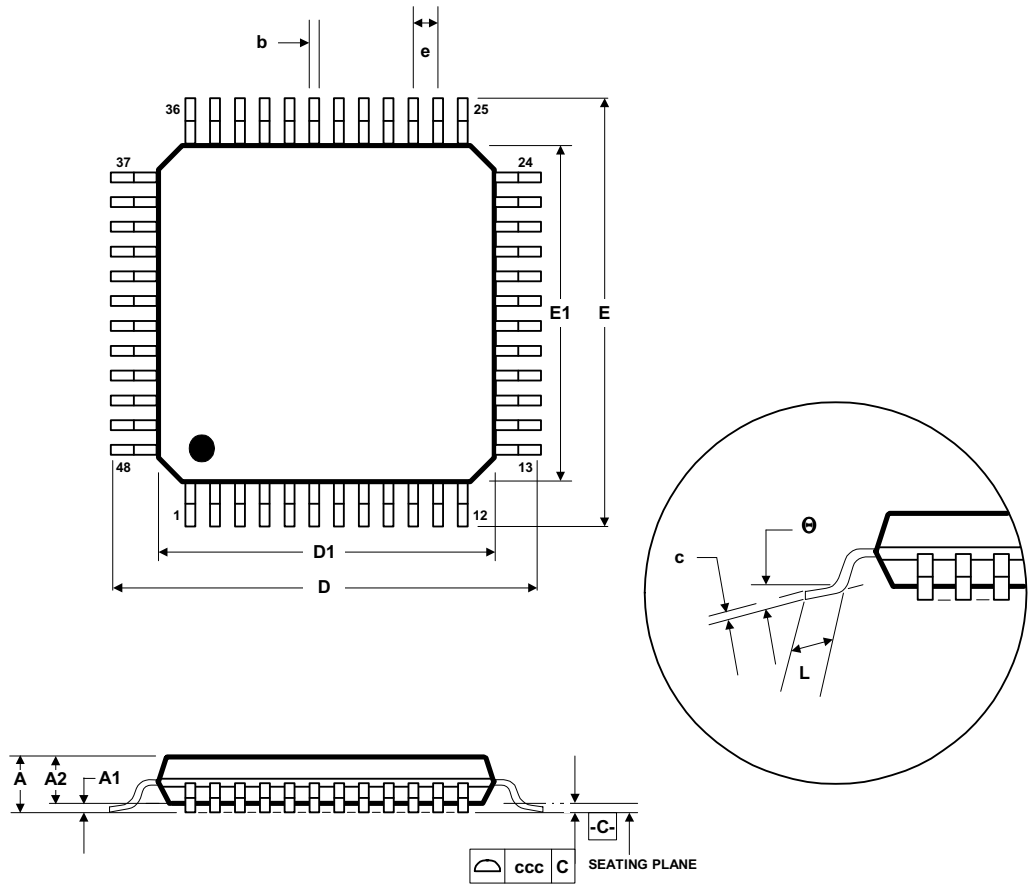


Notes:
1. All decoupling capacitors should be as close to WM9710 as possible.
2. AGND and DGND should be connected as close to WM9710 as possible.

Figure 13 External Components Diagram

PACKAGE DIMENSIONS – TQFP

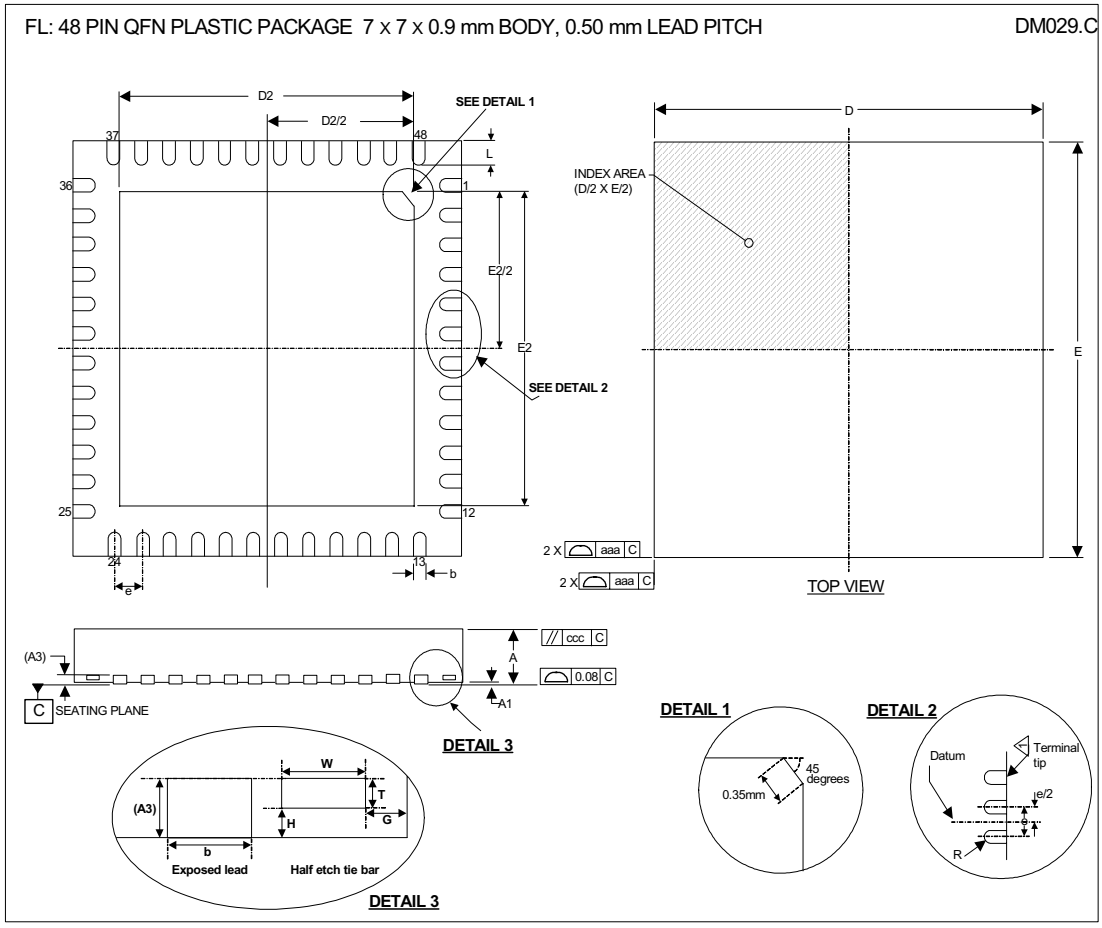
FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

PACKAGE DIMENSIONS – QFN



Symbols	Dimensions (mm)			
	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0	0.02	0.05	
A3		0.20 REF		
b	0.18	0.25	0.30	1
D		7.00 BSC		
D2	5.00	5.15	5.25	
E		7.00 BSC		
E2	5.00	5.15	5.25	
e		0.5 BSC		
G		0.213		
H		0.1		
L	0.30	0.4	0.50	
T		0.1		
W		0.2		
Tolerances of Form and Position				
aaa	0.15			
bbb	0.10			
ccc	0.10			
REF	JEDEC, MO-220, VARIATION VKKD-2			

NOTES:
1. **DIMENSION b APPLIED TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 mm AND 0.30 mm FROM TERMINAL TIP.**
2. **ALL DIMENSIONS ARE IN MILLIMETRES**
3. **THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-002.**
4. **COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.**
5. **THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.**

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