



WS57C128FB

HIGH SPEED 16K x 8 CMOS EPROM

KEY FEATURES

- **Very Fast Access Time**
— 35 ns
- **Low Power Consumption**
- **EPI Processing**
— Latch-up Immunity Up to 200 mA
- **Standard EPROM Pinout**
- **DIP and Surface Mount Packaging Available**

GENERAL DESCRIPTION

The WS57C128FB is a High Performance 128K UV Erasable Electrically Programmable Read Only Memory. It is manufactured with an advanced CMOS technology which enables it to operate at Bipolar speeds while consuming only 90 mA.

Two major features of the WS57C128FB are its Low Power and High Speed. These features make it an ideal solution for applications which require fast access times, low power, and non-volatility. Typical applications include systems which do not utilize mass storage devices and/or are board space limited.

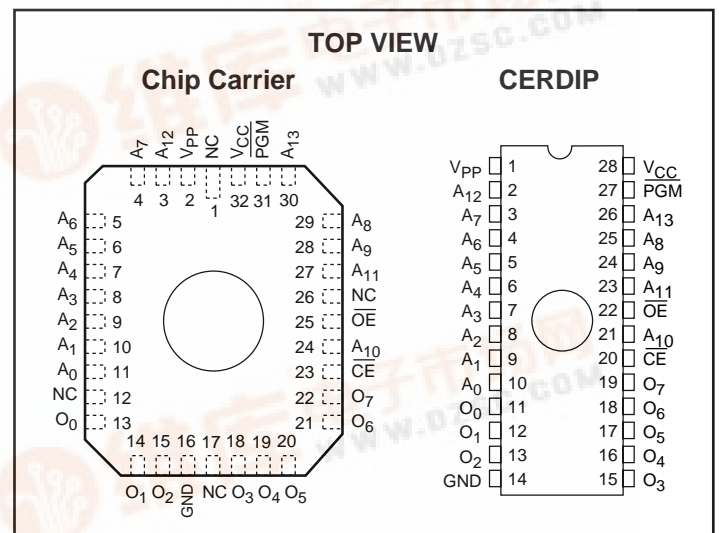
The WS57C128FB is configured in the standard EPROM pinout which provides an easy upgrade path for systems which are currently using standard EPROMs. The EPROMs are available in both 600 Mil DIP packages, and both J-leaded and leadless surface mount packages.

MODE SELECTION

| MODE \ PINS | PGM | CE | OE | V _{PP} | V _{CC} | OUTPUTS |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| Read | X | V _{IL} | V _{IL} | V _{CC} | V _{CC} | D _{OUT} |
| Output Disable | X | X | V _{IH} | V _{CC} | V _{CC} | High Z |
| Standby | X | V _{IH} | X | V _{CC} | V _{CC} | High Z |
| Program | V _{IL} | V _{IL} | V _{IH} | V _{PP} | V _{CC} | D _{IN} |
| Program Verify | V _{IH} | V _{IL} | V _{IL} | V _{PP} | V _{CC} | D _{OUT} |
| Program Inhibit | X | V _{IH} | X | V _{PP} | V _{CC} | High Z |

X can be V_{IL} or V_{IH}.

PIN CONFIGURATION



PRODUCT SELECTION GUIDE

| PARAMETER | WS57C128FB-35 | WS57C128FB-45 | WS57C128FB-55 | WS57C128FB-70 |
|---------------------------|---------------|---------------|---------------|---------------|
| Address Access Time (Max) | 35 ns | 45 ns | 55 ns | 70 ns |
| Chip Select Time (Max) | 35 ns | 45 ns | 55 ns | 70 ns |
| Output Enable Time (Max) | 20 ns | 25 ns | 25 ns | 25 ns |

ABSOLUTE MAXIMUM RATINGS*

| | |
|--|-----------------|
| Storage Temperature..... | –65° to + 150°C |
| Voltage on any Pin with Respect to Ground | –0.6V to +7V |
| V _{PP} with Respect to Ground..... | –0.6V to + 13V |
| ESD Protection..... | >2000V |

***NOTICE:**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING RANGE

| RANGE | TEMPERATURE | V _{CC} |
|------------|-----------------|-----------------|
| Commercial | 0°C to +70°C | +5V ± 10% |
| Industrial | –40°C to +85°C | +5V ± 10% |
| Military | –55°C to +125°C | +5V ± 10% |

DC READ CHARACTERISTICS Over Operating Range with V_{PP} = V_{CC}

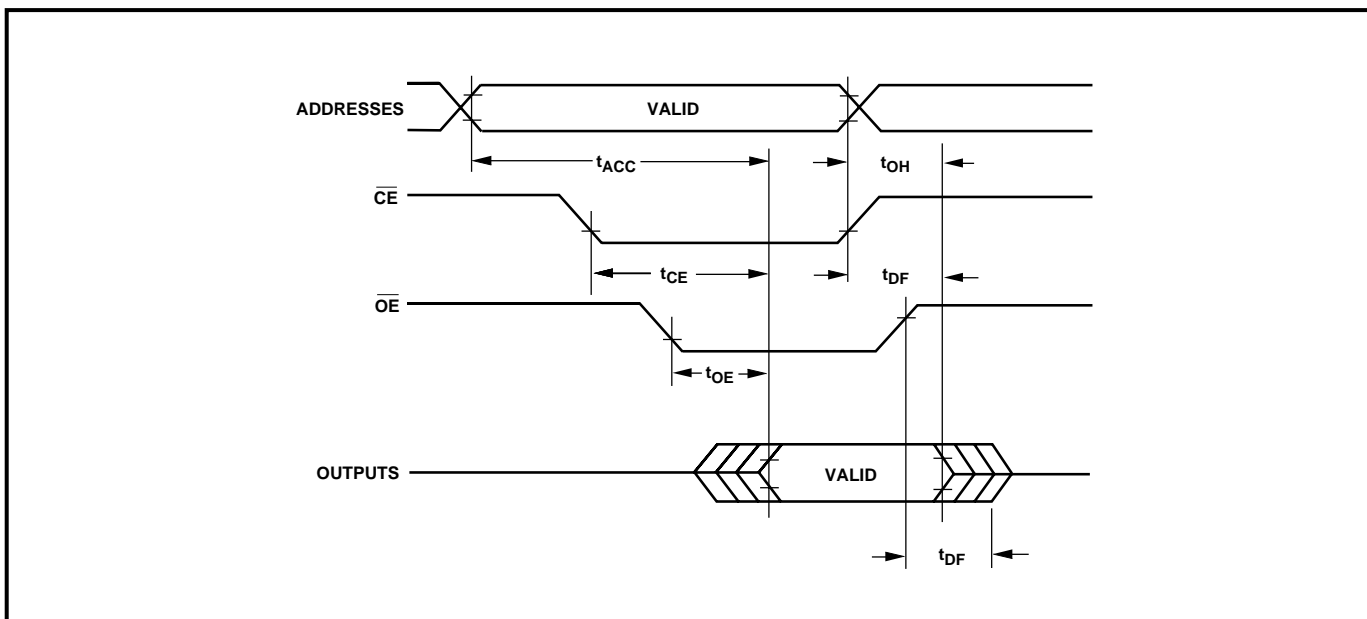
| SYMBOL | PARAMETER | TEST CONDITIONS | MIN | MAX | UNITS |
|------------------|--|---------------------------------------|-----------------------|-----------------------|-------|
| V _{IL} | Input Low Voltage | (Note 5) | –0.1 | 0.8 | V |
| V _{IH} | Input High Voltage | (Note 5) | 2.0 | V _{CC} + 0.3 | V |
| V _{OL} | Output Low Voltage | I _{OL} = 16 mA | | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = –4 mA | 2.4 | | V |
| I _{SB1} | V _{CC} Standby Current (CMOS) | (Notes 1 and 3) | | 500 | µA |
| I _{SB2} | V _{CC} Standby Current (TTL) | (Notes 2 and 3) | | 15 | mA |
| I _{CC1} | V _{CC} Active Current (CMOS) | (Notes 1 and 4) Outputs Not Loaded | Comm'l | 30 | mA |
| | | | Industrial | 40 | mA |
| | | | Military | 40 | mA |
| I _{CC2} | V _{CC} Active Current (TTL) | (Notes 2 and 4) Outputs Not Loaded | Comm'l | 50 | mA |
| | | | Industrial | 60 | mA |
| | | | Military | 60 | mA |
| I _{PP} | V _{PP} Supply Current | V _{PP} = V _{CC} | | 100 | µA |
| V _{PP} | V _{PP} Read Voltage | | V _{CC} – 0.4 | V _{CC} | V |
| I _{LI} | Input Leakage Current | V _{IN} = 5.5V or Gnd | –10 | 10 | µA |
| I _{LO} | Output Leakage Current | V _{OUT} = 5.5 V or Gnd | –10 | 10 | µA |

NOTES: 1. CMOS inputs: GND ± 0.3V or V_{CC} ± 0.3V.
2. TTL inputs: V_{IL} ≤ 0.8V, V_{IH} ≥ 2.0V.
3. Add 1 mA/MHz for A.C. power component.

4. Add 4 mA/MHz for A.C. power component.
5. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise.
Do not attempt to test these values without suitable equipment.

AC READ CHARACTERISTICS Over Operating Range with V_{PP} = V_{CC}

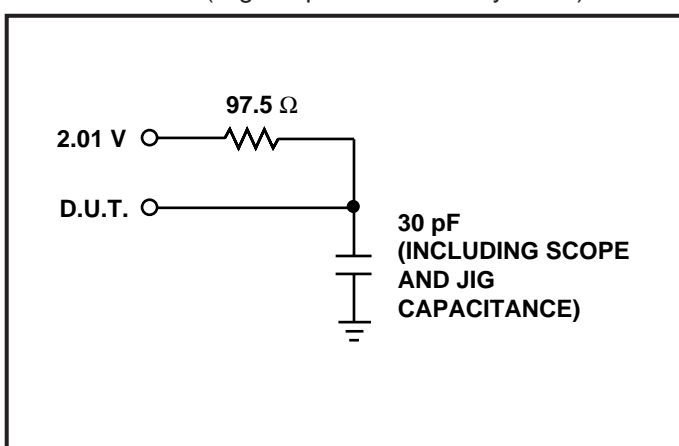
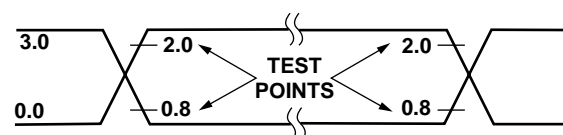
| PARAMETER | SYMBOL | 57C128FB-35 | | 57C128FB-45 | | 57C128FB-55 | | 57C128FB-70 | | UNITS |
|--|------------------|-------------|-----|-------------|-----|-------------|-----|-------------|-----|-------|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| Address to Output Delay | t _{ACC} | | 35 | | 45 | | 55 | | 70 | ns |
| $\overline{\text{CE}}$ to Output Delay | t _{CE} | | 35 | | 45 | | 55 | | 70 | |
| $\overline{\text{OE}}$ to Output Delay | t _{OE} | | 20 | | 25 | | 25 | | 25 | |
| Output Disable to Output Float | t _{DF} | | 20 | | 25 | | 25 | | 25 | |
| Address to Output Hold | t _{OH} | 0 | | 0 | | 0 | | 0 | | |

AC READ TIMING DIAGRAM**CAPACITANCE**⁽⁶⁾ $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$

| SYMBOL | PARAMETER | CONDITIONS | TYP ⁽⁷⁾ | MAX | UNITS |
|-----------|----------------------|------------------------|--------------------|-----|-------|
| C_{IN} | Input Capacitance | $V_{IN} = 0\text{ V}$ | 4 | 6 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0\text{ V}$ | 8 | 12 | pF |
| C_{VPP} | V_{PP} Capacitance | $V_{PP} = 0\text{ V}$ | 18 | 25 | pF |

NOTES: 6. This parameter is only sampled and is not 100% tested.

7. Typical values are for $T_A = 25^\circ\text{C}$ and nominal supply voltages.

TEST LOAD (High Impedance Test Systems)**A.C. TESTING INPUT/OUTPUT WAVEFORM**

A.C. testing inputs are driven at 3.0 V for a logic "1" and 0.0 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0".

NOTE: 8. Provide adequate decoupling capacitance as close as possible to this device to achieve the published A.C. and D.C. parameters. A 0.1 microfarad capacitor in parallel with a 0.01 microfarad capacitor connected between V_{CC} and ground is recommended. Inadequate decoupling may result in access time degradation or other transient performance failures.

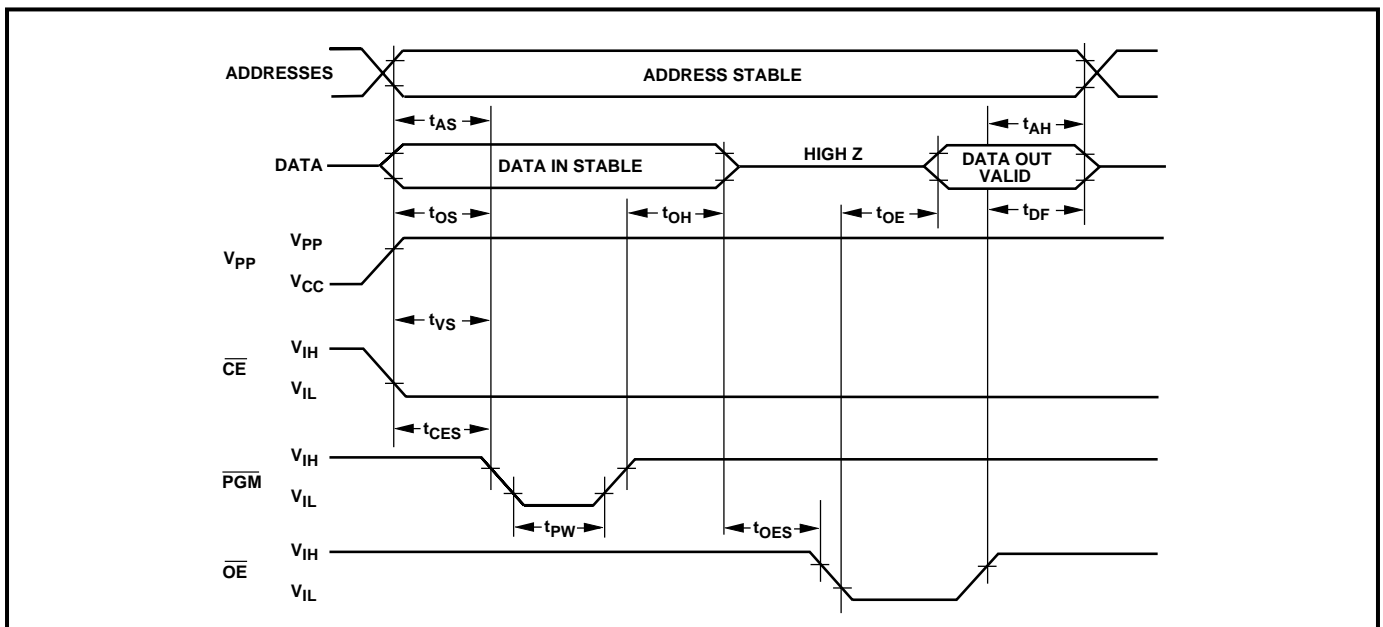
PROGRAMMING INFORMATION**DC CHARACTERISTICS** ($T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.75 \pm 0.25\text{ V}$)

| SYMBOLS | PARAMETER | MIN | MAX | UNITS |
|----------|---|-----|-----|---------------|
| I_{LI} | Input Leakage Current ($V_{IN} = V_{CC}$ or Gnd) | -10 | 10 | μA |
| I_{PP} | V_{PP} Supply Current During Programming Pulse ($\overline{CE} = \overline{PGM} = V_{IL}$) | | 60 | mA |
| I_{CC} | V_{CC} Supply Current | | 30 | mA |
| V_{OL} | Output Low Voltage During Verify ($I_{OL} = 16\text{ mA}$) | | 0.4 | V |
| V_{OH} | Output High Voltage During Verify ($I_{OH} = -4\text{ mA}$) | 2.4 | | V |

- NOTE:**
- V_{CC} must be applied either coincidentally or before V_{PP} and removed either coincidentally or after V_{PP} .
 - V_{PP} must not be greater than 13 volts including overshoot. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from 5 volts to 12.5 volts or vice-versa.
 - During power up the PGM pin must be brought high ($\geq V_{IH}$) either coincident with or before power is applied to V_{PP} .

AC CHARACTERISTICS ($T_A = 25 \pm 5^\circ\text{C}$, $V_{CC} = 6.25\text{ V} \pm 0.25\text{ V}$, $V_{PP} = 12.75 \pm 0.25\text{ V}$)

| SYMBOLS | PARAMETER | MIN | TYP | MAX | UNITS |
|-----------|------------------------------------|-----|-----|-----|---------------|
| t_{AS} | Address Setup Time | 2 | | | μs |
| t_{CES} | Chip Enable Setup Time | 2 | | | μs |
| t_{OES} | Output Enable Setup Time | 2 | | | μs |
| t_{OS} | Data Setup Time | 2 | | | μs |
| t_{AH} | Address Hold Time | 0 | | | μs |
| t_{OH} | Data Hold Time | 2 | | | μs |
| t_{DF} | Chip Disable to Output Float Delay | 0 | | 130 | ns |
| t_{OE} | Data Valid From Output Enable | | | 130 | ns |
| t_{VS} | V_{PP} Setup Time | 2 | | | μs |
| t_{PW} | \overline{PGM} Pulse Width | 100 | | 200 | μs |

PROGRAMMING WAVEFORM

ORDERING INFORMATION

| PART NUMBER | SPEED (ns) | PACKAGE TYPE | PACKAGE DRAWING | OPERATING TEMPERATURE RANGE | WSI MANUFACTURING PROCEDURE |
|------------------|------------|---------------------|-----------------|-----------------------------|-----------------------------|
| WS57C128FB-35D | 35 | 28 Pin CERDIP, 0.6" | D2 | Comm'l | Standard |
| WS57C128FB-45D | 45 | 28 Pin CERDIP, 0.6" | D2 | Comm'l | Standard |
| WS57C128FB-45DMB | 45 | 28 Pin CERDIP, 0.6" | D2 | Military | MIL-STD-883C |
| WS57C128FB-45J | 45 | 32 Pin PLDCC | J4 | Comm'l | Standard |
| WS57C128FB-45L | 45 | 32 Pin CLDCC | L3 | Comm'l | Standard |
| WS57C128FB-55CMB | 55 | 32 Pad CLLCC | C2 | Military | MIL-STD-883C |
| WS57C128FB-55D | 55 | 28 Pin CERDIP, 0.6" | D2 | Comm'l | Standard |
| WS57C128FB-55DMB | 55 | 28 Pin CERDIP, 0.6" | D2 | Military | MIL-STD-883C |
| WS57C128FB-70D | 70 | 28 Pin CERDIP, 0.6" | D2 | Comm'l | Standard |
| WS57C128FB-70DM | 70 | 28 Pin CERDIP, 0.6" | D2 | Military | Standard |
| WS57C128FB-70DMB | 70 | 28 Pin CERDIP, 0.6" | D2 | Military | MIL-STD-883C |

NOTE: 12. The actual part marking will not include the initials "WS."

PROGRAMMING/ALGORITHMS/ERASURE/PROGRAMMERS

**REFER TO
PAGE 5-1**

The WS57C128FB is programmed using Algorithm D shown on page 5-9.