Features

-
-
- **Low Noise - Less Than 15μV_{P-P}**
- **Low Power Dissipation -**

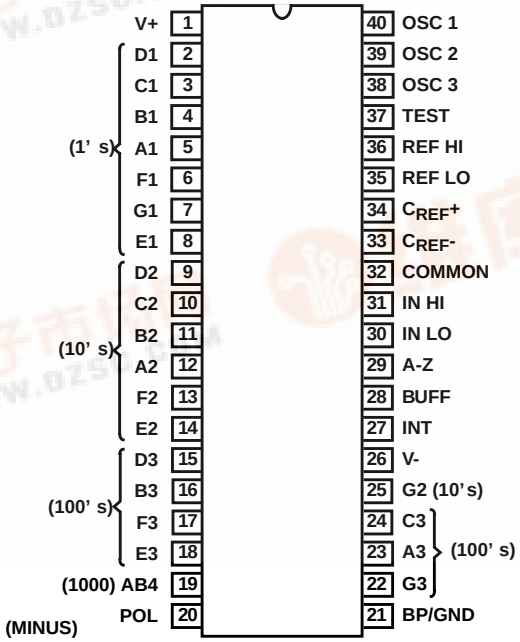
Description

are high performance, low power, $3^1/_2$ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the 7107 will directly drive an instrument size light emitting diode (LED) display.

7107 bring together a combination of high accuracy, versatility, and true economy.

Ordering Information

PART NO.	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.



Absolute Maximum Ratings

Supply Voltage

WS7106, V+ to V-.....15v

WS7107, V+ to GND.....6V

WS7107, V_ to GND..... ....-9V

Analog Input Voltage (Either Input) (Note 1)V+ to V-

Reference Input Voltage (Either Input)V+ to V-

Clock Input

WS7106TEST to V+

WS7107GND to V+

Thermal Information

Thermal Resistance (typical, Note 2) θ_{JA}(℃/W)

PDIP Package..... 50

Maximum Junction Temperature..... .....150℃

Maximum Storage Temperature Range.....-65℃ to 150℃

Operating Conditions

Temperature Range.....0℃ to 70℃

CAUTION: Stresses above those listed in "absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation

Of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Notes:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100μA
2. Θ_{JA} Is measured with the component mounted on an evaluation PC on board in fee air.

Electrical specifications (Note 3)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMACE					
Zero Input Reading	V_{IN}=0.0V, FULL Scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error	-V_{IN}=+V_{IN}=200mV Difference in Reading for Equal Positive and Negative Inputs Near Full Scale	-1	0.2	+1	Counts
Linearity	Full Scale = 200mV or Full Scale = 2V Maximum Deviation from Best Straight Line Fit (note 6)	-1	0.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, Full Scale = 200mv(Note 6)	-	50	-	μV/V
End Power Supply Character V+ Supply Current	V_{IN} = 0 (Does Not Include LED Current for WS7107	-	0.5	1.8	mA
End Power Supply Character V- Supply Current	WS7107 Only	-	0.5	1.8	mA
COMMON Pin Analog Common Voltage	25kΩ Between Common and Positive Supply (With Respect to + Supply)	2.4	3.0	3.2	V
Noise (P_K-P_K Value not exceeded 95% of time)	V_{IN}=0V Full Scale=200mV		15		uV_{P-P}
Input Leakage Current	V_{IN}=0V		1	10	pA
Analog COMMON Temperature Coefficient	25K between Common and V+ 0℃-70℃		60	75	ppm/℃
Scale Factor Temperature Coefficient	V_{IN}=199mV 0℃-70℃Ext. ref. 0ppm/℃		60	75	ppm/℃
Zero Reading Drift	V_{IN}=0℃V-70℃		0.2	1	uV/℃

DISPLAY DRIVER WS7106 ONLY

Peak-to-Peak Segment Drive Voltage Peak-to-Peak Backplane Drive Voltage	V+ = to V- = 9V (Note 5)	4	5	6	V

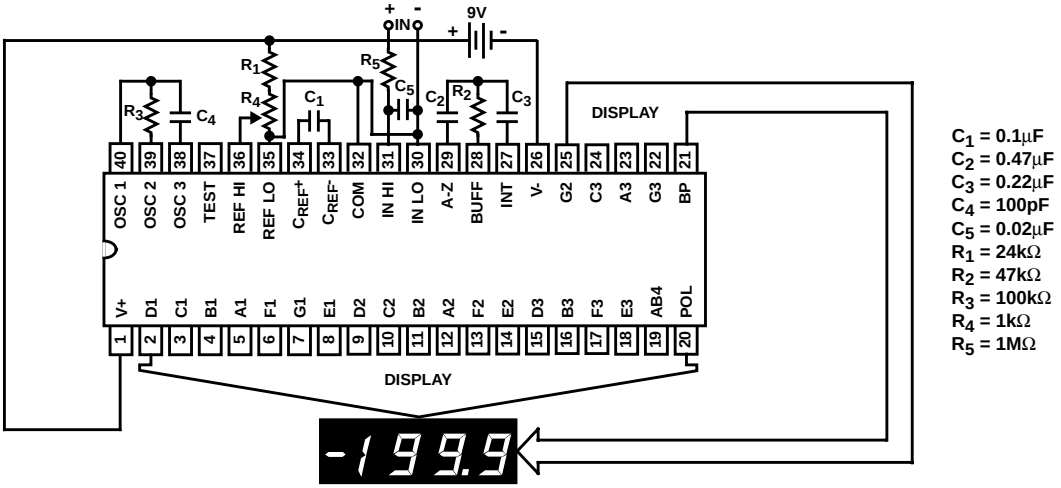
Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Segment Sinking Current (Except Pins 19 and 20)	V+ = 5V, Segment Voltage = 3V	5	8	-	mA
Pin 19 Only		10	16	-	mA
Pin 20 Only		4	7	-	mA

NOTES:

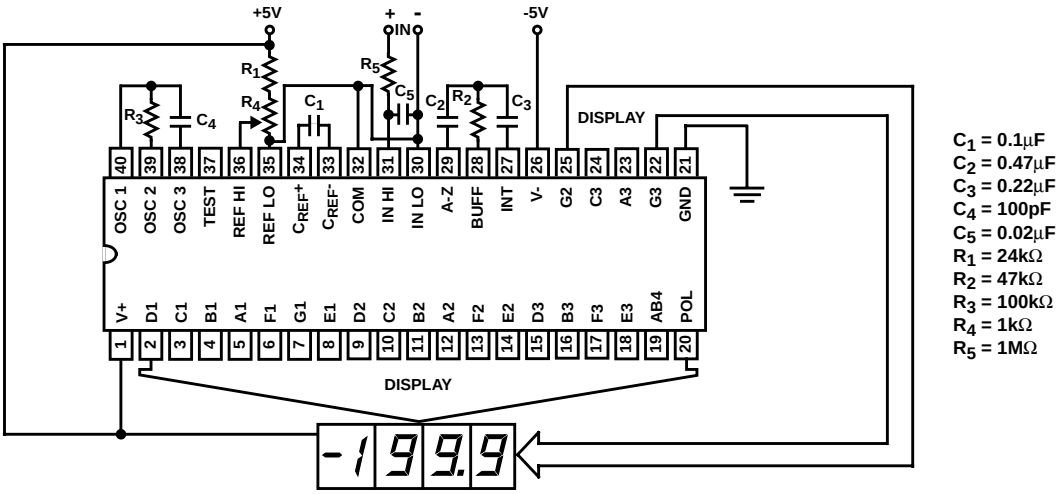
3. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Typical Applications and Test Circuits



C_1 = 0.1µF
C_2 = 0.47µF
C_3 = 0.22µF
C_4 = 100pF
C_5 = 0.02µF
R_1 = 24kΩ
R_2 = 47kΩ
R_3 = 100kΩ
R_4 = 1kΩ
R_5 = 1MΩ

7106 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE



C_1 = 0.1µF
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R_3 = 100kΩ
R_4 = 1kΩ
R_5 = 1MΩ

7107 TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**

  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50k\Omega$
  f_{OSC} (Typ) = 48kHz

- **OSCILLATOR PERIOD**

  $t_{OSC} = RC/0.45$

- **INTEGRATION CLOCK FREQUENCY**

  $f_{CLOCK} = f_{OSC}/4$

- **INTEGRATION PERIOD**

  $t_{INT} = 1000 \times (4/f_{OSC})$

- **60/50Hz REJECTION CRITERION**

  t_{INT}/t_{60Hz} or t_{INT}/t_{60Hz} = Integer

- **OPTIMUM INTEGRATION CURRENT**

  $I_{INT} = 4\mu A$

- **FULL SCALE ANALOG INPUT VOLTAGE**

  V_{INFS} (Typ) = 200mV or 2V

- **INTEGRATE RESISTOR**

  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

  $$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

  $$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

- **V_{INT} MAXIMUM SWING:**

  $(V- + 0.5V) < V_{INT} < (V+ - 0.5V)$, V_{INT} (Typ) = 2V

- **DISPLAY COUNT**

  $$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**

  $t_{CYC} = t_{CL0CK} \times 4000$
  $t_{CYC} = t_{OSC} \times 16{,}000$
  when f_{OSC} = 48kHz; t_{CYC} = 333ms

- **COMMON MODE INPUT VOLTAGE**

  $(V- + 1V) < V_{IN} < (V+ - 0.5V)$

- **AUTO-ZERO CAPACITOR**

  $0.01\mu F < C_{AZ} < 1\mu F$

- **REFERENCE CAPACITOR**

  $0.1\mu F < C_{REF} < 1\mu F$

- **V_{COM}**
  Biased between Vi and V-.

- **$V_{COM} \cong$ V+ - 2.8V**
  Regulation lost when V+ to V- < ≅6.8V
  If V_{COM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

7106 POWER SUPPLY: SINGLE 9V

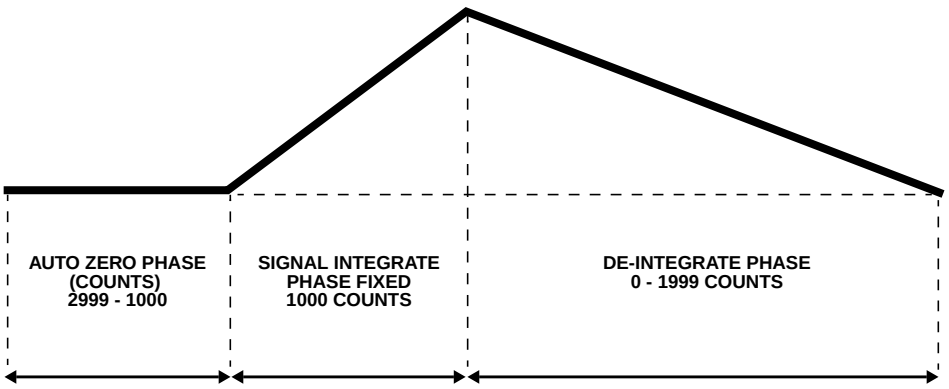
V+ - V- = 9V
Digital supply is generated internally
$V_{GND} \cong$ V+ - 4.5V

- Type: Direct drive with digital logic supply amplitude.

- V+ = +5V to GND
  V- = -5V to GND
  Digital Logic and LED driver supply V+ to GND

- Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 4000 x t_{CLOCK} = 16,000 x t_{OSC}

Detailed Description

Analog Section

Figure 3 shows the Analog Section for the
7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zer o Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000\left(\frac{V_{IN}}{V_{REF}}\right).$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

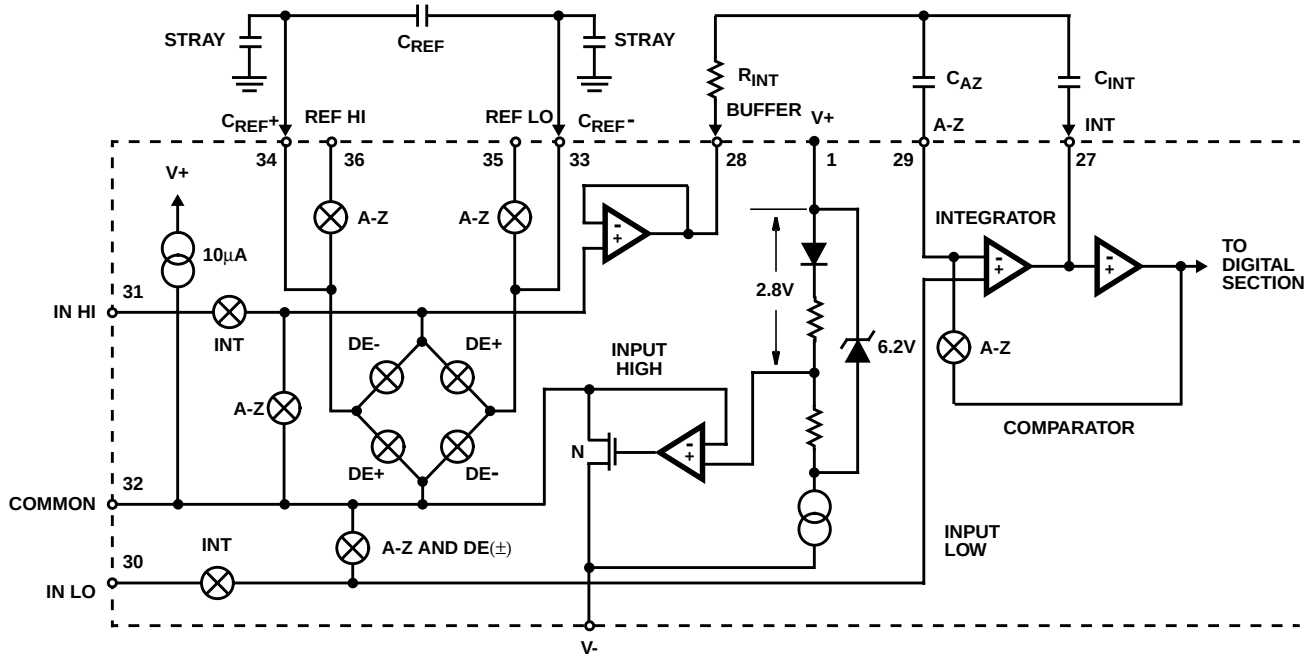


FIGURE 3. ANALOG SECTION OF

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation
where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/^{0}C.

The limitations of the on chip reference should also be recognized, however. With the
which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25µV to 80µV$_{P-P}$. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over-range and a non-over-range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the lC, analog COMMON is tied to an N-Channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10µA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

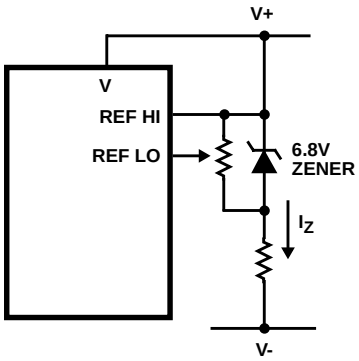


FIGURE 4A.

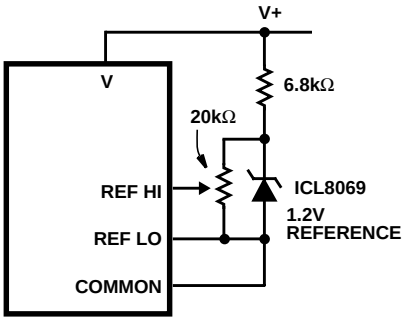


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the
coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

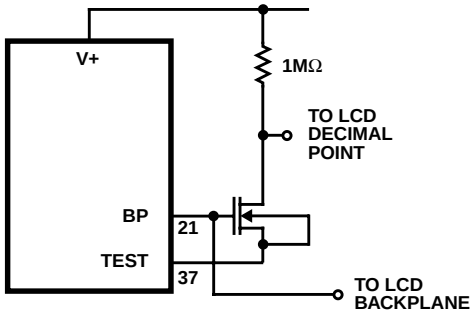


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

The second function is a “lamp test”. When TEST is pulled high (to V+) all segments will be turned on and the display should read “1888”. The TEST pin will sink about 15mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

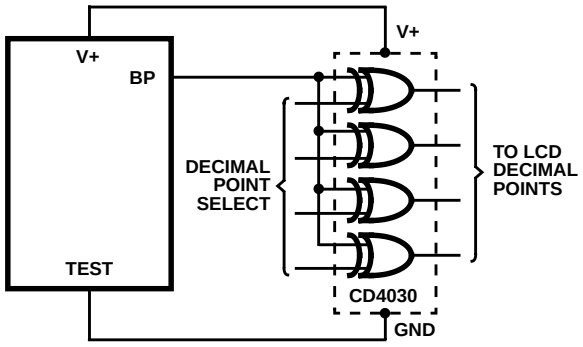


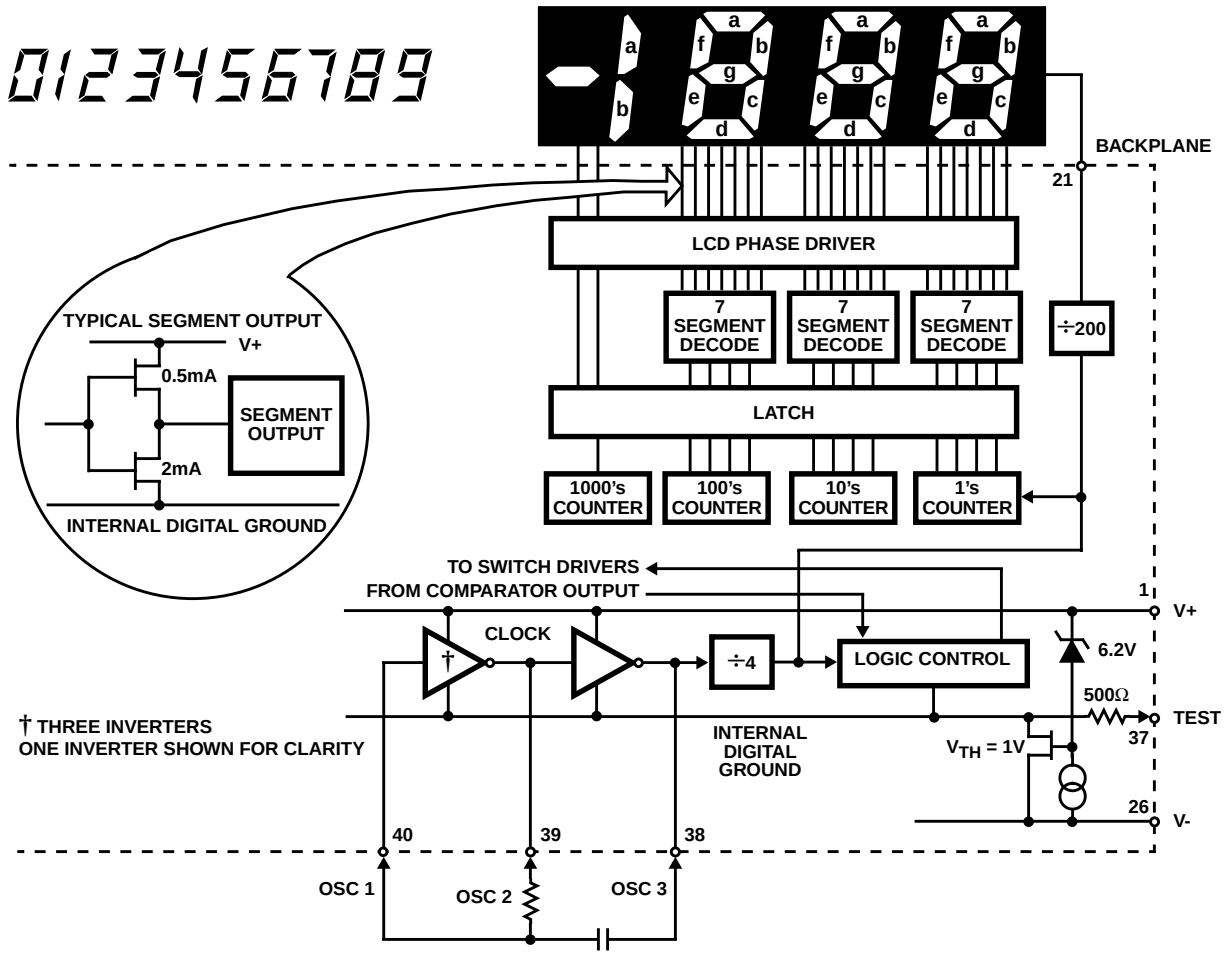
FIGURE 6. EXCLUSIVE ‘OR’ GATE FOR DECIMAL POINT DRIVE

Digital Section

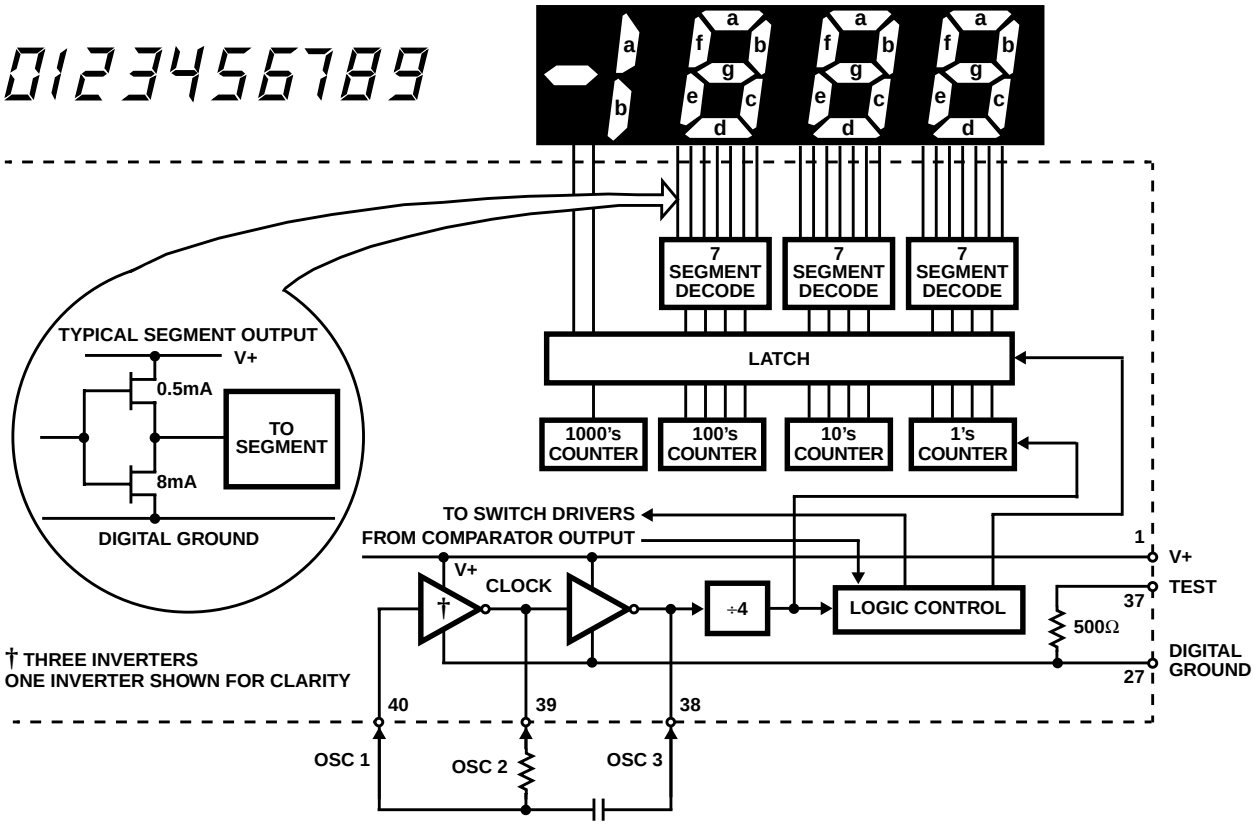
Figures 7 and 8 show the digital section for the , an internal digital ground is generated from a 6V Zener diode and a large P-Channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/sec., this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is “on” for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.



7106 DIGITAL SECTION



7107 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the . Two basic clocking arrangements can be used:

1. Figure 9A. An external oscillator connected to pin 40.
2. Figure 9B. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^{1}/_{3}$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^{2}/_{3}$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

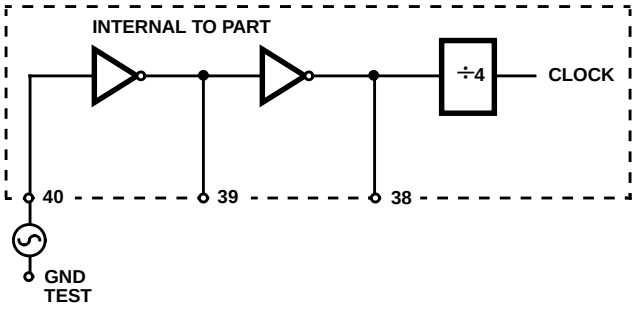


FIGURE 9A.

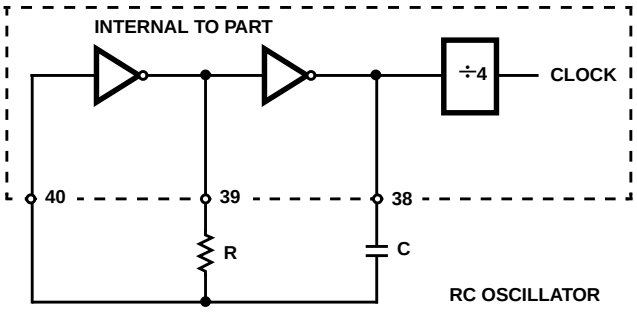


FIGURE 9B.

FIGURE 9. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 4µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.3V from either supply). In the
analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For the
supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22µF and 0.10µF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47µF capacitor is recommended. On the 2V scale, a 0.047µF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1µF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1µF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation:

$$f = \frac{0.45}{RC}$$ For 48kHz Clock (3 Readings/sec),

C = 100pF.

Reference Voltage

The analog input required to generate full scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 1 20kΩ and 0.22µF. This makes the system slightly quieter and also avoids a divider
7107 with ±5V supplies can
accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive lC. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

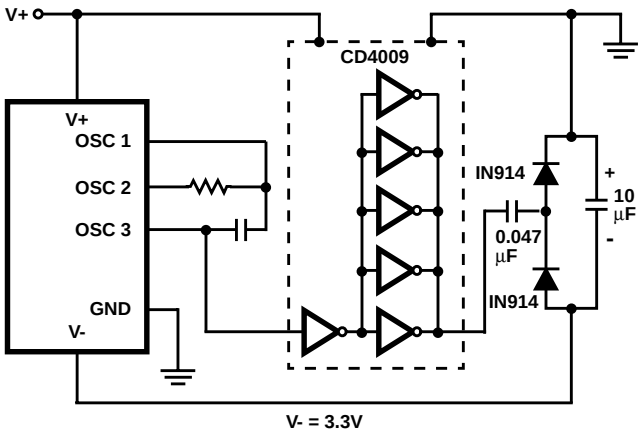
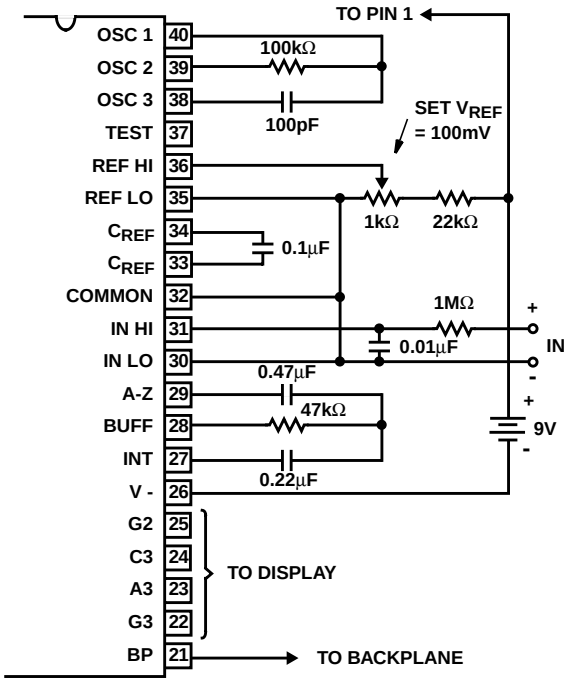
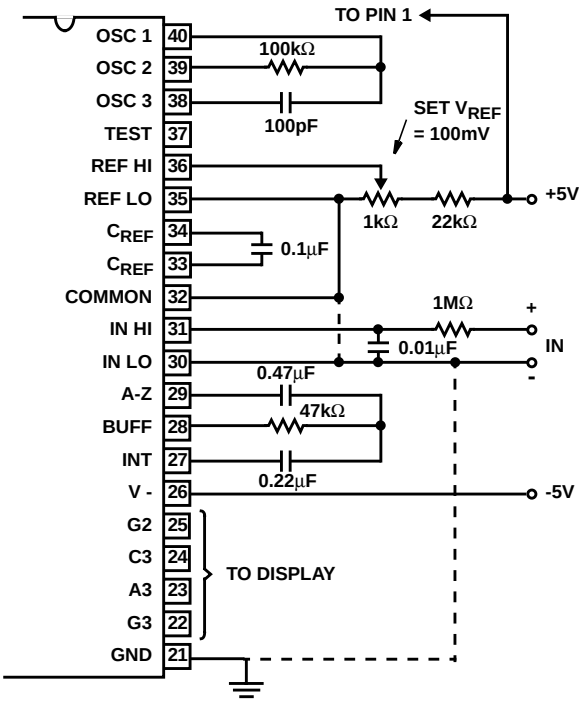


FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

Typical Applications

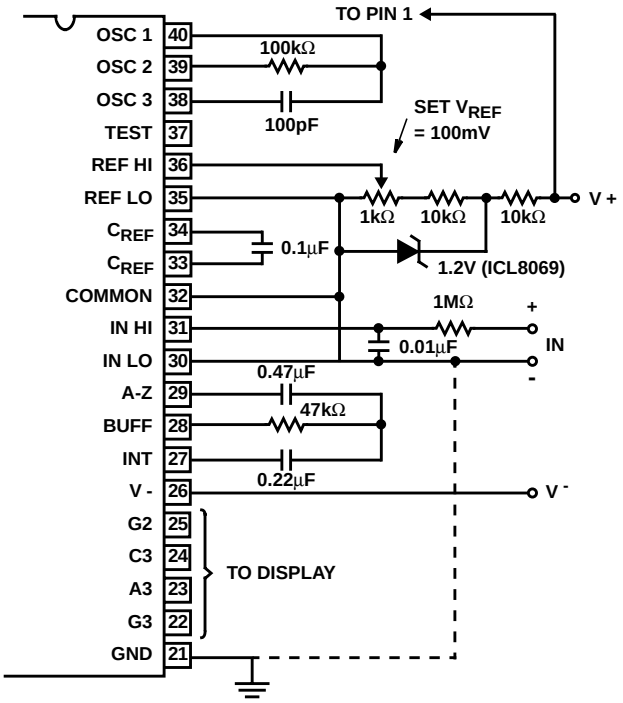


Values shown are for 200mV full scale, 3 readings/sec., floating supply voltage (9V battery).



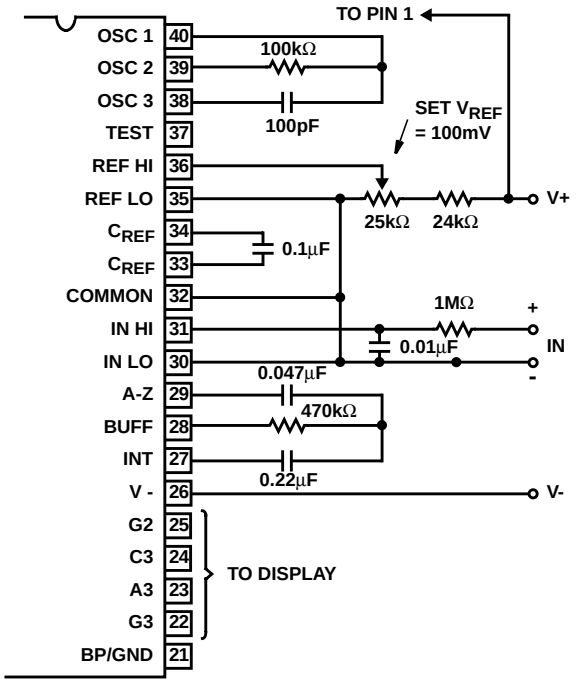
Values shown are for 200mV full scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

Typical Applications (Continued)

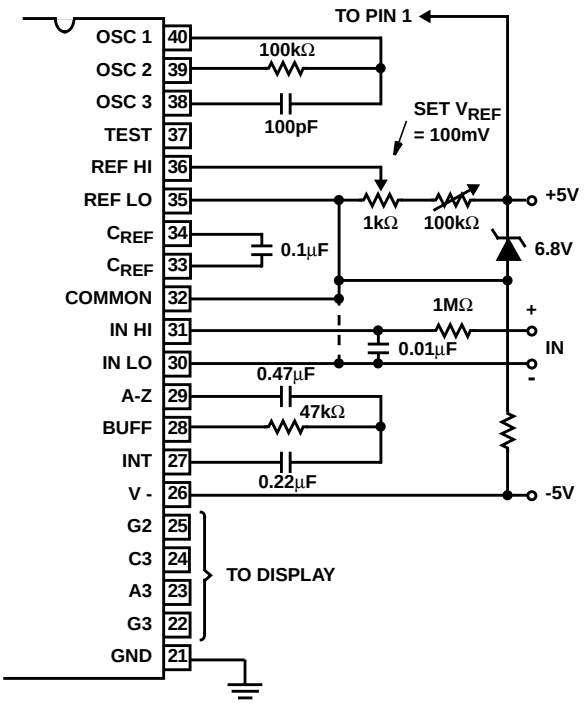


IN LO is tied to supply COMMON establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply GND) and the pre-regulator is overridden.

7107 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)

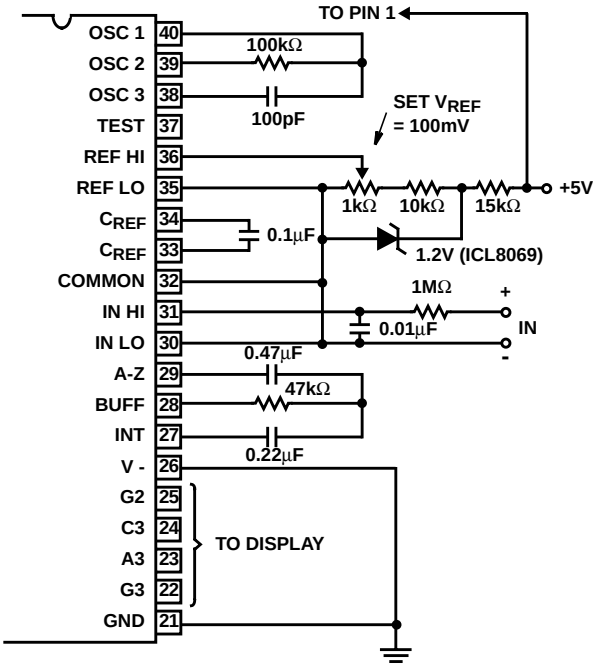


COMPONENT VALUES FOR 2V FULL SCALE



Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 14, IN LO may be tied to either COMMON or GND.

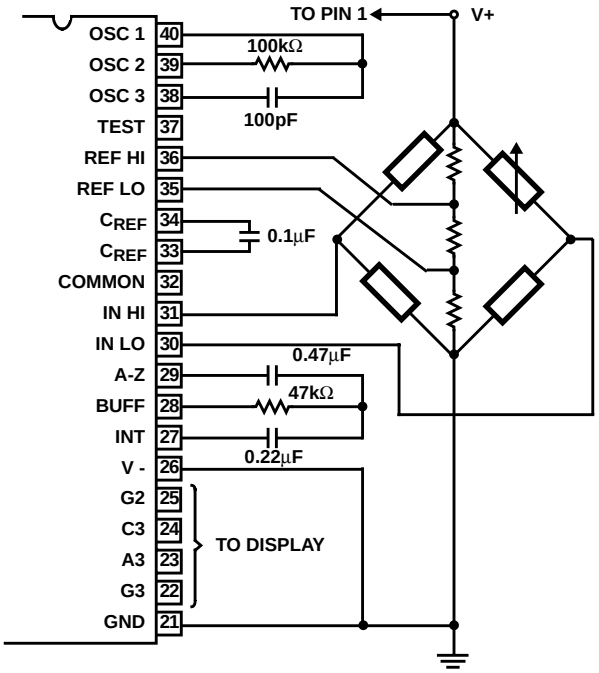
7107 WITH ZENER DIODE REFERENCE



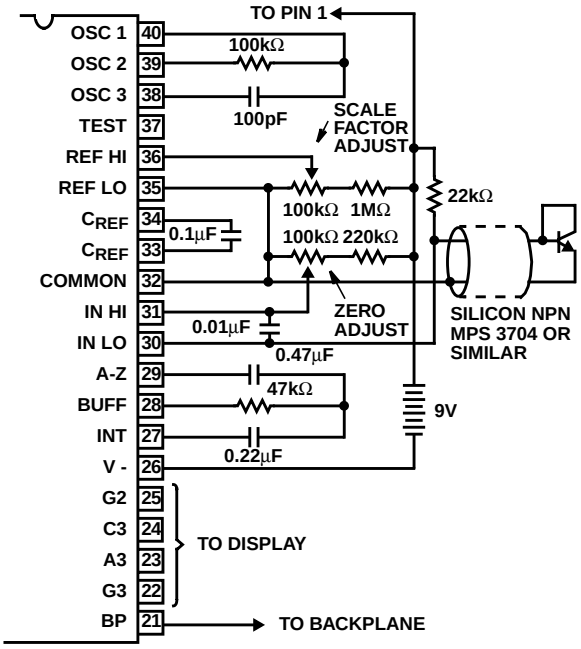
An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

7107 OPERATED FROM SINGLE +5V

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.



A silicon diode-connected transistor has a temperature coefficient of about -2mV/^{0}C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

7107 MEASUREING RATIOMETRIC VALUES OF QUAD LOAD CELL

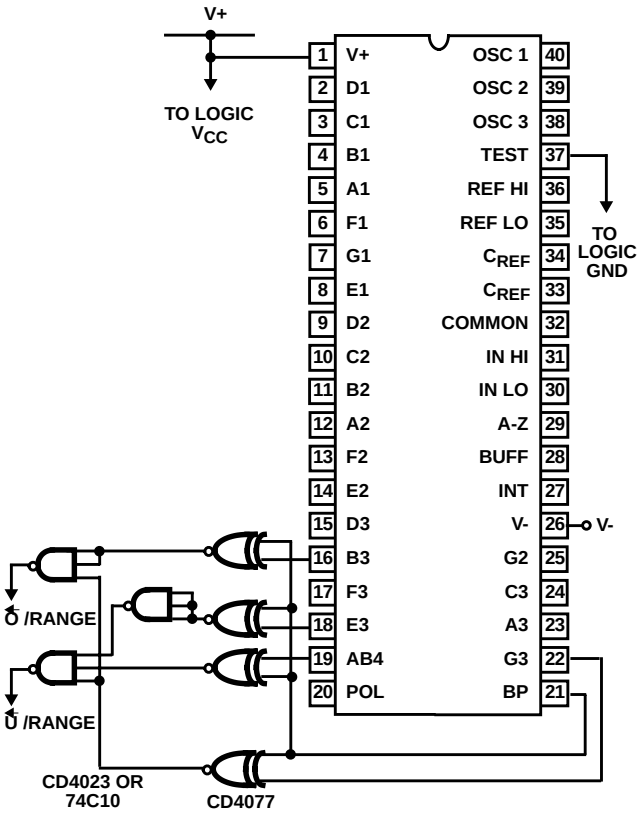
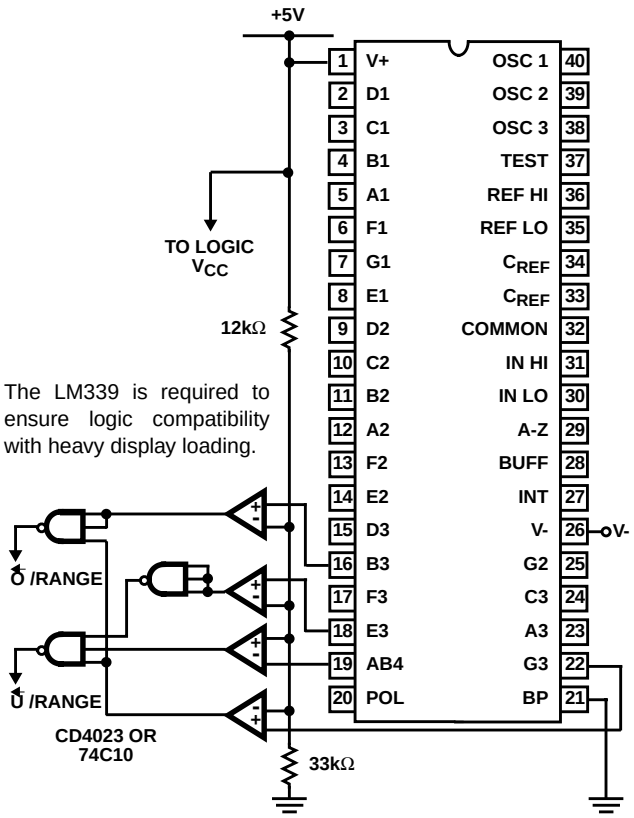


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNAL FROM

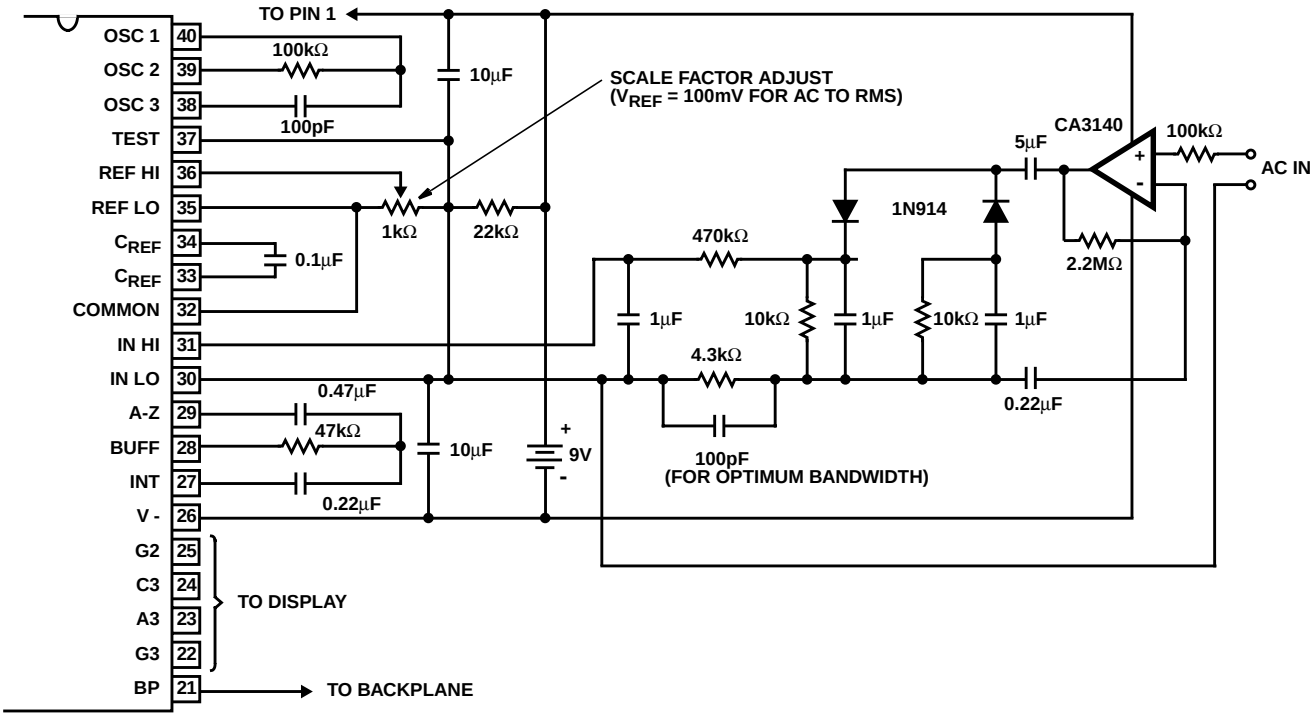
7106 USED AS A DIGITAL CENTIGRADE THERMOMETER



The LM339 is required to ensure logic compatibility with heavy display loading.

FIGURE 20. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

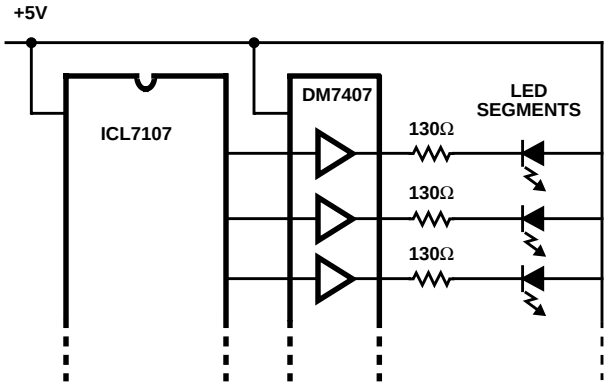
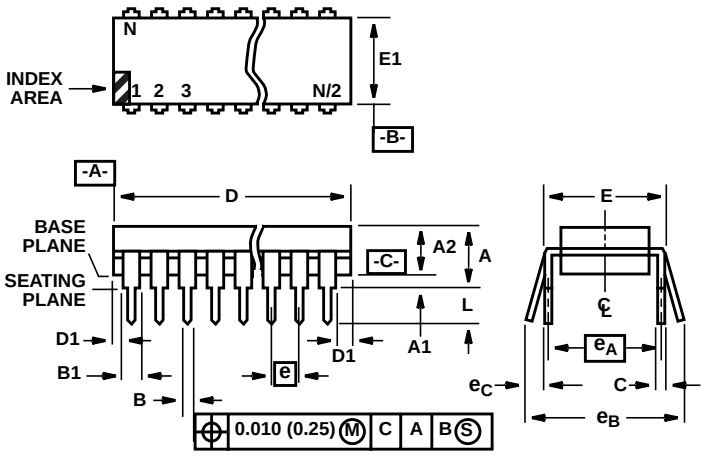


FIGURE 22. DISPLAY BUFFERING FOR INCREASED DRIVE CURRENT

Dual-In-Line Plastic Packages (PDIP)



E40.6 (JEDEC MS-011-AC ISSUE B)

40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).