19-2729; Rev 1; 8/05

EVALUATION KIT AVAILABLE

MAXIM

3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

General Description

The MAX1536 constant-off-time, pulse-width-modulated (PWM) step-down DC-to-DC converter is ideal for use in +5.0V and +3.3V to low voltages for notebook and sub-notebook computers. The MAX1536 features an internal PMOS power switch and internal synchronous rectification for high efficiency and reduced component count. No external Schottky diode is required across the internal synchronous rectifier switch. The internal 54mΩ PMOS power switch and 47mΩ NMOS synchronous-rectifier switch easily deliver continuous load currents up to 3.6A. The MAX1536 produces dynamically adjustable output voltages for chipsets and graphics processor cores using a logic-level control signal. The MAX1536 achieves efficiencies as high as 96%.

The MAX1536 uses a unique current-mode, constant-off-time, PWM control scheme. It has selectable Idle Mode™ to maintain high efficiency during light-load operation, or fixed-PWM mode for low output ripple. The programmable constant-off-time architecture allows a wide range of switching frequencies up to 1.4MHz, optimizing performance trade-offs between efficiency, output switching noise, component size, and cost. The MAX1536 features a digital soft-start to limit surge currents during startup, a 100% duty-cycle mode for low-dropout operation, and a low-power shutdown mode that disconnects the input from the output and reduces supply current below 1µA. The MAX1536 is available in a 28-pin thin QFN package with an exposed backside pad.

Applications

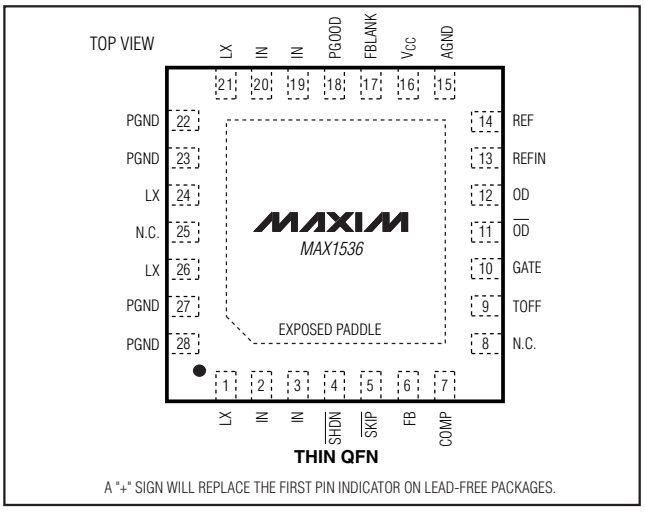
Chipset/Graphics Cores with Dual-Supply Voltages

Active Termination Buses

Notebook Computers

DDR Memory Termination

Pin Configuration



Idle Mode is a trademark of Maxim Integrated Products, Inc.

Features

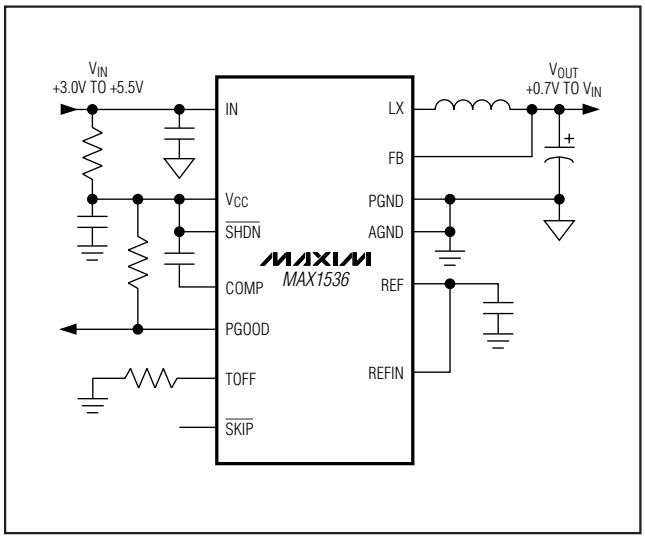
- **Dynamically Selectable Output Voltage from +0.7V to V_{IN}**
- **Internal PMOS/NMOS Switches**
  54mΩ/47mΩ On-Resistance at V_{IN} = +4.5V
  63mΩ/53mΩ On-Resistance at V_{IN} = +3.0V
- **+3.0V to +5.5V Input Voltage Range**
- **1.4MHz Maximum Switching Frequency**
- **2V ±0.75% Reference Output**
- **Constant-Off-Time PWM Operation**
- **Selectable Idle Mode/PWM Operation at Light Loads**
- **100% Duty Factor in Dropout**
- **Digital Soft-Start Inrush Current Limiting**
- **<1µA Typical Shutdown Supply Current**
- **<750µA Quiescent Supply Current**
- **Thermal Shutdown**
- **1% V_{OUT} Accuracy Over Line and Load**
- **External Reference Input**
- **Power-Good Window Comparator**
- **Selectable Power-Good Blanking Time During Output-Voltage Transition**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1536ETI	-40°C to +85°C	28 Thin QFN 5mm x 5mm
MAX1536ETI+	-40°C to +85°C	28 Thin QFN 5mm x 5mm

+Denotes lead-free package.

Minimal Operating Circuit



3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

ABSOLUTE MAXIMUM RATINGS

V_{CC}, IN, $\overline{SHDN}$, $\overline{SKIP}$ to AGND .....-0.3V to +6V
OD, $\overline{OD}$, GATE, PGOOD to AGND.....-0.3V to +6V
COMP, FB, REF to AGND.....-0.3V to +6V
TOFF, REFIN, FBLANK to AGND .....-0.3V to +6V
IN to V_{CC} .....-0.3V to +0.3V
PGND to AGND ..... -0.3V to +0.3V
LX to PGND ..... -0.3V to (V_{IN} + 0.3V)
LX Current (Note 1).....±5.7A
REF Short Circuit to AGND.....Continuous

Continuous Power Dissipation (T_A = +70°C)
28-Pin Thin QFN (derated 20.8mW/°C above +70°C; part mounted on 1in² of 1oz copper).....1667mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: LX has clamp diodes to PGND and IN. Thermal limits dictate the maximum continuous current through these diodes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, V_{REFIN} = +1.5V, $\overline{SKIP}$ = AGND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage	V_{IN}, V_{CC}			3.0		5.5	V
Output Adjust Range	V_{OUT}			V_{REFIN}		V_{IN}	V
Feedback Voltage Accuracy	V_{FB} - V_{REFIN}	V_{CC} = V_{IN} = +3.0V to +5.5V, I_{LOAD} = 0	T_A = +25°C to +85°C	-3	0	+3	mV
			T_A = 0°C to +85°C	-4	0	+4	
Feedback Load Regulation		I_{LOAD} = 0 to 3.5A, V_{CC} = V_{IN} = +3.0V to +5.5V, $\overline{SKIP}$ = V_{CC}			0.3		%
FB Input Bias Current	I_{FB}	V_{FB} = 1.01 × V_{REFIN}		-50		+50	nA
Dropout	V_{DO}	V_{CC} = V_{IN} = +3.0V, I_{LOAD} = 3A, FB = AGND			189	330	mV
PMOS Switch On-Resistance	R_{PMOS}	V_{CC} = V_{IN} = +4.5V, I_{LOAD} = 0.5A			54	90	mΩ
		V_{CC} = V_{IN} = +3.0V, I_{LOAD} = 0.5A			63	110	
NMOS Switch On-Resistance	R_{NMOS}	V_{CC} = V_{IN} = +4.5V, I_{LOAD} = 0.5A			47	80	mΩ
		V_{CC} = V_{IN} = +3.0V, I_{LOAD} = 0.5A			53	90	
Maximum Output Current	$I_{OUT(RMS)}$	(Note 2)				3.6	A
Current-Limit Threshold	I_{LIMIT}	(Note 3)		4.0	4.8	5.5	A
Idle Mode Current Threshold		$\overline{SKIP}$ = AGND		0.21	0.60	1.00	A
Zero-Cross Current Threshold		$\overline{SKIP}$ = AGND			200		mA
Switching Frequency	f_{SW}	(Note 2)				1.4	MHz
Off-Time	t_{OFF}	V_{FB} ≥ 0.3 × V_{REFIN}	R_{TOFF} = 30.1kΩ	0.24	0.30	0.37	µs
			R_{TOFF} = 110kΩ	0.85	1.00	1.15	
			R_{TOFF} = 499kΩ	3.8	4.5	5.2	
Extended Off-Time		V_{FB} < 0.3 × V_{REFIN}			4 × t_{OFF}		µs
On-Time	t_{ON}	(Note 2)		0.3			µs
Soft-Start Time		(Note 3)			3 × 256		Cycles
Quiescent Supply Current	I_{CC} + I_{IN}	$\overline{SKIP}$ = AGND, V_{FB} = 1.01 × V_{REFIN}			350	750	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, V_{REFIN} = +1.5V, $\overline{SKIP}$ = AGND, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Currents	I_{CC} + I_{IN}	$\overline{SHDN}$ = AGND; current into V_{CC} and IN; LX = 0 or +3.3V		0.2	20	µA
	I_{IN}	$\overline{SHDN}$ = AGND; current into IN; LX = 0		0.2	20	
	I_{LX}	$\overline{SHDN}$ = AGND; current into LX; LX = +3.3V		0.1	20	
REFERENCE						
REF Voltage	V_{REF}	V_{CC} = V_{IN} = +3.0V to +5.5V	1.985	2.000	2.015	V
REF Load Regulation		I_{REF} = -1µA to +50µA			10	mV
REFIN Input Voltage Range	V_{REFIN}	V_{CC} = V_{IN} = +3.0V to +5.5V, V_{CC} > V_{REFIN} + 1.35V	0.7		2.0	V
REFIN Input Bias Current	I_{REFIN}	V_{REFIN} = 1.5V, V_{FB} = 1.01 × V_{REFIN}	-50		+50	nA
FAULT DETECTION						
Thermal Shutdown	T_{SHDN}	Rising, hysteresis = 15°C		165		°C
Undervoltage Lockout Threshold		V_{CC} and V_{IN} rising, hysteresis 60mV typical	2.4	2.6	2.8	V
		V_{CC} - V_{REFIN}, V_{CC} rising, hysteresis 60mV typical		0.9	1.35	
		V_{CC} - V_{FB}, V_{CC} rising, hysteresis 60mV typical		0.9	1.35	
PGOOD Lower Trip Threshold		No load, falling edge, hysteresis = 1% (Note 4)	-12.5	-10	-8.0	%
PGOOD Upper Trip Threshold		No load, rising edge, hysteresis = 1% (Note 4)	+8.0	+10	+12.5	%
PGOOD Propagation Delay	t_{PGOOD}	FB forced 2% beyond PGOOD trip threshold		5		µs
PGOOD Output Low Voltage		I_{SINK} = 1mA			0.1	V
PGOOD Leakage Current		High-impedance state, forced to +5.5V			1	µA
Fault Blanking Time	t_{FBLANK}	FBLANK = V_{CC}	112	150	188	µs
		FBLANK = open or AGND	75	100	125	
		FBLANK = REF	37	50	63	
INPUTS AND OUTPUTS						
Logic Input Threshold	$V_{\overline{SHDN}}$, $V_{\overline{SKIP}}$, V_{GATE}	$\overline{SHDN}$, $\overline{SKIP}$, GATE, V_{IN} = V_{CC} = +3.3V, rising edge, hysteresis = 100mV	0.9	1.3	1.6	V
		$\overline{SHDN}$, $\overline{SKIP}$, GATE, V_{IN} = V_{CC} = +5.0V, rising edge, hysteresis = 100mV	1.15	1.55	1.95	
Logic Input Current		$\overline{SHDN}$, $\overline{SKIP}$, GATE	-0.5		+0.5	µA
FBLANK Logic Thresholds	V_{FBLANK}	FBLANK = V_{CC}	V_{CC} - 0.2			V
		FBLANK = REF	1.8		2.2	
		FBLANK = open	0.8		1.2	
		FBLANK = AGND			0.2	
FBLANK Input Current	I_{FBLANK}	FBLANK forced to AGND or V_{CC}	-5		+5	µA
OD On-Resistance	R_{OD}	GATE = V_{CC}		10	25	Ω
OD Leakage Current		GATE = AGND, V_{OD} = +5.5V	-50		+50	nA
$\overline{OD}$ On-Resistance	$R_{\overline{OD}}$	GATE = AGND		10	25	Ω
$\overline{OD}$ Leakage Current		GATE = V_{CC}, $V_{\overline{OD}}$ = +5.5V	-50		+50	nA

3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, V_{REFIN} = +1.5V, $\overline{SKIP}$ = AGND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage	V_{IN}, V_{CC}			3.0		5.5	V
Feedback Voltage Accuracy	V_{FB} - V_{REFIN}	V_{CC} = V_{IN} = +3.0V to +5.5V, I_{LOAD} = 0		-4		+4	mV
FB Input Bias Current	I_{FB}	V_{FB} = 1.01 × V_{REFIN}		-50		+50	nA
Dropout	V_{DO}	V_{CC} = V_{IN} = +3.0V, I_{LOAD} = 3A, FB = AGND				330	mV
PMOS Switch On-Resistance	R_{PMOS}	V_{CC} = V_{IN} = +4.5V, I_{LOAD} = 0.5A				90	mΩ
		V_{CC} = V_{IN} = +3.0V, I_{LOAD} = 0.5A				110	
NMOS Switch On-Resistance	R_{NMOS}	V_{CC} = V_{IN} = +4.5V, I_{LOAD} = 0.5A				80	mΩ
		V_{CC} = V_{IN} = +3.0V, I_{LOAD} = 0.5A				90	
Maximum Output Current	$I_{OUT(RMS)}$	(Note 2)				3.6	A
Current-Limit Threshold	I_{LIMIT}	(Note 3)		4.0		5.7	A
Idle Mode Current Threshold		$\overline{SKIP}$ = AGND		0.21		1.00	A
Switching Frequency	f_{SW}	(Note 2)				1.4	MHz
Off-Time	t_{OFF}	V_{FB} ≥ 0.3 × V_{REFIN}	R_{TOFF} = 30.1kΩ	0.24		0.37	µs
			R_{TOFF} = 110kΩ	0.85		1.15	
			R_{TOFF} = 499kΩ	3.8		5.2	
On-Time	t_{ON}	(Note 2)		0.3			µs
Quiescent Supply Current	I_{CC} + I_{IN}	$\overline{SKIP}$ = AGND, V_{FB} = 1.01 × V_{REFIN}				750	µA
Shutdown Supply Currents	I_{CC} + I_{IN}	$\overline{SHDN}$ = AGND; current into V_{CC} and IN; LX = 0 or +3.3V				20	µA
	I_{IN}	$\overline{SHDN}$ = AGND; current into IN; LX = 0				20	
	I_{LX}	$\overline{SHDN}$ = AGND; current into LX; LX = +3.3V				20	
REFERENCE							
REF Voltage	V_{REF}	V_{CC} = V_{IN} = +3.0V to +5.5V		1.98		2.02	V
REFIN Input Voltage Range	V_{REFIN}	V_{CC} = V_{IN} = +3.0V to +5.5V, V_{CC} > V_{REFIN} + 1.35V		0.7		2.0	V
FAULT DETECTION							
PGOOD Lower Trip Threshold		No load, falling edge, hysteresis = 1% (Note 4)		-12.5		-8	%
PGOOD Upper Trip Threshold		No load, rising edge, hysteresis = 1% (Note 4)		+8		+12.5	%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = V_{CC} = $V_{\overline{SHDN}}$ = +3.3V, V_{REFIN} = +1.5V, $\overline{SKIP}$ = AGND, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS AND OUTPUTS						
Logic Input Threshold	$V_{\overline{SHDN}}$, $V_{\overline{SKIP}}$, V_{GATE}	$\overline{SHDN}$, $\overline{SKIP}$, GATE, V_{IN} = V_{CC} = +3.3V, rising edge, hysteresis = 100mV	0.9		1.6	V
		$\overline{SHDN}$, $\overline{SKIP}$, GATE, V_{IN} = V_{CC} = +5.0V, rising edge, hysteresis = 100mV	1.15		1.95	
FBLANK Logic Thresholds	V_{FBLANK}	FBLANK = V_{CC}	V_{CC} - 0.2			V
		FBLANK = REF	1.8		2.2	
		FBLANK = open	0.8		1.2	
		FBLANK = AGND			0.2	
OD On-Resistance	R_{OD}	GATE = V_{CC}			25	Ω
$\overline{OD}$ On-Resistance	$R_{\overline{OD}}$	GATE = AGND			25	Ω

Note 2: Guaranteed by design and not production tested.

Note 3: To limit input surge currents, the current-limit threshold is set to 25% of its final value (25% x 4.8A = 1.2A) when the MAX1536 is enabled or powered up. The current-limit threshold is increased by 25% every 256 LX cycles. The current-limit threshold is at its final level of 4.8A after 768 LX cycles. See the *Internal Soft-Start Circuit* section.

Note 4: The upper and lower PGOOD thresholds are expressed as a ratio of V_{FB} with respect to V_{REFIN}.

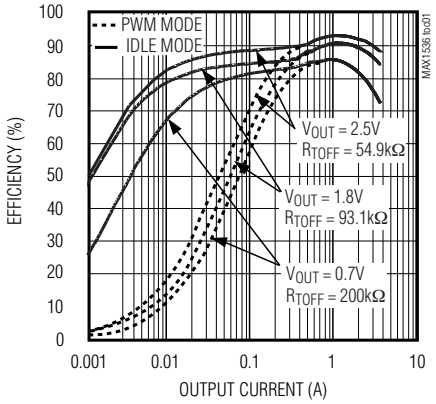
$$\frac{V_{FB}-V_{REFIN}}{V_{REFIN}} \times 100\%$$

Note 5: Specifications to -40°C are guaranteed by design and are not production tested.

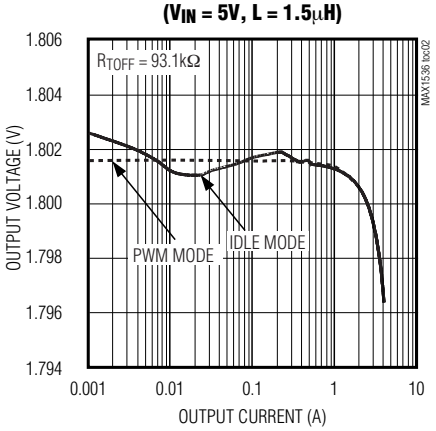
Typical Operating Characteristics

(MAX1536 Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

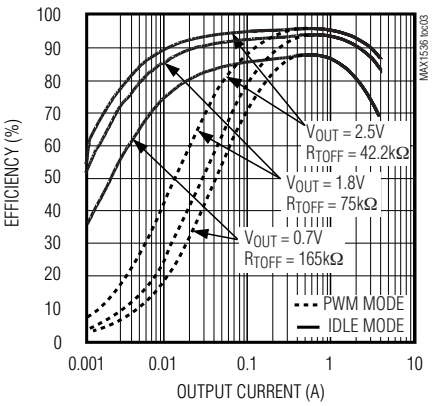
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 5V, L = 1.5µH)



OUTPUT VOLTAGE vs. OUTPUT CURRENT (V_{IN} = 5V, L = 1.5µH)



EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 3.3V, L = 1.2µH)

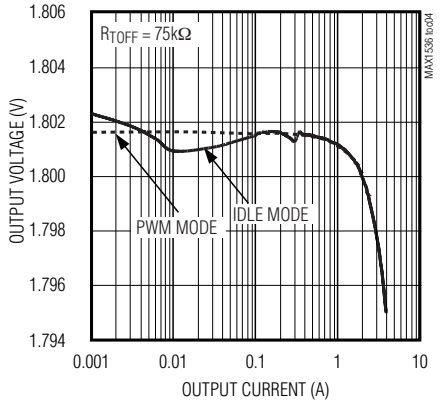


3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

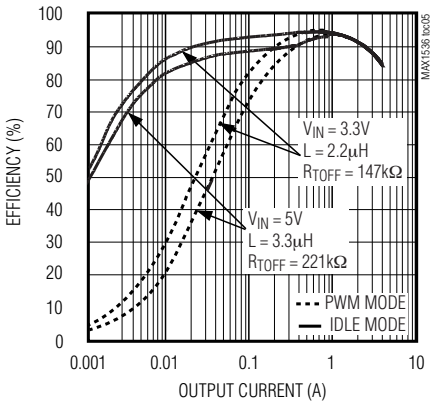
Typical Operating Characteristics (continued)

(MAX1536 Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

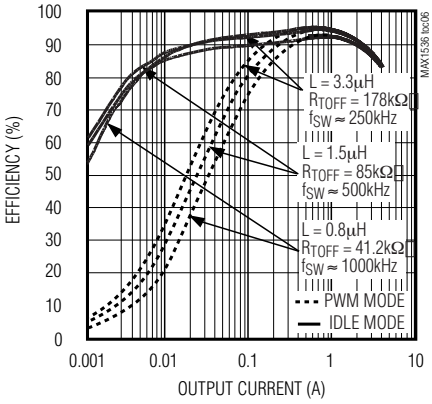
OUTPUT VOLTAGE vs. OUTPUT CURRENT (V_{IN} = 3.3V, L = 1.2µH)



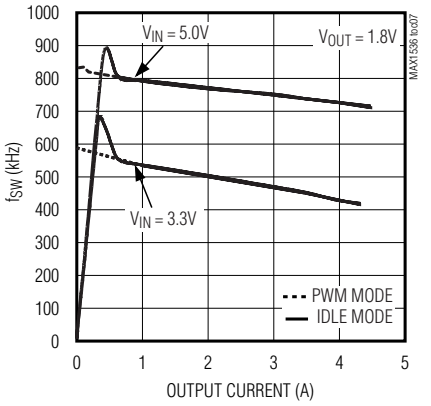
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 1.8V, f_{SW} = 300kHz)



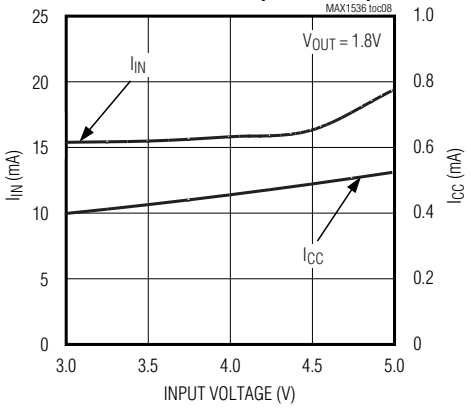
EFFICIENCY vs. OUTPUT CURRENT (V_{IN} = 3.3V, V_{OUT} = 1.8V)



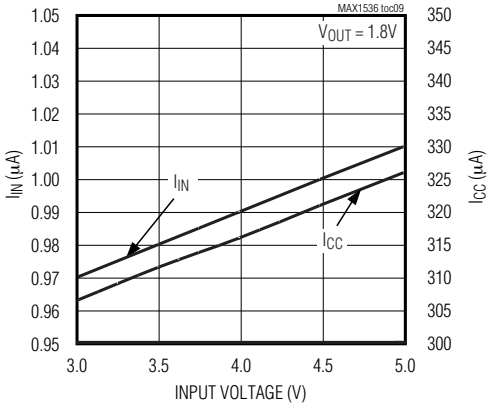
SWITCHING FREQUENCY vs. OUTPUT CURRENT



NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (PWM MODE)



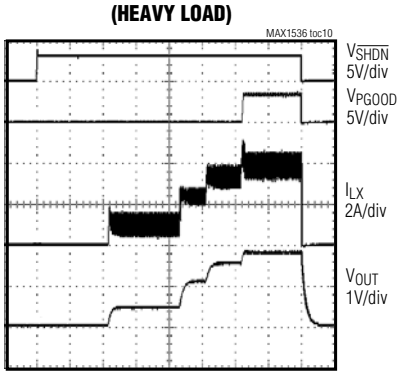
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE (IDLE MODE)



Typical Operating Characteristics (continued)

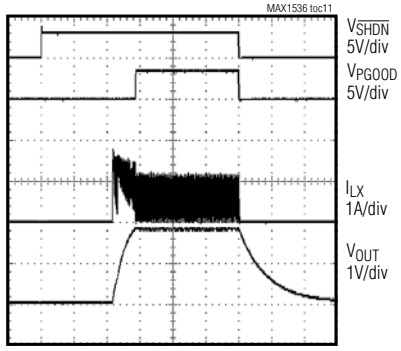
(MAX1536 Circuit of Figure 1, T_A = +25°C, unless otherwise noted.)

STARTUP AND SHUTDOWN (HEAVY LOAD)



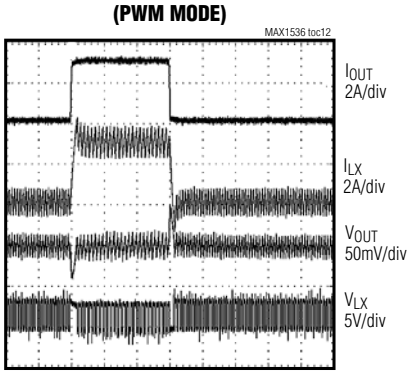
V_{IN} = 3.3V, V_{OUT} = 1.8V, R_{LOAD} = 0.5Ω

STARTUP AND SHUTDOWN (LIGHT LOAD)



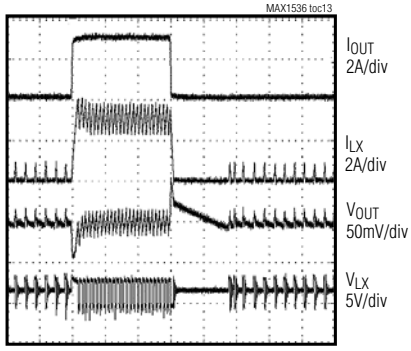
V_{IN} = 3.3V, V_{OUT} = 1.8V, R_{LOAD} = 3Ω

LOAD-TRANSIENT RESPONSE (PWM MODE)



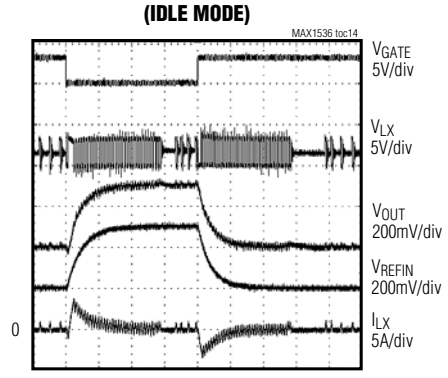
V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 0.1A TO 3A TO 0.1A

LOAD-TRANSIENT RESPONSE (IDLE MODE)



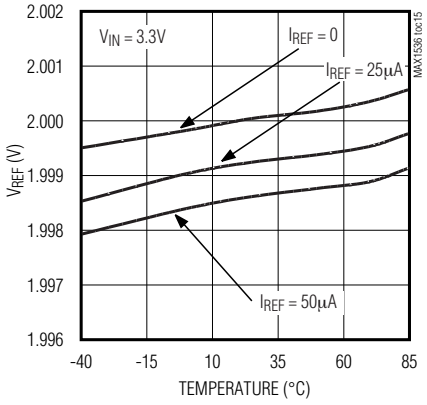
V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 0.1A TO 3A TO 0.1A

DYNAMIC OUTPUT-VOLTAGE TRANSITION (IDLE MODE)



V_{IN} = 3.3V, V_{OUT} = 1.5V TO 1.8V TO 1.5V, FBLANK = REF, I_{LOAD} = 0.1A

REFERENCE VOLTAGE vs. TEMPERATURE



3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

Pin Description

PIN	NAME	FUNCTION
1, 21, 24, 26	LX	Inductor Connection. Connection for the drains of the PMOS power switch and NMOS synchronous-rectifier switch. Connect all LX pins together.
2, 3, 19, 20	IN	Power Input. Power input for the internal PMOS switch. Connect all IN pins together.
4	$\overline{SHDN}$	Shutdown Control Input. Drive $\overline{SHDN}$ low to disable the reference, control circuitry, and internal MOSFETs. Drive $\overline{SHDN}$ high or connect to V_{CC} for normal operation.
5	$\overline{SKIP}$	Pulse-Skipping Control Input. Connect $\overline{SKIP}$ to V_{CC} for low-noise, forced-PWM mode. Connect $\overline{SKIP}$ to AGND for high-efficiency Idle Mode.
6	FB	Feedback Input. The voltage at REFIN sets the feedback regulation voltage ($V_{FB} = V_{REFIN}$).
7	COMP	Integrator Compensation. Connect a 470pF capacitor from COMP to V_{CC} for integrator compensation. See the *Integrator Amplifier* section.
8, 25	N.C.	No Connection. Not internally connected. Connecting pin 25 to LX eases PC board layout.
9	TOFF	Off-Time Select Input. Sets the PMOS power switch off-time during constant off-time operation. Connect a resistor from TOFF to AGND to adjust the PMOS switch off-time. See the *Programming the No-Load Switching Frequency and Off-Time* section.
10	GATE	Buffered OD and $\overline{OD}$ Control Input. A logic low on GATE forces $\overline{OD}$ low and OD high impedance. A logic high on GATE forces $\overline{OD}$ high impedance and OD low.
11	OD	Open-Drain Output. A logic low on GATE forces OD high impedance. A logic high on GATE forces OD low.
12	$\overline{OD}$	Inverted Open-Drain Output. A logic low on GATE forces $\overline{OD}$ low. A logic high on GATE forces $\overline{OD}$ high impedance.
13	REFIN	External Reference Input. The voltage at REFIN sets the feedback regulation voltage ($V_{FB} = V_{REFIN}$).
14	REF	+2.0V Reference Voltage Output. Bypass REF to AGND with a minimum capacitance of 0.22µF. REF supplies up to 50µA for external loads. The internal reference turns off in shutdown.
15	AGND	Analog Ground. Connect backside pad to AGND.
16	V_{CC}	Analog Power Input. Power input to the internal analog circuitry. Bypass V_{CC} with a 10Ω and 2.2µF (min) lowpass filter (Figure 1).
17	FBLANK	Fault-Blanking Control Input. FBLANK is a four-level logic input that enables or disables fault blanking, and sets the minimum forced-PWM operation time (t_{FBLANK}). Enabling fault blanking forces PGOOD high for the selected time period after a transition is detected on GATE. Additionally, the controller enters forced-PWM mode for the duration of t_{FBLANK} anytime GATE changes states. Connect FBLANK to the following pins to select t_{FBLANK} and fault blanking: V_{CC} = 150µs (typ), fault blanking enabled Open = 100µs (typ), fault blanking enabled REF = 50µs (typ), fault blanking enabled AGND = 100µs (typ), fault blanking disabled
18	PGOOD	Open-Drain Power-Good Output. PGOOD is low during soft-start, in shutdown, and when the output voltage is more than 10% (typ) above or below the normal regulation point. After the soft-start, PGOOD becomes high impedance if the output is in regulation. PGOOD is blanked—forced into a high-impedance state—when FBLANK is enabled and a transition is detected on GATE.
22, 23, 27, 28	PGND	Power Ground. Internally connected to the source of the internal NMOS synchronous-rectifier switch. Connect all PGND pins together.

3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

Standard Application Circuit

The MAX1536 standard application circuit (Figure 1) generates a dynamically adjustable output voltage typical of graphic processor core requirements. See Table 1 for component selections. Table 2 lists the component manufacturers.

Detailed Description

The MAX1536 synchronous, current-mode, constant-off-time, PWM DC-to-DC converter steps down an input voltage (V_{IN}) from +3.0V to +5.5V to an output voltage from +0.7V to V_{IN}. The MAX1536 output delivers up to 3.6A of continuous current. An internal 54mΩ PMOS power switch and an internal 47mΩ NMOS synchronous rectifier switch improve efficiency, reduce component count, and eliminate the need for an external Schottky diode (Figure 2).

Modes of Operation

The MAX1536 has two modes of operation: constant-off-time PWM mode, and pulse-skipping Idle Mode. The logic level on the $\overline{SKIP}$ input and the current through the PMOS switch determine the MAX1536 mode of operation.

Forced-PWM mode keeps the switching frequency relatively constant and is desirable in applications that must always keep the frequency of conducted and radiated emissions in a narrow band. Visit Maxim's website at www.maxim-ic.com for more information on how to control electromagnetic interference (EMI). Pulse-skipping Idle Mode has a dynamic switching frequency under light loads and is desirable in applications that require high efficiency at light loads.

Forced-PWM Mode ($\overline{SKIP}$ = V_{CC})

Connect $\overline{SKIP}$ to V_{CC} to force the MAX1536 to operate in low-noise, constant-off-time PWM mode. Constant-off-time PWM architecture provides a relatively constant switching frequency (see the *Frequency Variation with Output Current* section). A single resistor (R_{TOFF}) sets the PMOS power switch off-time that results in a switching frequency up to 1.4MHz optimizing performance trade-offs in efficiency, switching noise, component size, and cost.

PWM mode regulates the output voltage by increasing the PMOS switch on-time to increase the amount of energy transferred to the load per cycle. At the end of each off-time, the PMOS switch turns on and remains on until the output is in regulation or the current through the switch increases to the 4.8A current limit. When the PMOS switch turns off, it remains off for the programmed off-time (t_{OFF}), and the NMOS synchronous switch turns on. The NMOS switch remains on until the end of t_{OFF}. Since either the NMOS or the PMOS switch is always on in PWM mode, the inductor current is continuous.

Idle Mode ($\overline{SKIP}$ = AGND)

Connect $\overline{SKIP}$ to AGND to allow the MAX1536 to automatically switch between high-efficiency Idle Mode under light loads and PWM mode under heavy loads. The transition from PWM mode to Idle Mode occurs when the load current is half the Idle Mode current threshold (600mA typ).

In Idle Mode operation, the switching frequency is reduced to increase efficiency. The inductor current is discontinuous in this mode and the MAX1536 only initiates an LX switching cycle when $V_{FB} < V_{REFIN}$. When V_{FB} falls below V_{REFIN}, the PMOS switch turns on and remains on until output is in regulation and the current through the switch increases to the Idle Mode current threshold (600mA typ). When the PMOS switch turns off, the NMOS synchronous switch turns on and remains on until the current through the switch decreases to the zero-cross-current threshold of 200mA.

100% Duty-Cycle Operation

When the input voltage drops near the output voltage, the LX duty cycle increases until the PMOS switch is on continuously. The dropout voltage in 100% duty cycle is the output current multiplied by the on-resistance of the internal PMOS switch and parasitic resistance in the inductor. The PMOS switch remains on continuously as long as the current limit is not reached.

Internal Soft-Start Circuit

Soft-start allows a gradual increase of the current-limit level at startup to reduce input surge currents. When the MAX1536 is enabled or powered up, its current-limit threshold is set to 25% of its final value (25% of 4.8A = 1.2A). The current-limit threshold is increased by 25% every 256 LX cycles. The current-limit threshold reaches its final level of 4.8A after 768 LX cycles or when the output voltage is in regulation, whichever occurs first. Additionally, when $V_{FB} < 0.3 \times V_{REFIN}$, the PMOS switch remains off for the extended off-time of 4 × t_{OFF}. As a result of this soft-start feature, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on the nominal switching frequency, output capacitance, and the load current. See the startup waveforms in the *Typical Operating Characteristics*.

Short-Circuit/Overload Protection

The MAX1536 can sustain a constant short circuit or overload. Under a short-circuit or overload condition, when $V_{FB} < 0.3 \times V_{REFIN}$, the MAX1536 uses an

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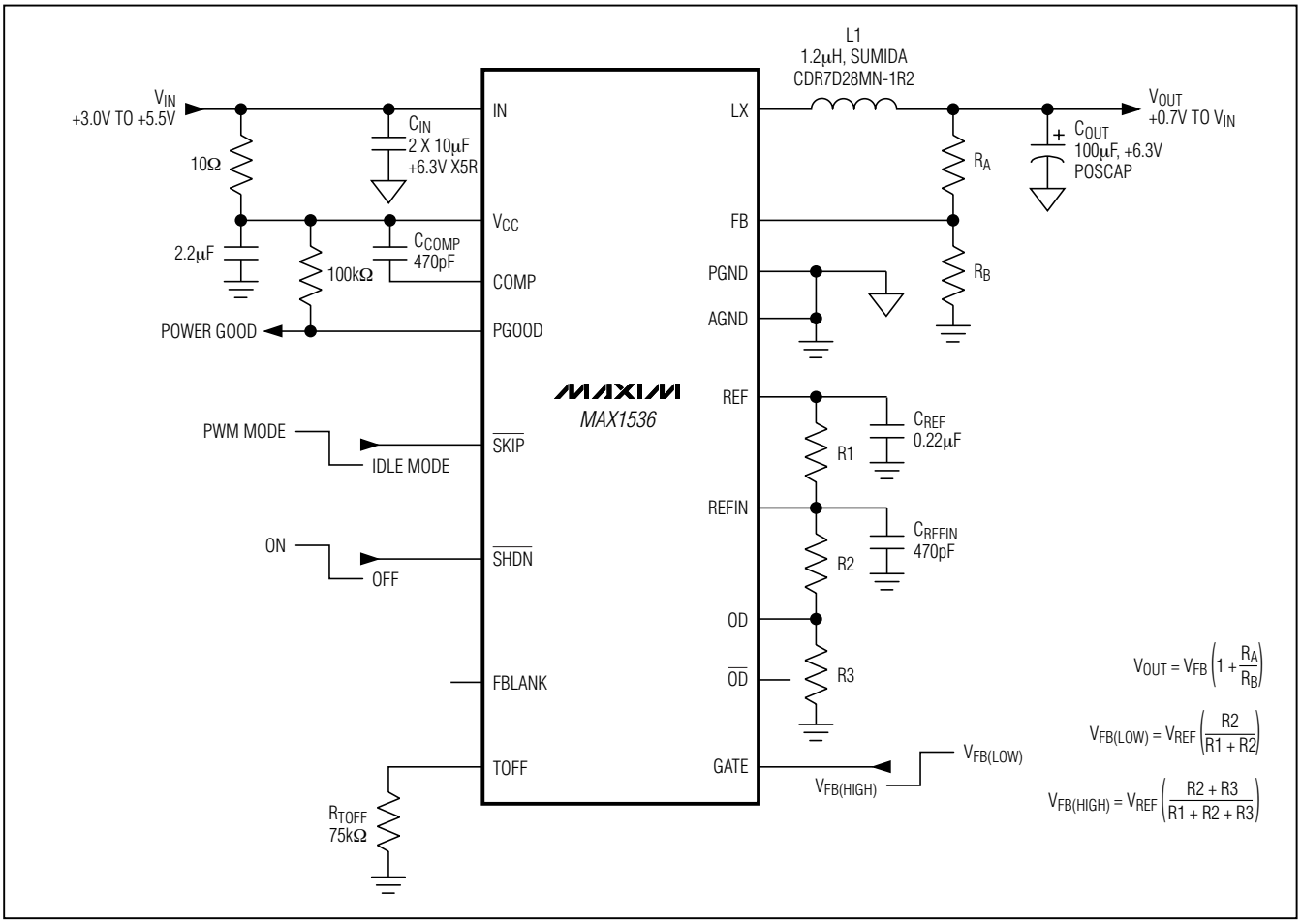

Figure 1. MAX1536 Standard Application Circuit

Table 1. Recommended Component Values (I_{OUT} = 3.6A)

V_{IN} (V)	V_{OUT} (V)	FULL-LOAD SWITCHING FREQUENCY f_{PWM} (kHz)	L (µH)	R_{TOFF} (kΩ)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	R_A (kΩ)	R_B (kΩ)
5	3.3*	1020	1.2	30.1	Short	Open	Open	6.49	10
5	2.5*	1020	1.2	47.5	Short	Open	Open	2.49	10
5	1.8/1.5**	820/900	1.2	78.7	20	60.4	121	Short	Open
5	0.7*	450	1.2	200	130	69.8	Short	Short	Open
3.3	2.5*	640	1.0	30.1	Short	Open	Open	2.49	10
3.3	1.8/1.5**	840/1030	1.0	49.9	20	60.4	121	Short	Open
3.3	0.7*	660	1.0	121	130	69.8	Short	Short	Open

**In single-output voltage applications, OD, $\overline{OD}$, and GATE are general-purpose gates. If OD and $\overline{OD}$ are not used, connect GATE to AGND and leave OD and $\overline{OD}$ open.*

***The output voltage changes between two set points depending on V_{GATE}. See the Setting Dynamic Output Voltages with REFIN section.*

Table 2. Component Manufacturers

SUPPLIER	COMPONENT	PHONE	WEBSITE
Coilcraft	Inductors	800-322-2645 (USA)	www.coilcraft.com
Coiltronics	Inductors	561-752-5000 (USA)	www.coiltronics.com
Kemet	Capacitors	408-986-0424 (USA)	www.kemet.com
Sanyo	Capacitors	818-998-7322 (USA)	www.sanyo.com
Sumida	Inductors	408-982-9660 (USA)	www.sumida.com
Taiyo Yuden	Capacitors	03-3667-3408 (Japan), 408-573-4150 (USA)	www.t-yuden.com
TDK	Capacitors	847-803-6100 (USA), 81-3-5201-7241 (Japan)	www.component.tdk.com
TOKO	Inductors	858-675-8013 (USA)	www.toko.com

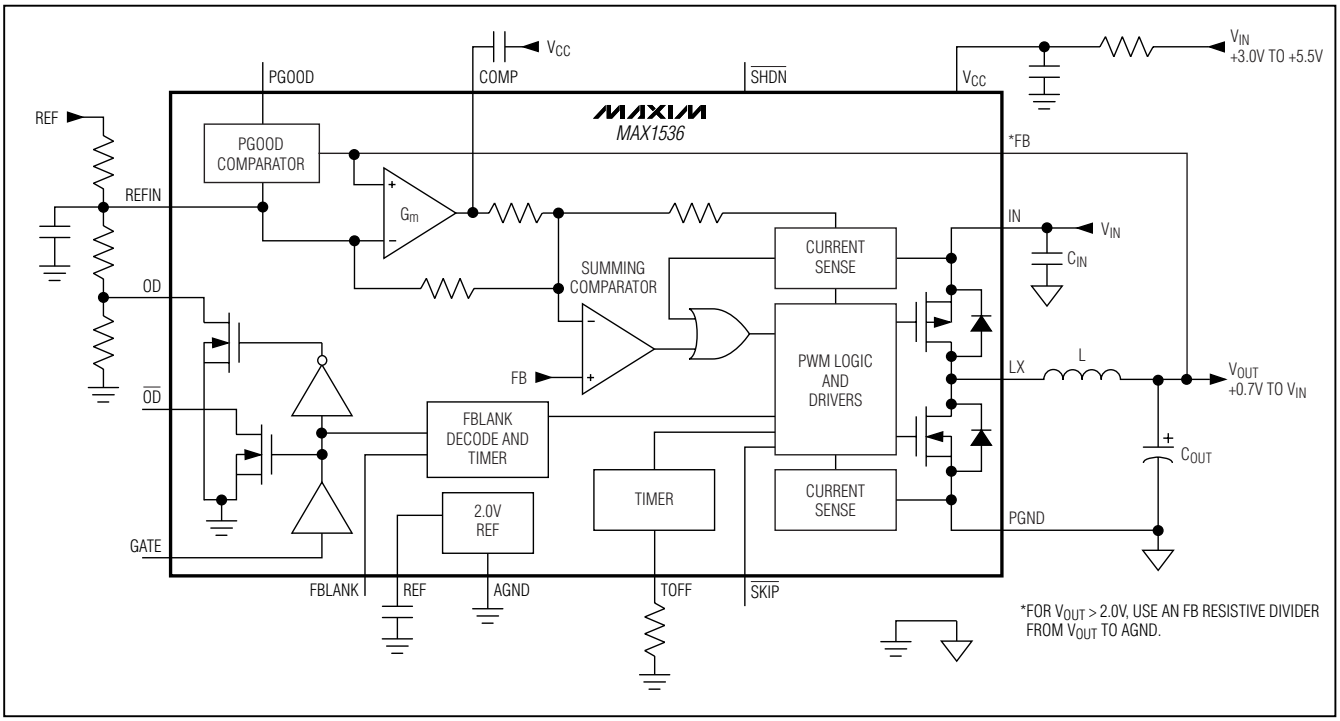

Figure 2. MAX1536 Functional Diagram

extended off-time to control the current. Operation during a short-circuit or overload is similar to forced-PWM mode except the off-time is 4 × t_{OFF}. At the end of each off-time, the PMOS switch turns on and remains on until the output is in regulation or the current through the switch increases to the 4.8A current limit. When the PMOS switch turns off, it remains off for four times the programmed off-time (t_{OFF}), and the NMOS synchronous switch turns on. Since either the NMOS or the PMOS switch is always on, the inductor current is continuous. The RMS inductor current during a short circuit remains below the 4.8A current-limit threshold. The MAX1536 operates using the extended off-time until the short-circuit or overload is removed and $V_{FB} > 0.3 \times V_{REFIN}$. Prolonged short circuit or overload can result in thermal shutdown.

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Shutdown ($\overline{SHDN}$)

Drive $\overline{SHDN}$ low to disable the MAX1536 and reduce the supply current to less than 1µA. In shutdown, all circuitry and internal MOSFETs turn off, and the LX node becomes high impedance. Drive $\overline{SHDN}$ high or connect to V_{CC} for normal operation.

Summing Comparator

Three signals are added together at the input of the summing comparator (Figure 2): an output-voltage error signal relative to the reference voltage, an integrated output-voltage error signal, and the sensed PMOS switch current. The transconductance amplifier with an external capacitor between COMP and V_{CC} provides an integrated error signal. This integrator provides high DC accuracy without the need for a high-gain amplifier (see the *Integrator Amplifier* section).

Power-Good Output (PGOOD)

PGOOD is an open-drain output that indicates if the output voltage is in regulation. PGOOD is actively held low in shutdown and during soft-start. After the soft-start terminates, PGOOD becomes high impedance as long as the output voltage is within ±10% of the nominal regulation voltage.

Once the MAX1536 has started, PGOOD pulls low when the output voltage drops 10% below or rises 10% above the nominal regulation voltage. PGOOD returns to high impedance when the output voltage regains regulation. For logic-level output voltages, connect a 100kΩ external pullup resistor between PGOOD and V_{CC}.

PGOOD is forced high impedance during the transition period selected by FBLANK (see the *Fault Blanking* section).

Table 3. FBLANK Configuration Table

FBLANK	FAULT BLANKING	TYPICAL FORCED-PWM DURATION (µs)
V_{CC}	Enabled	150
Open	Enabled	100
REF	Enabled	50
AGND	Disabled	100

Fault Blanking (FBLANK)

The MAX1536 automatically enters forced-PWM operation for a predefined period following any GATE transition. The FBLANK control input determines how long the MAX1536 maintains forced-PWM operation (Table 3).

When fault blanking is enabled (FBLANK = V_{CC}, open, or REF), the MAX1536 forces PGOOD to a high-impedance state during the transition period selected by FBLANK (Table 3). This prevents the PGOOD signal from going low when the output-voltage change (ΔV_{OUT}) cannot occur as fast as the change in REFIN voltage (ΔV_{REFIN}).

Synchronous Rectification

In a nonsynchronous step-down regulator, an external Schottky diode provides a path for current to flow when the inductor is discharging. The MAX1536 synchronous rectifier replaces the external Schottky diode with an internal low-resistance NMOS switch reducing conduction losses and improving efficiency (Figure 3). There is typically 40ns of delay between MOSFET transitions, thus preventing cross conduction or "shoot through."

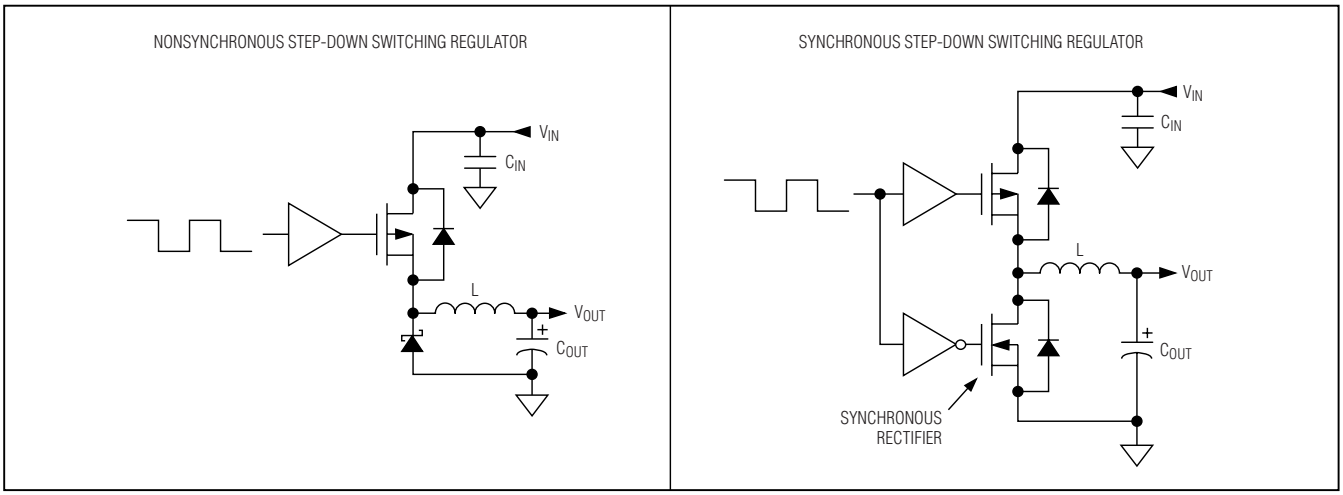

Figure 3. Step-Down Switching Regulator

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Thermal Shutdown

The MAX1536 features a thermal fault-protection circuit. When the junction temperature rises above +165°C, a thermal sensor shuts down the MAX1536 regardless of $V_{\overline{SHDN}}$. The MAX1536 is reactivated after the junction temperature cools to +150°C.

Thermal Resistance

Junction-to-ambient thermal resistance, θ_{JA}, is highly dependent on the amount of copper area connected to the exposed backside pad. Airflow over the board significantly reduces θ_{JA}. For heat-sinking purposes, evenly distribute the copper area connected at the IC among the high-current pins. Refer to the Maxim website (www.maxim-ic.com) for QFN thermal considerations.

Power Dissipation

Power dissipation in the MAX1536 is dominated by conduction losses in the two internal power switches. Power dissipation due to supply current in the control section and average current used to charge and discharge the gate capacitance of the internal switches (i.e., switching losses—P_{SL}) is approximately:

$$P_{SL} = C \times V_{IN}^2 \times f_{SW}$$

where:

C = 5nF.

f_{SW} = switching frequency.

The combined conduction losses (P_{CL}) in the two power switches are approximated by:

$$P_{CL} = I_{OUT}^2 \times R_{PMOS}$$

where:

I_{OUT} = load current.

R_{PMOS} = PMOS switch on-resistance.

The junction-to-ambient thermal resistance required to dissipate this amount of power is calculated by:

$$\theta_{JA} \le \frac{T_{J(MAX)} - T_{A(MAX)}}{P_{SL} + P_{CL}}$$

where:

θ_{JA} = junction-to-ambient thermal resistance.

$T_{J(MAX)}$ = maximum junction temperature = +150°C.

$T_{A(MAX)}$ = maximum ambient temperature.

Design Procedure

For typical applications, use the recommended component values in Table 1. For other applications, take the following steps:

1) Select the desired PWM-mode switching frequency. See Figure 4 for maximum operating frequency.
2) Select the constant off-time as a function of input voltage, output voltage, and switching frequency.
3) Select R_{TOFF} as a function of off-time.
4) Select the inductor as a function of output voltage, off-time, and peak-to-peak inductor current.

Setting the Output Voltage

Setting V_{OUT} with a Resistive Voltage-Divider at FB

The MAX1536 output voltage (V_{OUT}) is set using FB and REFIN (Figure 5). The MAX1536 regulates V_{FB} to be equal to V_{REFIN}. Connect FB to a resistive voltage-divider between V_{OUT} and AGND to adjust V_{OUT} from +0.7V to V_{IN}. Select an R_B from 10kΩ to 100kΩ, then calculate R_A based on the desired V_{OUT}:

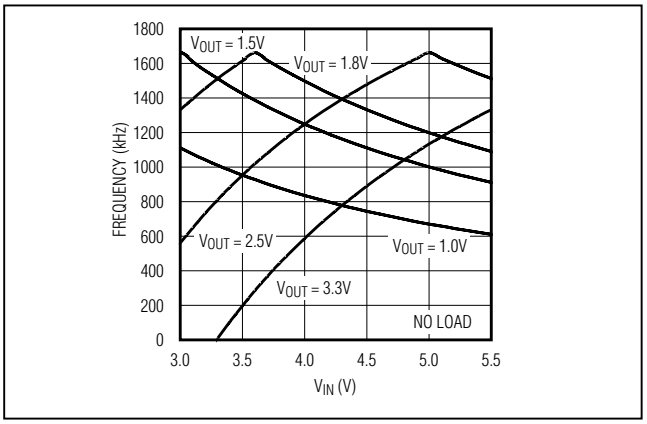

Figure 4. Maximum Recommended Operating Frequency vs. Input Voltage

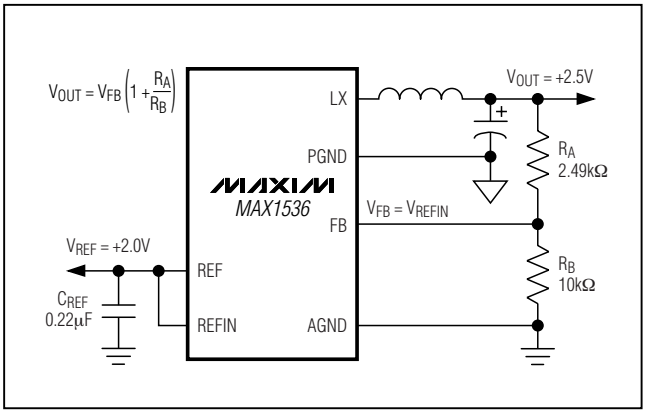

Figure 5. Setting V_{OUT} with a Resistive Voltage-Divider at FB

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$$R_A = R_B \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where $V_{FB} = V_{REFIN}$.

Setting Dynamic Output Voltages with REFIN

The MAX1536 regulates V_{FB} to be equal to V_{REFIN}. Changing V_{REFIN} allows for a dynamic output voltage that changes between two set points (see the *Multioutput Voltage Settings* section for information on three or more output-voltage set points). Figure 1 shows a dynamically adjustable resistive voltage-divider network at REFIN. Keep V_{REFIN} between 0.7V and 2V. Keep V_{REFIN} below V_{CC} - 1.35V to avoid an undervoltage lockout condition. Toggling GATE switches in and out the resistor connected between OD and AGND changing V_{REFIN}. A logic high on GATE turns on the internal N-channel MOSFET, forcing OD to a low-impedance state. A low logic on GATE turns off the internal N-channel MOSFET, making OD high impedance. The output voltage is determined by the following equations:

$$V_{OUT} = V_{FB} \left(1 + \frac{R_A}{R_B} \right)$$

$$V_{FB(LOW)} = V_{REF} \left(\frac{R2}{R1 + R2} \right)$$

$$V_{FB(HIGH)} = V_{REF} \left(\frac{R2 + R3}{R1 + R2 + R3} \right)$$

The MAX1536 automatically enters forced-PWM operation on the rising and falling edges of GATE, and remains in forced-PWM mode for a minimum time selected by FBLANK (Table 3). Forced-PWM operation is required to ensure fast, accurate negative voltage transitions when REFIN is lowered. Since forced-PWM operation disables the zero-crossing comparator, the inductor current can reverse under light loads, quickly discharging the output capacitors. The MAX1536 also forces PGOOD to a high-impedance state for the period selected by FBLANK (Table 3).

For a step-voltage change at REFIN, the rate of change of the output voltage is limited by the inductor current ramp, the total output capacitance, the current limit, and the load during the transition. The voltage across the inductor and the inductance limits the inductor current ramp. The total output capacitance determines how much current is needed to change the output voltage. Additional load current slows down the output voltage change during a positive REFIN voltage change, and speeds up the output voltage change during a negative REFIN voltage change.

Adding a capacitor across REFIN and AGND filters noise and controls the rate of change of the REFIN voltage during dynamic transitions. With the additional capacitance, the REFIN voltage slews between the two set points with a time constant given by the equivalent parallel resistance seen by the slew capacitor C_{REFIN}. As shown in Figure 1, the time constant for a positive REFIN voltage transition is:

$$\tau_{POS} = \left(\frac{R1 \times (R2 + R3)}{R1 + R2 + R3} \right) C_{REFIN}$$

and the time constant for a negative REFIN voltage transition is:

$$\tau_{NEG} = \left(\frac{R1 \times R2}{R1 + R2} \right) C_{REFIN}$$

During a negative REFIN voltage transition, the MAX1536 sinks current to discharge the output capacitor and bring the output voltage down to the new set point. The MAX1536 does not have a negative current limit, so τ_{NEG} must be set long enough to keep the sinking current within the maximum current capability of the IC:

$$\tau_{NEG} \geq \frac{C_{OUT} \times \Delta V_{OUT}}{I_{SINK}} \text{ and } I_{SINK} \leq I_{LIMIT}$$

Programming the No-Load Switching Frequency and Off-Time

The MAX1536 features a programmable PWM mode switching frequency, which is set by the input and output voltage and the value of R_{TOFF}. R_{TOFF} sets the PMOS power switch off-time in PWM mode. Use the following equation to select the off-time according to the desired no-load switching frequency in PWM mode:

$$t_{OFF} = \frac{V_{IN} - V_{OUT}}{f_{PWM} \times V_{IN}}$$

where:

t_{OFF} = the programmed off-time.

V_{IN} = the input voltage.

V_{OUT} = the output voltage.

f_{PWM} = no-load switching frequency, PWM mode.

Select R_{TOFF} according to the formula:

$$R_{TOFF} = (t_{OFF} - 0.07\mu s)\frac{110k\Omega}{1.00\mu s}$$

V_{TOFF} is typically 1.1V and the recommended values for R_{TOFF} range from 30.1kΩ to 499kΩ for off-times of 0.3µs to 4.5µs.

Frequency Variation with Output Current

The operating frequency of the MAX1536 in PWM mode is determined primarily by t_{OFF} (set by R_{TOFF}), V_{IN}, and V_{OUT} as shown in the following formula:

$$f_{PWM} = \frac{V_{IN} - V_{OUT} - V_{PMOS}}{t_{OFF}(V_{IN} - V_{PMOS} + V_{NMOS})}$$

where:

V_{PMOS} = the voltage drop across the internal PMOS power switch, $I_{OUT} \times R_{PMOS}$.

V_{NMOS} = the voltage drop across the internal NMOS synchronous-rectifier switch, $I_{OUT} \times R_{NMOS}$.

As the output current increases, V_{NMOS} and V_{PMOS} increase and the voltage across the inductor decreases. This causes the frequency to drop. Approximate the change in frequency with the following formula:

$$\Delta f_{PWM} = -\frac{I_{OUT} \times R_{PMOS}}{V_{IN} \times t_{OFF}}$$

where R_{PMOS} is the resistance of the internal MOSFETs (54mΩ, typ).

Inductor Selection

The key inductor parameters must be specified: inductor value (L) and peak current (I_{PEAK}). The following equation includes a constant, denoted as LIR, which is the ratio of peak-to-peak inductor AC ripple current to maximum DC load current. A higher value of LIR allows smaller inductance but results in higher losses and ripple. A good compromise between size and losses is found at approximately a 25% ripple-current to load-current ratio (LIR = 0.25), which corresponds to a peak-inductor current 1.125 times the DC load current:

$$L = \frac{V_{OUT} \times t_{OFF}}{I_{OUT} \times LIR}$$

where:

I_{OUT} = maximum DC load current.

LIR = ratio of peak-to-peak AC inductor current to DC load current, typically 0.25.

The peak-inductor current at full load is 1.125 × I_{OUT} if the above equation is used; otherwise, the peak current is calculated by:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT} \times t_{OFF}}{2 \times L}$$

Choose an inductor with a saturation current at least as high as the peak-inductor current. The inductor selected should exhibit low losses at the chosen operating frequency.

Capacitor Selection

The input-filter capacitor reduces peak currents and noise at the voltage source. Use a low-ESR and low-ESL capacitor located no further than 5mm from IN. Select the input capacitor according to the RMS input ripple-current requirements and voltage rating:

$$I_{RIPPLE} = I_{LOAD}\frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where I_{RIPPLE} = input RMS current ripple.

The output-filter capacitor affects the output-voltage ripple, output load-transient response, and feedback-loop stability. For stable operation, the MAX1536 requires a minimum output ripple voltage of $V_{RIPPLE} \geq 1\% \times V_{OUT}$.

The minimum ESR of the output capacitor is calculated by:

$$ESR > 1\% \times \frac{L}{t_{OFF}}$$

Stable operation requires the correct output-filter capacitor. When choosing the output capacitor, ensure that:

$$C_{OUT} \geq \frac{t_{OFF}}{V_{OUT}} \times \frac{79\mu F \times 1V}{1\mu s}$$

Integrator Amplifier

An internal transconductance amplifier fine tunes the output DC accuracy. A capacitor, C_{COMP}, from COMP to V_{CC} compensates the transconductance amplifier. For stability, choose C_{COMP} = 470pF. A larger capacitor value maintains a constant average output voltage, but slows the loop response to changes in output voltage. A smaller capacitor value speeds up the loop response to changes in output voltage but decreases stability.

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Applications Information

Multioutput Voltage Settings

The MAX1536 is optimized to work in applications that require two dynamic output voltages; however, discrete logic or a DAC connected to REFIN allows three or more dynamic output voltages.

Figure 6 shows an application circuit providing four voltage levels using discrete logic. Switching resistors in and out of the resistor network changes the voltage at REFIN. An edge-detection circuit is added to trigger a 1µs pulse on GATE to start the fault-blanking and forced-PWM operation. GATE requires a minimum pulse width of 500ns. The edge-detection circuit is not required if the MAX1536 is always in PWM mode ($\overline{SKIP}$ = V_{CC}) and fault blanking is not necessary.

Active Bus Termination

Active bus termination power supplies generate a voltage rail that tracks a set reference. Active bus termination power supplies are unique because they source and sink current. DDR memory architecture requires active bus termination. In DDR memory architecture, the termination voltage is set at exactly half the memory supply voltage. Configure the MAX1536 to generate the termination voltage using a resistor-divider at REFIN. Force the MAX1536 to operate in PWM mode ($\overline{SKIP}$ = V_{CC}) to source and sink current. Figure 7 shows the MAX1536 configured as a DDR termination regulator. Connect GATE and FBLANK to AGND when unused.

Circuit Layout and Grounding

Good layout is necessary to achieve the intended output power level, high efficiency, and low noise. Good layout includes the use of a ground plane, careful component placement, and correct routing of traces using appropriate trace widths. Refer to the MAX1536 EV Kit for layout reference.

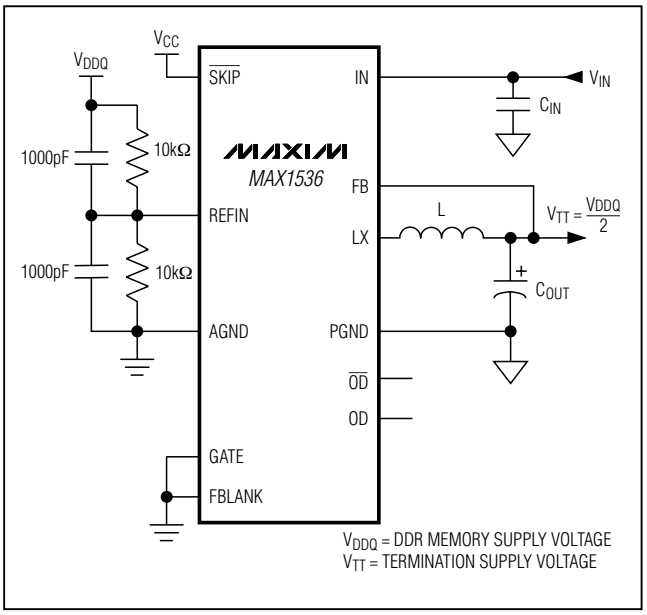


Figure 7. Active Bus Termination

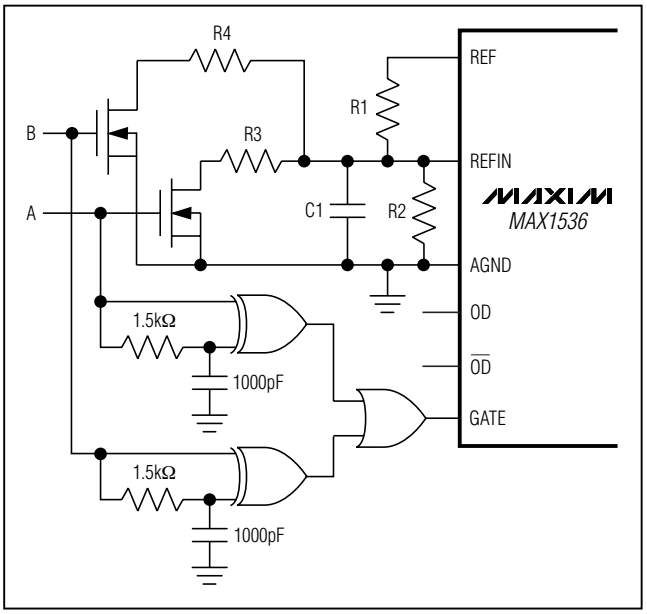


Figure 6. Multioutput Voltage Settings

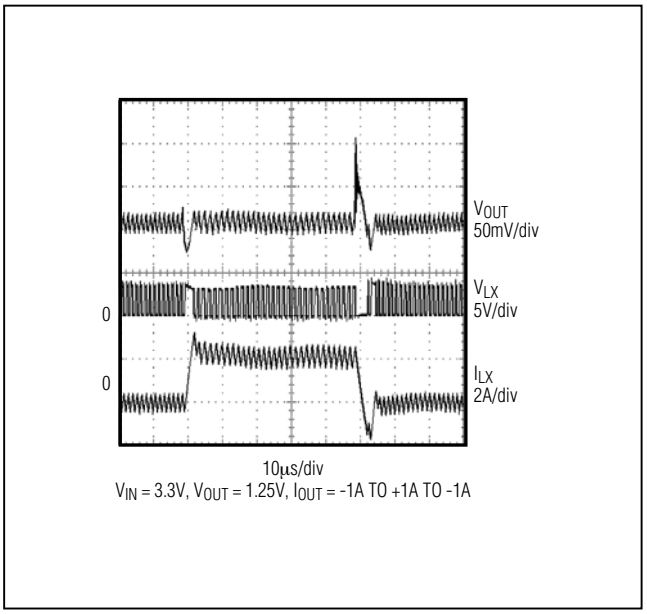


Figure 8. Source/Sink Waveforms

The following points are in order of decreasing importance:

1) Minimize switched-current and high-current ground loops. Connect the input capacitor's ground, the output capacitor's ground, and PGND at a single point. Connect the resulting island to AGND at only one point.
2) Connect the input filter capacitor less than 5mm away from IN. The connecting copper trace carries large currents and must be at least 1mm wide, preferably 2.5mm.
3) Place the LX node components as close together and as near to the device as possible. This reduces noise, resistive losses, and switching losses.
4) A ground plane is essential for optimal performance. In most applications, the circuit is located on a multilayer board, and full use of the four or more layers is recommended. Use the top and bottom layers for interconnections and the inner layers for an uninterrupted ground plane. Avoid large AC currents through the ground plane.

Chip Information

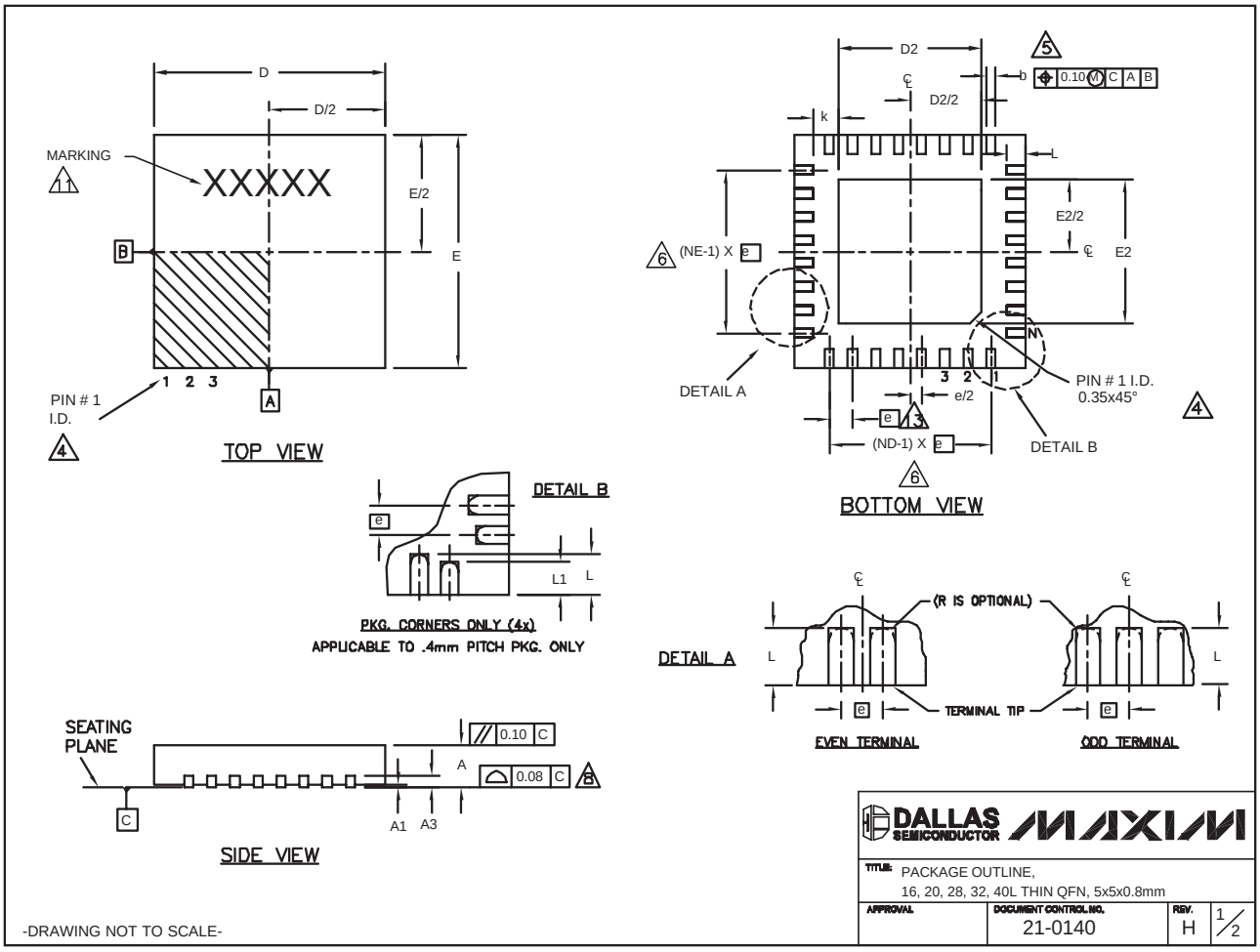
TRANSISTOR COUNT: 4305
PROCESS: BiCMOS

3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



3.6A, 1.4MHz, Low-Voltage, Internal-Switch Step-Down Regulator with Dynamic Output Voltage Control

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	0.35	0.45
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	-	-	-	-	-	-	-	-	-	-	-	-	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS								
PKG. CODES	D2			E2			L	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.15	
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	**	YES
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	**	NO
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	**	YES
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40	YES
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	**	NO
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	**	YES
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	**	NO
T4055-1	3.20	3.30	3.40	3.20	3.30	3.40	**	YES

** SEE COMMON DIMENSIONS TABLE

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-1, T2855-3, AND T2855-6.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16, 20, 28, 32, 40L THIN QFN, 5x5x0.8mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	H	2/2