RELIABILITY REPORT

FOR

MAX1555EZK

PLASTIC ENCAPSULATED DEVICES

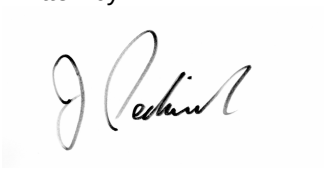
August 28, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

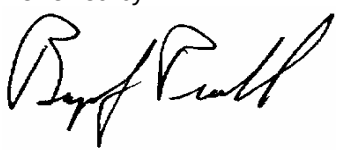
SUNNYVALE, CA 94086

Written by



Jim Pedicord
Quality Assurance
Reliability Lab Manager

Reviewed by



Bryan J. Preeshl
Quality Assurance
Executive Director

Conclusion

The MAX1555 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. .....Device Description
II. .....Manufacturing Information
III. .....Packaging Information
IV. .....Die Information
V. .....Quality Assurance Information
VI. .....Reliability Evaluation
.....Attachments

I. Device Description

A. General

The MAX1555 charges a single-cell lithium-ion (Li+) battery from both USB* and AC adapter sources. It operates with no external FETs or diodes, and accept operating input voltages up to 7V.

On-chip thermal limiting simplifies PC board layout and allows optimum charging rate without the thermal limits imposed by worst-case battery and input voltage. When the MAX1551 thermal limits are reached, the charger does not shut down, but progressively reduces charging current.

The MAX1555 includes a POK-bar output to indicate when input power is present. The MAX1555 features a CHG-bar output to indicate charging.

With USB connected, but without DC power, charge current is set to 100mA (max). This allows charging from both powered and unpowered USB hubs with no port communication required. When DC power is connected, charging current is set at 280mA (typ). No input-blocking diodes are required to prevent battery drain.

The MAX1555 is available in 5-pin thin SOT23 packages and operates over a -40°C to +85°C range.

B. Absolute Maximum Ratings

Item	Rating
DC to GND	0 to +8V
DC to BAT	0 to +7V
BAT, CHG, POK, USB to GND	-0.3V to +7V
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-40°C to +150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation (TA = +70°C)	
5-Pin Thin SOT23	727mW
Derates above +70°C	
5-Pin Thin SOT23	9.1mW/°C

II. Manufacturing Information

A. Description/Function:	SOT23 Dual-Input USB/AC Adapter 1-Cell Li+ Battery Charger
B. Process:	B8 - Standard 8 micron silicon gate CMOS
C. Number of Device Transistors:	541
D. Fabrication Location:	California, USA
E. Assembly Location:	Philippines
F. Date of Initial Production:	June, 2003

III. Packaging Information

A. Package Type:	**5-Lead SOT23**
B. Lead Frame:	Copper
C. Lead Finish:	Solder Plate
D. Die Attach:	Silver-filled Epoxy
E. Bondwire:	Gold (1.0 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	Buildsheet # 05-9000-0523
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-A112:	Level 1

IV. Die Information

A. Dimensions:	59 X 40 mils
B. Passivation:	Si_3N_4/SiO_2 (Silicon nitride/ Silicon dioxide)
C. Interconnect:	TiW/ AlCu/ TiWN
D. Backside Metallization:	None
E. Minimum Metal Width:	.8 microns (as drawn)
F. Minimum Metal Spacing:	.8 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director of QA)
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 48 \times 2}$$

(Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 22.62 \times 10^{-9}$ $\lambda = 22.62$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability qualification and monitor programs. Maxim also performs weekly Burn-In on samples from production to assure reliability of its processes. The reliability required for lots which receive a burn-in qualification is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on rejects from lots exceeding this level. The Burn-In Schematic (Spec.# 06-6146) shows the static circuit used for this test. Maxim also performs 1000 hour life test monitors quarterly for each process. This data is published in the Product Reliability Report (**RR-1M**) located on the Maxim website at http://www.maxim-ic.com .

B. Moisture Resistance Tests

Maxim evaluates pressure pot stress from every assembly process during qualification of each new design. Pressure Pot testing must pass a 20% LTPD for acceptance. Additionally, industry standard 85°C/85%RH or HAST tests are performed quarterly per device/package family.

B. E.S.D. and Latch-Up

PN20-1 die type has been found to have all pins able to withstand a transient pulse of ±1000V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX1555EZK

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)				
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0
Moisture Testing (Note 2)				
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality	77	0
Mechanical Stress (Note 2)				
Temperature Cycle	-65°C/150°C 1000 Cycles Method 1010	DC Parameters & functionality	77	0

Note 1: Life Test Data may represent plastic D.I.P. qualification lots.
Note 2: Generic process/package data

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

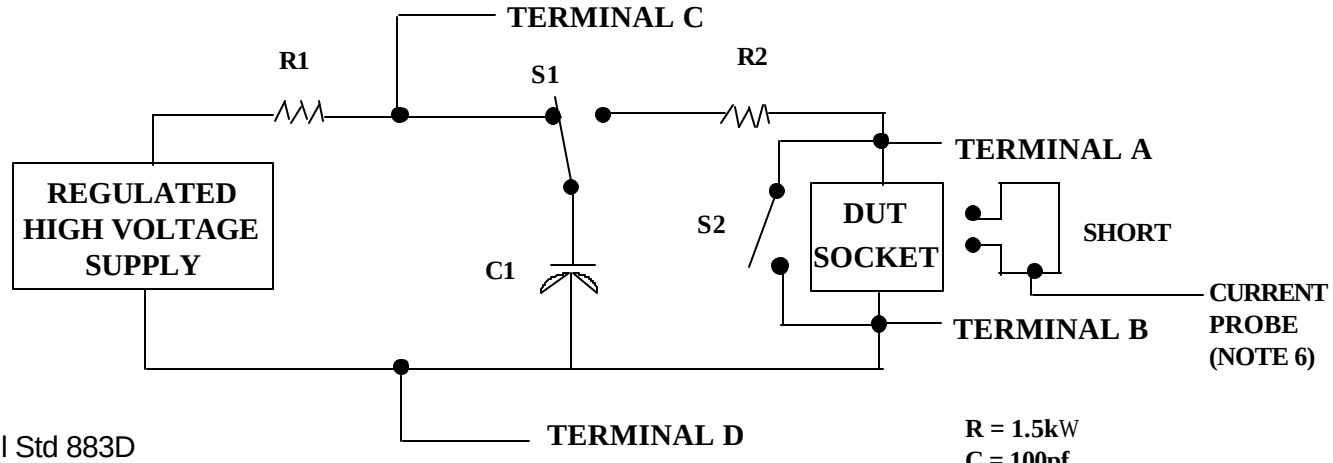
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

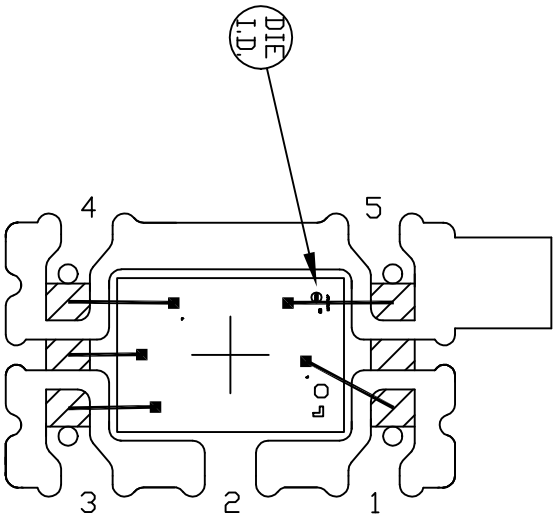
b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



Mil Std 883D
Method 3015.7
Notice 8

THIN SOT PACKAGE

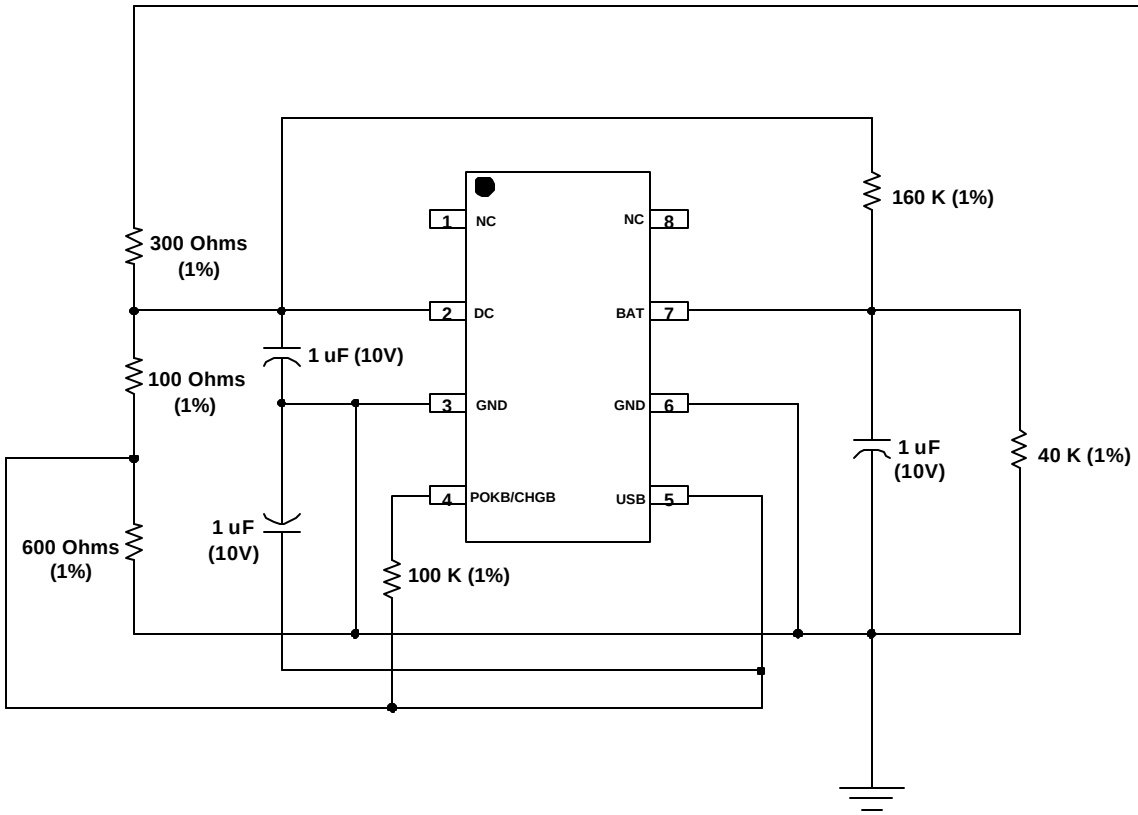


CAVITY DOWN

BONDABLE AREA

PKG. CODE: Z5-1		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: 63×44	PKG.			BOND DIAGRAM #: 05-9000-0523	REV: A
	DESIGN				

ONCE PER SOCKET



DEVICES: MAX 1551ESA/1555ESA (PN20Z)
PACKAGE: 8-NSO
MAX. EXPECTED CURRENT = 12mA

DRAWN BY: TEK TAN
NOTES:

DOCUMENT I.D. 06-6146	REVISION B	*MAXIM* TITLE: BI Circuit (MAX1551/1555) PN20Z