**MOTOROLA**
**SEMICONDUCTOR TECHNICAL DATA**

# Multi-Character
# LED Display/Lamp Driver
## CMOS

The MC14489B is a flexible light–emitting–diode driver which directly in-terfaces to individual lamps, 7–segment displays, or various combinations of both. LEDs wired with common cathodes are driven in a multiplexed–by–5 fashion. Communication with an MCU/MPU is established through a synchro-nous serial port. The MC14489B features data retention plus decode and scan circuitry, thus relieving processor overhead. A single, current–setting resistor is the only ancillary component required.

A single device can drive any one of the following: a 5–digit display plus decimals, a 4–1/2–digit display plus decimals and sign, or 25 lamps. A special technique allows driving 5 1/2 digits; see Figure 16. A configuration register allows the drive capability to be partitioned off to suit many additional applica-tions. The on–chip decoder outputs 7–segment–format numerals 0 to 9, hexa-decimal characters A to F, plus 15 letters and symbols.

The MC14489B is compatible with the Motorola SPI and National MI-CRO-WIRE[TM] serial data ports. The chip's patented BitGrabber[TM] registers augment the serial interface by allowing random access without steering or address bits. A 24–bit transfer updates the display register. Changing the con-figuration register requires an 8–bit transfer.

- Operating Voltage Range of Drive Circuitry: 4.5 to 5.5 V
- Operating Junction Temperature Range: – 40° to 130°C
- Current Sources Controlled by Single Resistor Provide Anode Drive
- Low–Resistance FET Switches Provide Direct Common Cathode Interface
- Low–Power Mode (Extinguishes the LEDs) and Brightness Controlled via Serial Port
- Special Circuitry Minimizes EMI when Display is Driven and Eliminates EMI in Low–Power Mode
- Power–On Reset (POR) Blanks the Display on Power–Up, Independent of Supply Ramp Up Time
- May Be Used with Double–Heterojunction LEDs for Optimum Efficiency
- Chip Complexity: 4300 Elements (FETs, Resistors, Capacitors, etc.)
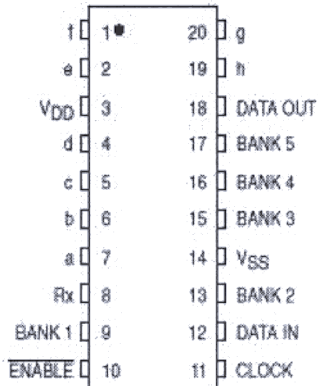
## MC14489B

P SUFFIX
PLASTIC DIP
CASE 738

DW SUFFIX
SOG PACKAGE
CASE 751D

**ORDERING INFORMATION**

| | |
|---|---|
| MC14489BP | Plastic DIP |
| MC14489BDW | SOG Package |

**PIN ASSIGNMENT**

| | | | |
|---|---|---|---|
| f | 1 | 20 | g |
| e | 2 | 19 | h |
| V$_{DD}$ | 3 | 18 | DATA OUT |
| d | 4 | 17 | BANK 5 |
| c | 5 | 16 | BANK 4 |
| b | 6 | 15 | BANK 3 |
| a | 7 | 14 | V$_{SS}$ |
| Rx | 8 | 13 | BANK 2 |
| BANK 1 | 9 | 12 | DATA IN |
| ENABLE | 10 | 11 | CLOCK |

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MICROWIRE is a trademark of National Semiconductor Corp.

**REV 0**
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**MOTOROLA**

## BLOCK DIAGRAM
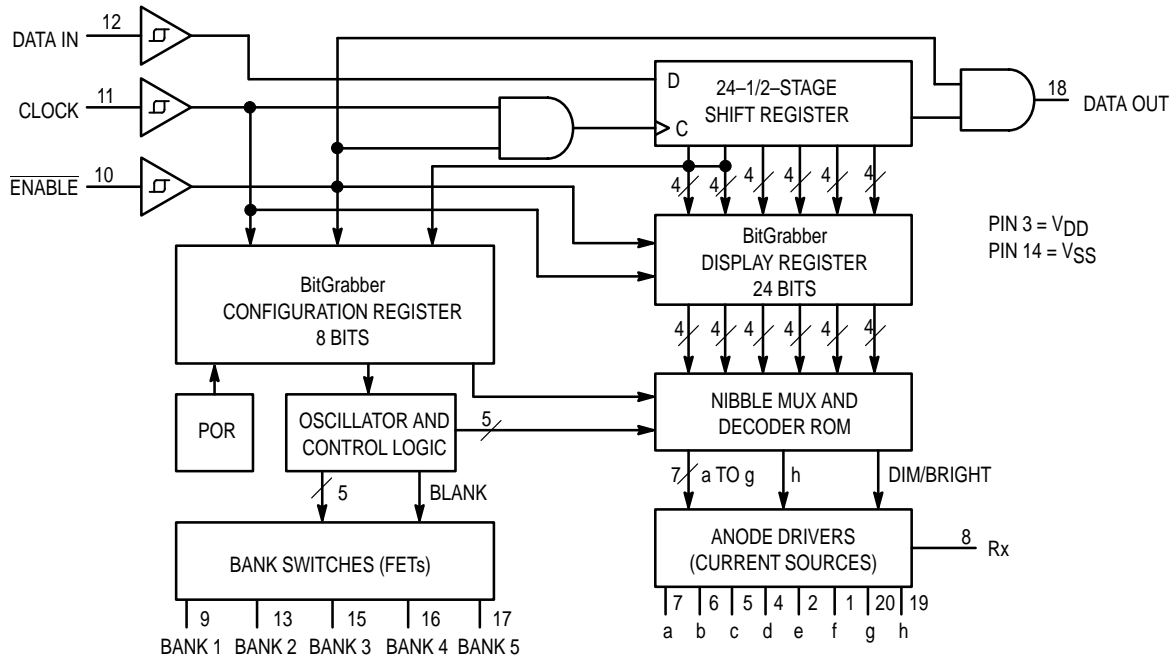


## MAXIMUM RATINGS* (Voltages Referenced to $V_{SS}$)

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{DD}$ | DC Supply Voltage | – 0.5 to + 6.0 | V |
| $V_{in}$ | DC Input Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage | – 0.5 to $V_{DD}$ + 0.5 | V |
| $I_{in}$ | DC Input Current — per Pin (Includes Pin 8) | ± 15 | mA |
| $I_{out}$ | DC Output Current — Pins 1, 2, 4 – 7, 19, 20 Sourcing / Sinking | – 40 / 10 | mA |
| | Pins 9, 13, 15, 16, 17 Sinking | 320 | |
| | Pin 18 | ± 15 | |
| $I_{DD}$, $I_{SS}$ | DC Supply Current, $V_{DD}$ and $V_{SS}$ Pins | ± 350 | mA |
| $T_J$ | Chip Junction Temperature | – 40 to + 130 | °C |
| $R_{\theta JA}$ | Device Thermal Resistance, Junction–to–Ambient (see Thermal Considerations section)   Plastic DIP / SOG Package | 90 / 100 | °C/W |
| $T_{stg}$ | Storage Temperature | – 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds | 260 | °C |

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Descriptions section.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$, $T_J$ = – 40° to 130°C* unless otherwise indicated)

| Symbol | Parameter | Test Condition | $V_{DD}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Power Supply Voltage Range of LED Drive Circuitry | | — | 4.5 to 5.5 | V |
| $V_{DD}$ (stby) | Minimum Standby Voltage | Bits Retained in Display and Configuration Registers, Data Port Fully Functional | — | 3.0 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage (Data In, Clock, $\overline{Enable}$) | | 3.0<br>5.5 | 0.9<br>1.65 | V |
| $V_{IH}$ | Minimum High–Level Input Voltage (Data In, Clock, $\overline{Enable}$) | | 3.0<br>5.5 | 2.1<br>3.85 | V |
| $V_{Hys}$ | Minimum Hysteresis Voltage (Data In, Clock, $\overline{Enable}$) | | 3.0<br>5.5 | 0.2<br>0.4 | V |
| $V_{OL}$ | Maximum Low–Level Output Voltage (Data Out) | $I_{out}$ = 20 µA | 3.0<br>5.5 | 0.1<br>0.1 | V |
| | | $I_{out}$ = 1.3 mA | 4.5 | 0.4 | |
| $V_{OH}$ | Minimum High–Level Output Voltage (Data Out) | $I_{out}$ = – 20 µA | 3.0<br>5.5 | 2.9<br>5.4 | V |
| | | $I_{out}$ = – 800 µA | 4.5 | 4.1 | |
| $I_{in}$ | Maximum Input Leakage Current (Data In, Clock, $\overline{Enable}$) | $V_{in}$ = $V_{DD}$ or $V_{SS}$ | 5.5 | ± 2.0 | µA |
| | | $V_{in}$ = $V_{DD}$ or $V_{SS}$, $T_J$ = 25°C only | 5.5 | ± 0.1 | |
| $i_{OL}$ | Minimum Sinking Current (a, b, c, d, e, f, g, h) | $V_{out}$ = 1.0 V | 4.5 | 0.2 | mA |
| $i_{OH}$ | Peak Sourcing Current — See Figure 7 for currents up to 35 mA (a, b, c, d, e, f, g, h) | Rx = 2.0 kΩ, $V_{out}$ = 3.0 V, Dimmer Bit = High | 5.0 | 13 to 17.5 | mA |
| | | Rx = 2.0 kΩ, $V_{out}$ = 3.0 V, Dimmer Bit = Low | 5.0 | 6 to 9 | |
| $I_{OZ}$ | Maximum Output Leakage Current (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5) | $V_{out}$ = $V_{DD}$ (FET Leakage) | 5.5 | 50 | µA |
| | | $V_{out}$ = $V_{DD}$ (FET Leakage), $T_J$ = 25°C only | 5.5 | 1 | |
| | | $V_{out}$ = $V_{SS}$ (Protection Diode Leakage) | 5.5 | 1 | |
| $R_{on}$ | Maximum ON Resistance (Bank 1, Bank 2, Bank 3, Bank 4, Bank 5) | $I_{out}$ = 0 to 200 mA | 5.0 | 10 | Ω |
| $I_{DD}$, $I_{SS}$ | Maximum Quiescent Supply Current | Device in Low–Power Mode, $V_{in}$ = $V_{SS}$ or $V_{DD}$, Rx in Place, Outputs Open | 5.5 | 100 | µA |
| | | Same as Above, $T_J$ = 25°C | 5.5 | 20 | |
| $I_{SS}$ | Maximum RMS Operating Supply Current (The $V_{SS}$ leg does not contain the Rx current component. See Pin Descriptions.) | Device NOT in Low–Power Mode, $V_{in}$ = $V_{SS}$ or $V_{DD}$, Outputs Open | 5.5 | 1.5 | mA |

* See Thermal Considerations section.

**AC ELECTRICAL CHARACTERISTICS** ($T_J$ = – 40° to 130°C*, $C_L$ = 50 pF, Input $t_r$ = $t_f$ = 10 ns)

| Symbol | Parameter | $V_{DD}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|
| $f_{clk}$ | Serial Data Clock Frequency, Single Device or Cascaded Devices<br>NOTE: Refer to Clock $t_w$ below<br>(Figure 1) | 3.0<br>4.5<br>5.5 | dc to 3.0<br>dc to 4.0<br>dc to 4.0 | MHz |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Clock to Data Out<br>(Figures 1 and 5) | 3.0<br>4.5<br>5.5 | 140<br>80<br>80 | ns |
| $t_{TLH}$,<br>$t_{THL}$ | Maximum Output Transistion Time, Data Out<br>(Figures 1 and 5) | 3.0<br>4.5<br>5.5 | 70<br>50<br>50 | ns |
| $f_R$ | Refresh Rate — Bank 1 through Bank 5<br>(Figures 2 and 6) | 3.0<br>4.5<br>5.5 | NA<br>700 to 1900<br>700 to 1900 | Hz |
| $C_{in}$ | Maximum Input Capacitance — Data In, Clock, $\overline{Enable}$ | — | 10 | pF |

* See Thermal Considerations section.

**TIMING REQUIREMENTS** ($T_J$ = – 40° to 130°C*, Input $t_r$ = $t_f$ = 10 ns unless otherwise indicated)

| Symbol | Parameter | $V_{DD}$ V | Guaranteed Limit | Unit |
|---|---|---|---|---|
| $t_{su}$, $t_h$ | Minimum Setup and Hold Times, Data In versus Clock<br>(Figure 3) | 3.0<br>4.5<br>5.5 | 50<br>40<br>40 | ns |
| $t_{su}$, $t_h$,<br>$t_{rec}$ | Minimum Setup, Hold, ** and Recovery Times, $\overline{Enable}$ versus Clock<br>(Figure 4) | 3.0<br>4.5<br>5.5 | 150<br>100<br>100 | ns |
| $t_{w(L)}$ | Minimum Active–Low Pulse Width, $\overline{Enable}$<br>(Figure 4) | 3.0<br>4.5<br>5.5 | 4.5<br>3.4<br>3.4 | µs |
| $t_{w(H)}$ | Minimum Inactive–High Pulse Width, $\overline{Enable}$<br>(Figure 4) | 3.0<br>4.5<br>5.5 | 300<br>150<br>150 | ns |
| $t_w$ | Minimum Pulse Width, Clock<br>(Figure 1) | 3.0<br>4.5<br>5.5 | 167<br>125<br>125 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times — Data In, Clock, $\overline{Enable}$<br>(Figure 1) | 3.0<br>4.5<br>5.5 | 1<br>1<br>1 | ms |

* See Thermal Considerations section.

** For a high–speed 8–Clock access, $t_h$ for $\overline{Enable}$ is determined as follows:

$V_{DD}$ = 3 to 4.5 V, $f_{clk}$ > 1.78 MHz: $t_h$ = 4350 – (7500/$f_{clk}$)
$V_{DD}$ = 4.5 to 5.5 V, $f_{clk}$ > 2.34 MHz: $t_h$ = 3300 – (7500/$f_{clk}$)
where $t_h$ is in ns and $f_{clk}$ is in MHz.

NOTES:
1. This restriction does NOT apply for $f_{clk}$ rates less than those listed above. For "slow" $f_{clk}$ rates, use the $t_h$ limits in the above table.
2. This restriction does NOT apply for an access involving more than 8 Clocks. For > 8 Clocks, use the $t_h$ limits in the above table.
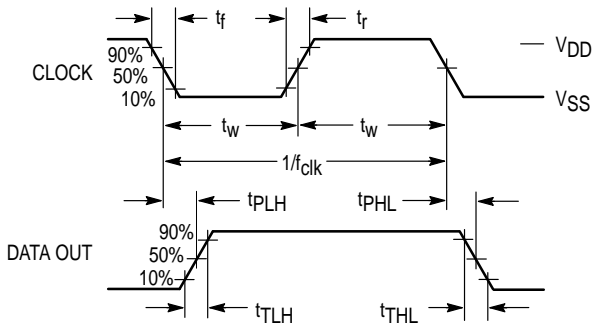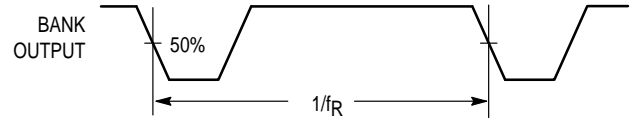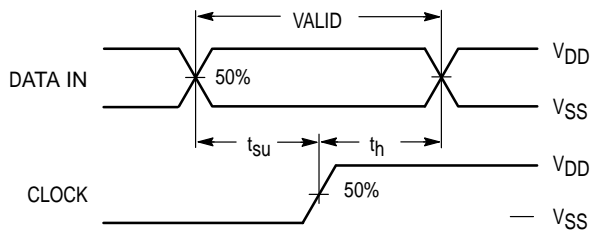
**Figure 1.**



**Figure 2.**



**Figure 3.**



**Figure 4.**



*Includes all probe and fixture capacitance.

**Figure 5.**



*Includes all probe and fixture capacitance.
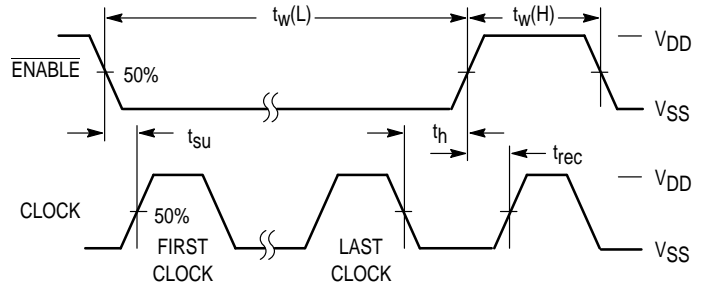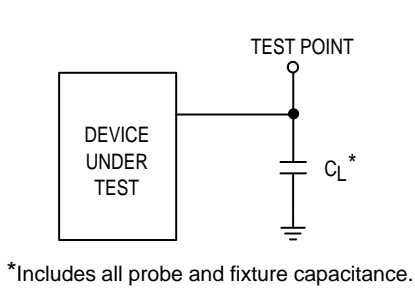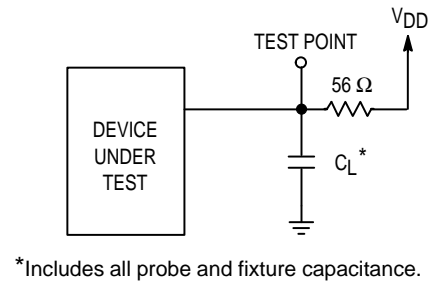
**Figure 6.**

# PIN DESCRIPTIONS

## DIGITAL INTERFACE

### Data In (Pin 12)

Serial Data Input. The bit stream begins with the MSB and is shifted in on the low–to–high transition of Clock. When the device is not cascaded, the bit pattern is either 1 byte (8 bits) long to change the configuration register or 3 bytes (24 bits) long to update the display register. For two chips cascaded, the pattern is either 4 or 6 bytes, respectively. The display does not change during shifting (until $\overline{Enable}$ makes a low–to–high transition) which allows slow serial data rates, if desired.

The bit stream needs neither address nor steering bits due to the innovative BitGrabber registers. Therefore, all bits in the stream are available to be data for the two registers. Random access of either register is provided. That is, the registers may be accessed in any sequence. Data is retained in the registers over a supply range of 3 to 5.5 V. Formats are shown in Figures 8 through 14 and summarized in Table 2. Information on the segment decoder is given in Table 1.

Data In typically switches near 50% of $V_{DD}$ and has a Schmitt–triggered input buffer. These features combine to maximize noise immunity for use in harsh environments and bus applications. This input can be directly interfaced to CMOS devices with outputs guaranteed to switch near rail–to–rail. When interfacing to NMOS or TTL devices, either a level shifter (MC14504B, MC74HCT04A) or pullup resistor of 1 kΩ to 10 kΩ must be used. Parameters to be considered when sizing the resistor are the worst–case $I_{OL}$ of the driving device, maximum tolerable power consumption, and maximum data rate.

### Clock (Pin 11)

Serial Data Clock Input. Low–to–high transitions on Clock shift bits available at Data In, while high–to–low transitions shift bits from Data Out. The chip's 24–1/2–stage shift register is static, allowing clock rates down to dc in a continuous or intermittent mode. The Clock input does not need to be synchronous with the on–chip clock oscillator which drives the multiplexing circuit.

Eight clock cycles are required to access the configuration register, while 24 are needed for the display register when the MC14489B is not cascaded. See Figures 8 and 9.

As shown in Figure 10, two devices may be cascaded. In this case, 32 clock cycles access the configuration register and 48 access the display register, as depicted in Figure 10.

Cascading of 3, 4, 5, and 6 devices is shown in Figures 11, 12, 13, and 14, respectively. Also, reference Table 2.

Clock typically switches near 50% of $V_{DD}$ and has a Schmitt–triggered input buffer. Slow Clock rise and fall times are tolerated. See the last paragraph of **Data In** for more information.

#### NOTE

To guarantee proper operation of the power–on reset (POR) circuit, the Clock pin must NOT be floated or toggled during power–up. That is, the Clock pin must be **stable** until the $V_{DD}$ pin reaches at least 3 V.

If control of the Clock pin during power–up is not practical, then the MC14489B must be reset via bit C0 in the C register. To accomplish this, C0 is reset low, then set high.

### $\overline{Enable}$ (Pin 10)

Active–Low Enable Input. This pin allows the MC14489B to be used on a serial bus, sharing Data In and Clock with other peripherals. When $\overline{Enable}$ is in an inactive high state, Data Out is forced to a known (low) state, shifting is inhibited, and the port is held in the initialized state. To transfer data to the device, $\overline{Enable}$ (which initially must be inactive high) is taken low, a serial transfer is made via Data In and Clock, and $\overline{Enable}$ is taken high. The low–to–high transition on $\overline{Enable}$ transfers data to either the configuration or display register, depending on the data stream length.

Every rising edge on $\overline{Enable}$ initiates a blanking interval while data is loaded. Thus, continually loading the device with the same data may cause the LEDs on some banks to appear dimmer than others.

#### NOTE

Transitions on $\overline{Enable}$ must not be attempted while Clock is high. This puts the device out of synchronization with the microcontroller. Resynchronization occurs when $\overline{Enable}$ is high and Clock is low.

This input is also Schmitt–triggered and switches near 50% of $V_{DD}$, thereby minimizing the chance of loading erroneous data in the registers. See the last paragraph of **Data In** for more information.

### Data Out (Pin 18)

Serial Data Output. Data is transferred out of the shift register through Data Out on the high–to–low transition of Clock. This output is a no connect, unless used in one of the manners discussed below.

When cascading MC14489B's, Data Out feeds Data In of the next device per Figures 10, 11, 12, 13, and 14.

Data Out could be fed back to an MCU/MPU to perform a wrap–around test of serial data. This could be part of a system check conducted at power–up to test the integrity of the system's processor, pc board traces, solder joints, etc.

The pin could be monitored at an in–line Q.A. test during board manufacturing.

Finally, Data Out facilitates troubleshooting a system.

## DISPLAY INTERFACE

### Rx (Pin 8)

External Current–Setting Resistor. A resistor tied between this pin and ground ($V_{SS}$) determines the peak segment drive current delivered at pins a through h. Pin 8's resistor ties into a current mirror with an approximate current gain of 10 when bit D23 = high (brighten). With D23 = low, the peak current is reduced about 50%. Values for Rx range from 700 Ω to infinity. When Rx = ∞ (open circuit), the display is extinguished. For proper current control, resistors having ± 1% tolerance should be used. See Figure 7.

#### CAUTION

Small Rx values may cause the chip to overheat if precautions are not observed. See **Thermal Considerations.**

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**a through h (Pins 1, 2, 4 – 7, 19, 20)**

Anode–Driver Current Sources. These outputs are closely–matched current sources which directly tie to the anodes of external discrete LEDs (lamps) or display segment LEDs. Each output is capable of sourcing up to 35 mA.

When used with lamps, outputs a, b, c, and d are used to independently control up to 20 lamps. Output h is used to control up to 5 lamps dependently. (See Figure 17.) For lamps, the *No Decode* mode is selected via the configuration register, forcing e, f, and g inactive (low).

When used with segmented displays, outputs a through g drive segments a through g, respectively. Output h is used to drive the decimals. Refer to Figure 9. If unused, h must be left open.

**Bank 1 through Bank 5 (Pins 9, 13, 15, 16, 17)**

Diode–Bank FET Switches. These outputs are low–resistance switches to ground ($V_{SS}$) capable of handling currents of up to 320 mA each. These pins directly tie to the common cathodes of segmented displays or the cathodes of lamps (wired with cathodes common).

The display is refreshed at a nominal 1 kHz rate to achieve optimum brightness from the LEDs. A 20% duty cycle is utilized.

Special design techniques are used on–chip to accommodate the high currents with low EMI (electromagnetic interference) and minimal spiking on the power lines.

## POWER SUPPLY

### $V_{SS}$ (Pin 14)

Most–negative supply potential. This pin is usually ground.
Resistor Rx is externally tied to ground ($V_{SS}$). Therefore, the chip's $V_{SS}$ pin does not contain the Rx current component.

### $V_{DD}$ (Pin 13)

Most–positive supply potential.
To guarantee data integrity in the registers and to ensure the serial interface is functional, this voltage may range from 3 to 6 volts with respect to $V_{SS}$. For example, within this voltage range, the chip could be placed in and out of the low–power mode.
To adequately drive the LEDs, this voltage must be 4.5 to 6 volts with respect to $V_{SS}$.
The $V_{DD}$ pin contains the Rx current component plus the chip's current drain. In the low–power mode, the current mirror and clock oscillator are turned off, thus significantly reducing the $V_{DD}$ current, $I_{DD}$.
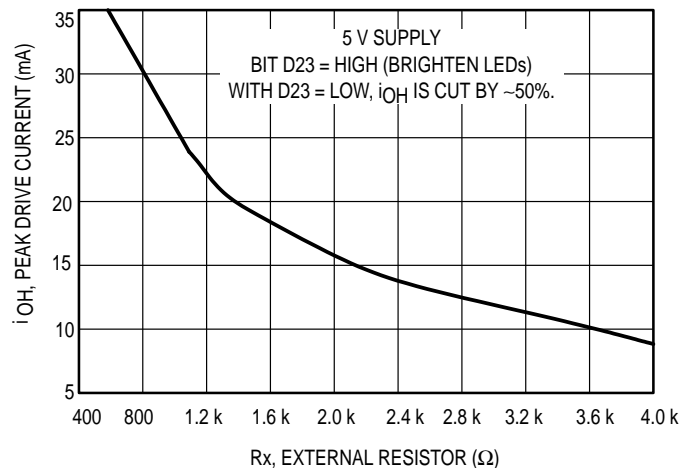


NOTE: Drive current tolerance is approximately ± 15%.

**Figure 7. a through h Nominal Current per Output versus Rx**

### Table 1. Triple–Mode Segment Decoder Function Table

| Bank Nibble Value | | | 7–Segment Display Characters | | Lamp Conditions | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| | | | | | No Decode ① (Invoked via Bits C1 to C7) | | | |
| Hexadecimal | Binary MSB | LSB | Hex Decode (Invoked via Bits C1 to C5) | Special Decode (Invoked via Bits C1 to C7) | d | c | b | a |
| $0 | L L L | L | 0 | | | | | |
| $1 | L L L | H | 1 | c | | | | on |
| $2 | L L H | L | 2 | H | | | on | |
| $3 | L L H | H | 3 | h | | | on | on |
| $4 | L H L | L | 4 | J | | on | | |
| $5 | L H L | H | 5 ② | L | | on | | on |
| $6 | L H H | L | 6 | n | | on | on | |
| $7 | L H H | H | 7 | o | | on | on | on |
| $8 | H L L | L | 8 ③ | P | on | | | |
| $9 | H L L | H | 9 ④ | r | on | | | on |
| $A | H L H | L | A | U | on | | on | |
| $B | H L H | H | b | u | on | | on | on |
| $C | H H L | L | C | y | on | on | | |
| $D | H H L | H | d | - | on | on | | on |
| $E | H H H | L | E | = | on | on | on | |
| $F | H H H | H | F | o | on | on | on | on |

NOTES:
1. In the *No Decode* mode, outputs e, f, and g are unused and are all forced inactive (low). Output h decoding is unaffected, i.e., unchanged from the other modes. The *No Decode* mode is used for three purposes:
   a. Individually controlling lamps.
   b. Controlling a half digit with sign.
   c. Controlling annunciators - examples: AM, PM, UHF, kV, mm Hg.
2. Can be used as capital S.
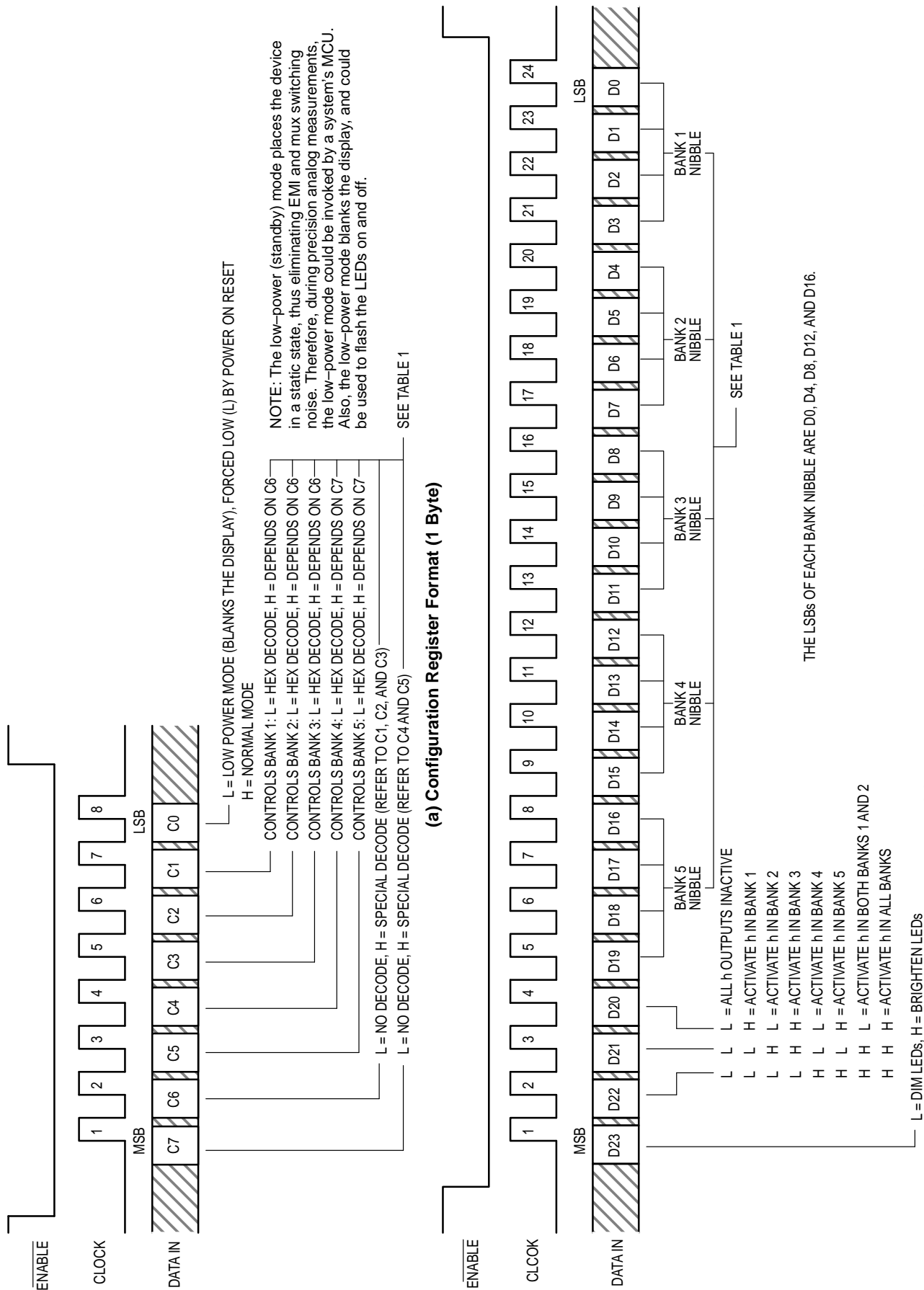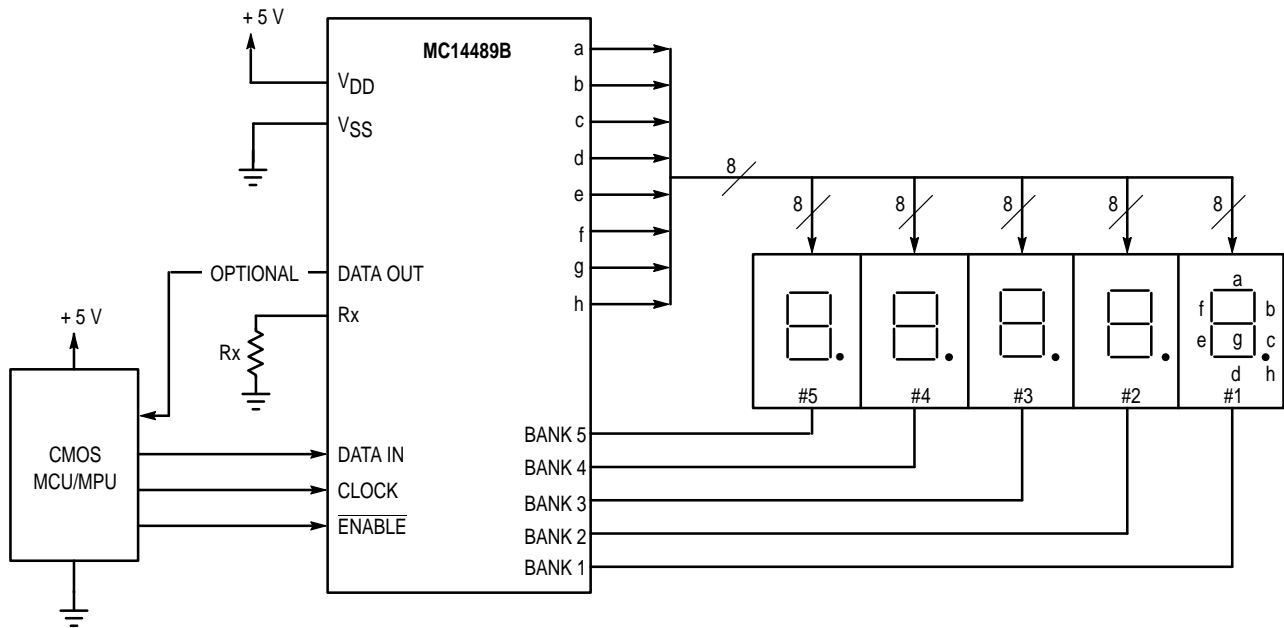3. Can be used as capital B.
4. Can be used as small g.

# Figure 8. Timing Diagrams for Non–Cascaded Devices

## (a) Configuration Register Format (1 Byte)

Signals: ENABLE, CLOCK, DATA IN

Clock pulses 1–8

DATA IN bits (MSB to LSB): C7, C6, C5, C4, C3, C2, C1, C0

- C0: L = LOW POWER MODE (BLANKS THE DISPLAY), FORCED LOW (L) BY POWER ON RESET
  H = NORMAL MODE
- C1: CONTROLS BANK 1: L = HEX DECODE, H = DEPENDS ON C6
- C2: CONTROLS BANK 2: L = HEX DECODE, H = DEPENDS ON C6
- C3: CONTROLS BANK 3: L = HEX DECODE, H = DEPENDS ON C6
- C4: CONTROLS BANK 4: L = HEX DECODE, H = DEPENDS ON C7
- C5: CONTROLS BANK 5: L = HEX DECODE, H = DEPENDS ON C7
- C6: L = NO DECODE, H = SPECIAL DECODE (REFER TO C1, C2, AND C3)
- C7: L = NO DECODE, H = SPECIAL DECODE (REFER TO C4 AND C5)

SEE TABLE 1

NOTE: The low–power (standby) mode places the device in a static state, thus eliminating EMI and mux switching noise. Therefore, during precision analog measurements, the low–power mode could be invoked by a system's MCU. Also, the low–power mode blanks the display, and could be used to flash the LEDs on and off.

## (b) Display Register Format (3 Bytes)

Signals: ENABLE, CLCOK, DATA IN

Clock pulses 1–24

DATA IN bits (MSB to LSB): D23, D22, D21, D20, D19, D18, D17, D16, D15, D14, D13, D12, D11, D10, D9, D8, D7, D6, D5, D4, D3, D2, D1, D0

- BANK 5 NIBBLE: D23, D22, D21, D20
- BANK 4 NIBBLE: D19, D18, D17, D16
- BANK 3 NIBBLE: D15, D14, D13, D12
- BANK 2 NIBBLE: D11, D10, D9, D8
- BANK 1 NIBBLE: D7, D6, D5, D4, D3, D2, D1, D0

SEE TABLE 1

THE LSBs OF EACH BANK NIBBLE ARE D0, D4, D8, D12, AND D16.

D23 D22:
- L L = ALL h OUTPUTS INACTIVE
- L H = ACTIVATE h IN BANK 1
- H L = ACTIVATE h IN BANK 2
- H H = ACTIVATE h IN BANK 3
- L L = ACTIVATE h IN BANK 4
- L H = ACTIVATE h IN BANK 5
- H L = ACTIVATE h IN BOTH BANKS 1 AND 2
- H H = ACTIVATE h IN ALL BANKS

L = DIM LEDs, H = BRIGHTEN LEDs

NOTE: L = Low Voltage Level (Logic 0), H = High Voltage Level (Logic 1)

**Figure 9. Non–Cascaded Application Example: 5 Character Common Cathode
LED Display with Two Intensities as Controlled via Serial Port**
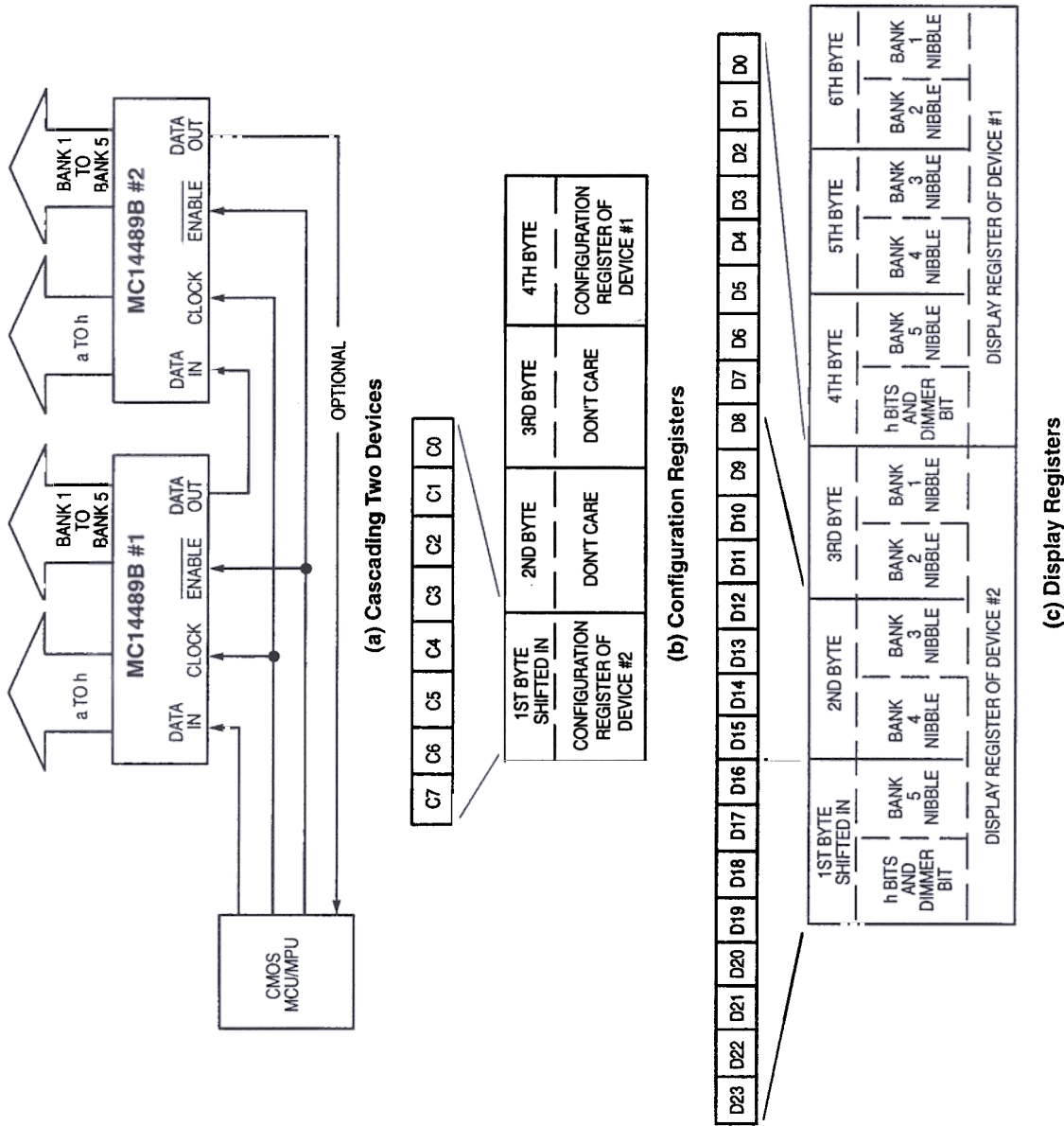
**Figure 10. Bit Stream Formats for Two Devices Cascaded**

(a) Cascading Two Devices

(b) Configuration Registers

(c) Display Registers

NOTE: ENABLE (which initially must be inactive high) is kept active–low during the entire 4–byte configuration transfer or 6–byte display transfer. When ENABLE is brought back high, either a 4– or 6–byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.

**(a) Cascading Three Devices**

CMOS MCU/MPU

MC14489B #1 — DATA IN, CLOCK, ENABLE, DATA OUT — a TO h — BANK 1 TO BANK 5
MC14489B #2 — DATA IN, CLOCK, ENABLE, DATA OUT — a TO h — BANK 1 TO BANK 5
MC14489B #3 — DATA IN, CLOCK, ENABLE, DATA OUT — a TO h — BANK 1 TO BANK 5

OPTIONAL

**(b) Configuration Registers**

| 1ST BYTE SHIFTED IN | 2ND BYTE | 3RD BYTE | 4TH BYTE | 5TH BYTE | 6TH BYTE | 7TH BYTE | 8TH (LAST) BYTE |
|---|---|---|---|---|---|---|---|
| DON'T CARE | CONFIGURATION REGISTER OF DEVICE #3 | DON'T CARE | DON'T CARE | CONFIGURATION REGISTER OF DEVICE #2 | DON'T CARE | DON'T CARE | CONFIGURATION REGISTER OF DEVICE #1 |

| C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|---|---|---|---|---|---|---|---|

**(c) Display Registers**

| D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

1ST BYTE SHIFTED IN — DON'T CARE (OPTIONAL, SEE NOTE)

2ND BYTE — h BITS AND DIMMER BIT | BANK 5 NIBBLE
3RD BYTE — BANK 4 NIBBLE | BANK 3 NIBBLE
DISPLAY REGISTER OF DEVICE #3

4TH BYTE — BANK 2 NIBBLE | BANK 1 NIBBLE
5TH BYTE — h BITS AND DIMMER BIT | BANK 5 NIBBLE
6TH BYTE — BANK 4 NIBBLE | BANK 3 NIBBLE
DISPLAY REGISTER OF DEVICE #2

7TH BYTE — BANK 2 NIBBLE | BANK 1 NIBBLE
8TH BYTE — h BITS AND DIMMER BIT | BANK 5 NIBBLE
9TH BYTE — BANK 4 NIBBLE | BANK 3 NIBBLE
10TH (LAST) BYTE — BANK 2 NIBBLE | BANK 1 NIBBLE
DISPLAY REGISTER OF DEVICE #1

**Figure 11. Bit Stream Formats for Three Devices Cascaded**

NOTE: When the leading "don't care" bytes are included, $\overline{\text{ENABLE}}$ (which initially must be inactive high) is kept active–low during the entire 8–byte configuration transfer or 10–byte display transfer. When ENABLE is brought back high, either an 8– or 10–byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the one "don't care" byte can be eliminated as follows: (1) take $\overline{\text{ENABLE}}$ active low, (2) transfer 6 bytes, (3) pulse $\overline{\text{ENABLE}}$ inactive high, see $t_w(H)$ spec, (4) transfer last 3 bytes, and (5) take $\overline{\text{ENABLE}}$ inactive high.
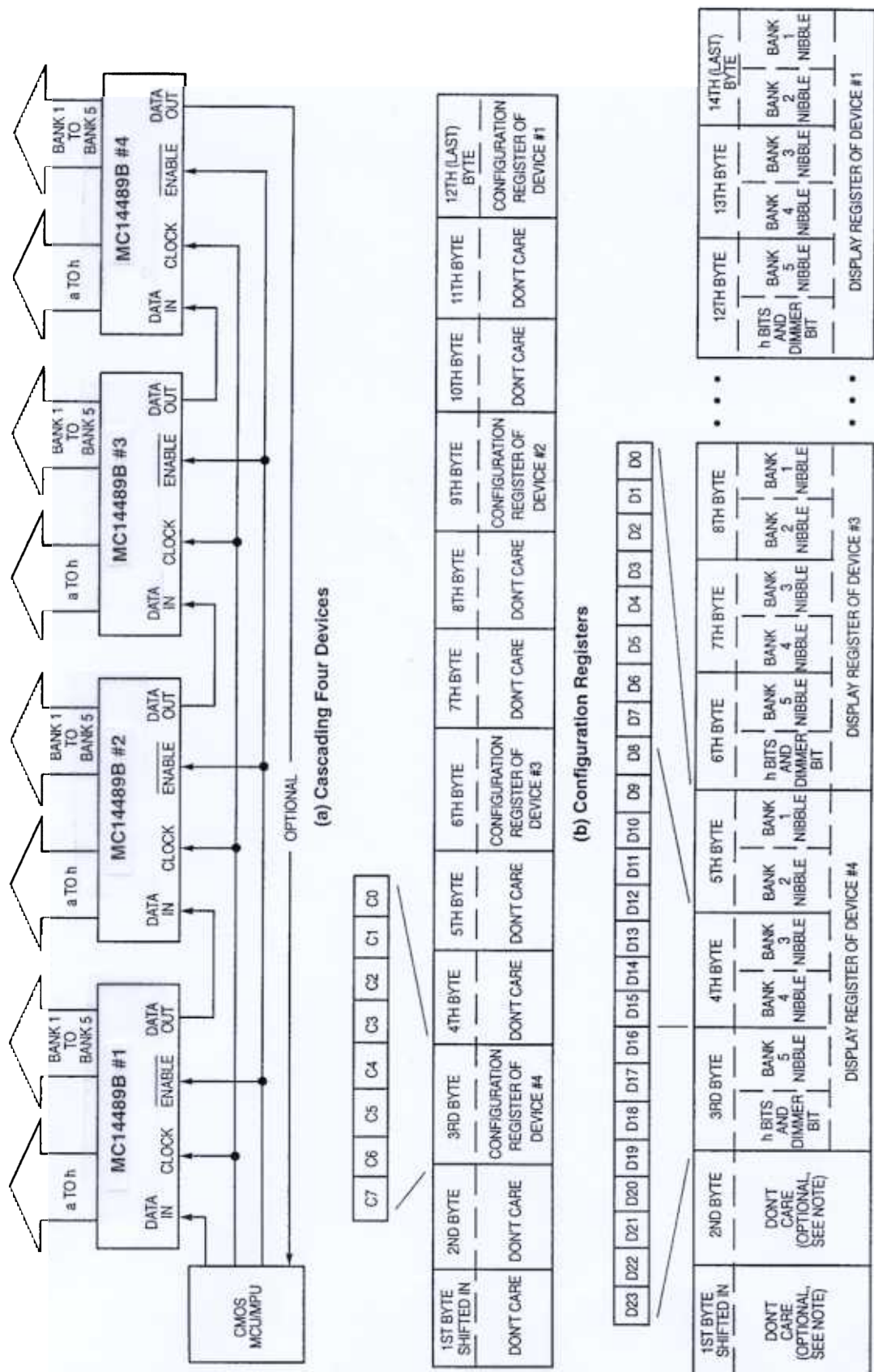
Figure 12. Bit Stream Formats for Four Devices Cascaded

NOTE: When the leading "don't care" bytes are included, ENABLE (which initially must be inactive high) is kept active-low during the entire 12-byte configuration transfer or 14-byte display transfer. When ENABLE is brought back high, either a 12- or 14-byte transfer occurs in the cascaded devices. Alternatively, when updating the display registers, the two "don't care" bytes can be eliminated as follows: (1) take ENABLE active low, (2) transfer 6 bytes, (3) pulse ENABLE inactive high, see $t_w(H)$ spec, (4) transfer last 6 bytes, and (5) take ENABLE inactive high.
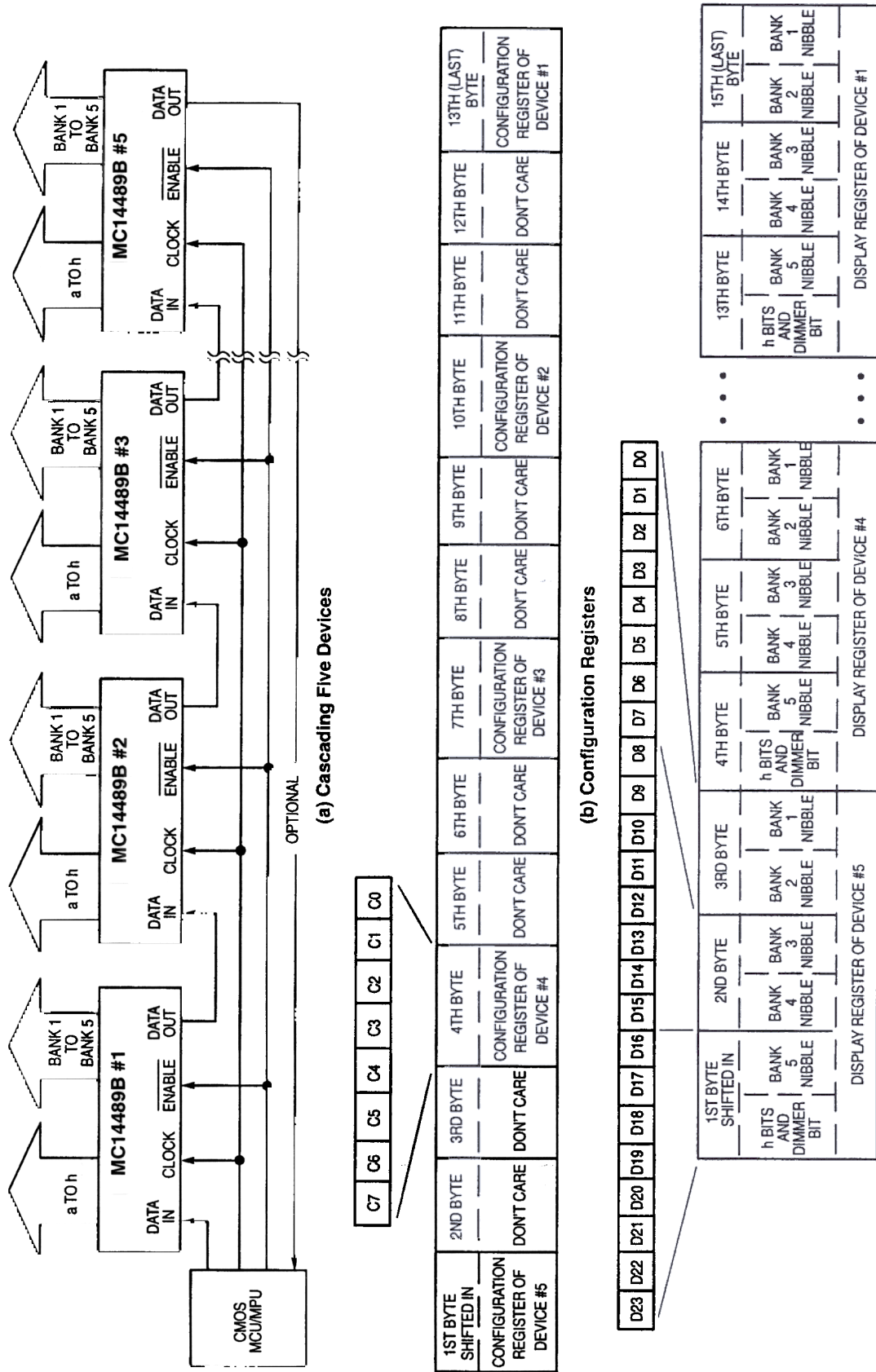
**Figure 13. Bit Stream Formats for Five Devices Cascaded**

**(a) Cascading Five Devices**

**(b) Configuration Registers**

**(c) Display Registers**

NOTE: ENABLE (which initially must be inactive high) is kept active—low during the entire 13—byte configuration transfer or 15—byte display transfer. When ENABLE is brought back high, either a 13— or 15—byte transfer occurs in the cascaded devices, depending on the number of bytes in the transfer.
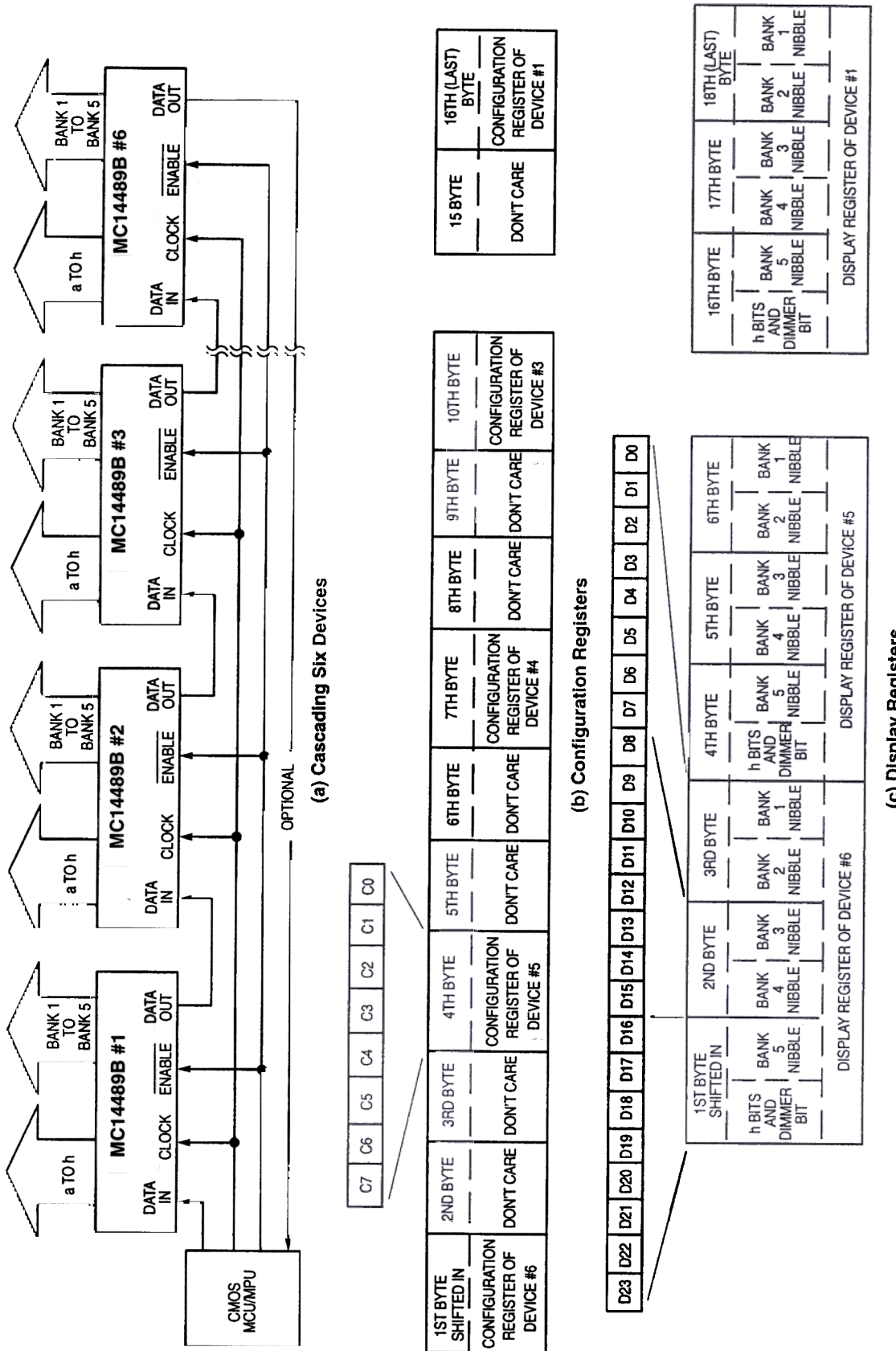
Figure 14. Bit Stream Formats for Six Devices Cascaded

**Table 2. Register Access for Two or More Cascaded Devices**

| Criteria* | Configuration Register Access | | Display Register Access | |
|---|---|---|---|---|
| | Total Number of Bytes | Number of Leading "Don't Care" Bytes | Total Number of Bytes | Number of Leading "Don't Care" Bytes |
| If 3N is a Multiple of 4 | 3N | 2 | 3N + 2 | 2 |
| If 3N − 1 is a Multiple of 4 | 3N − 1 | 1 | 3N + 1 | 1 |
| If 3N − 2 is a Multiple of 4 | 3N − 2 | 0 | 3N | 0 |
| If 3N − 3 is a Multiple of 4 | 3N − 2 | 0 | 3N | 0 |

* N = number of devices that are cascaded. For example, to drive 10 digits, 2 devices are cascaded; therefore, N = 2. To drive 35 digits, seven devices are cascaded; therefore N = 7.
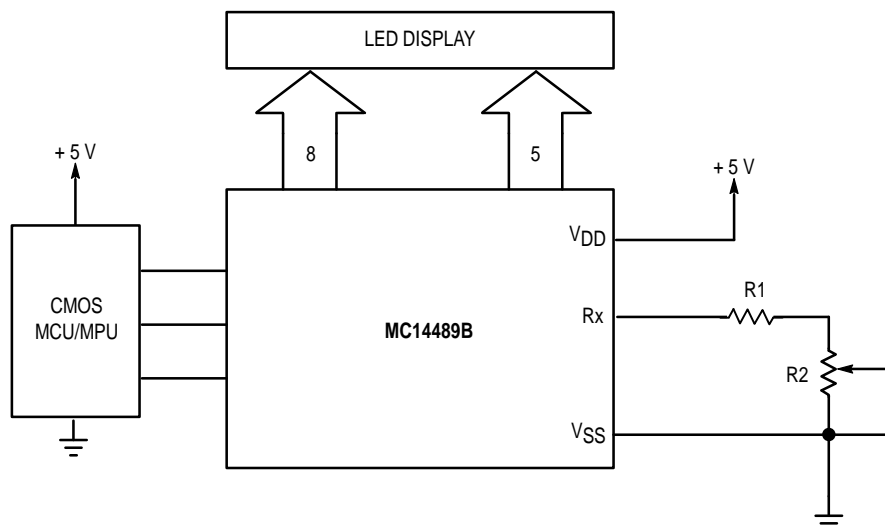


NOTE: R1 limits the maximum current to avoid damaging the display and/or the MC14489B due to overheating. See the Thermal Considerations section. An 1/8 watt resistor may be used for R1. R2 is a 1 kΩ or 5 kΩ potentiometer (≥ 1/8 watt). R2 may be a light–sensitive resistor.

**Figure 15. Common–Cathode LED Display with Dial–Adjusted Brightness**
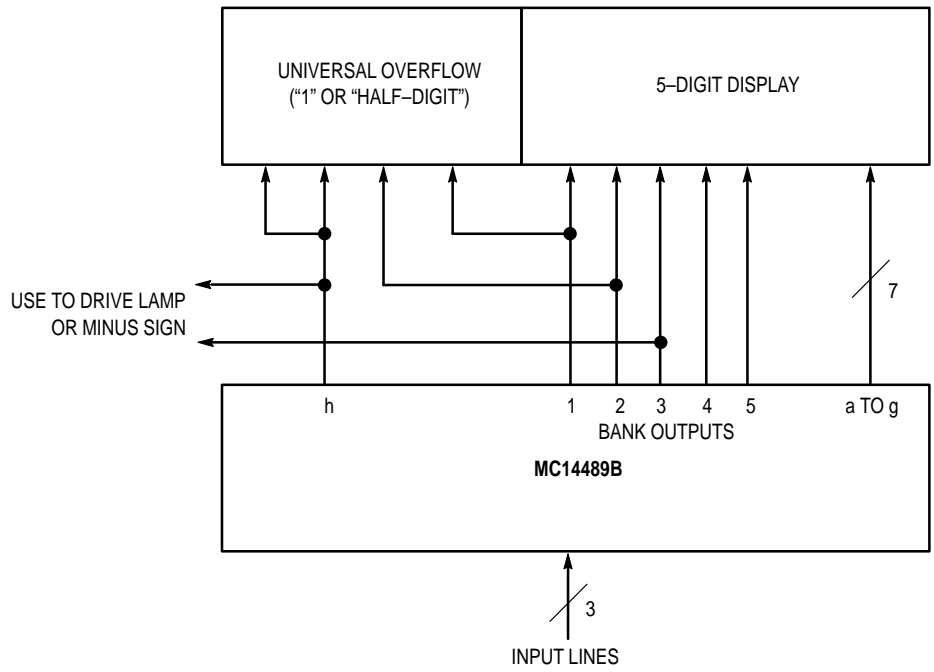
NOTE: A Universal Overflow pins out all anodes and cathodes.

**Figure 16. Driving 5 1/2 Digits**

THESE LAMPS
INDEPENDENTLY
CONTROLLED WITH
BITS D0 TO D19

THESE LAMPS DEPENDENTLY
CONTROLLED WITH
BITS D20, D21, AND D22*
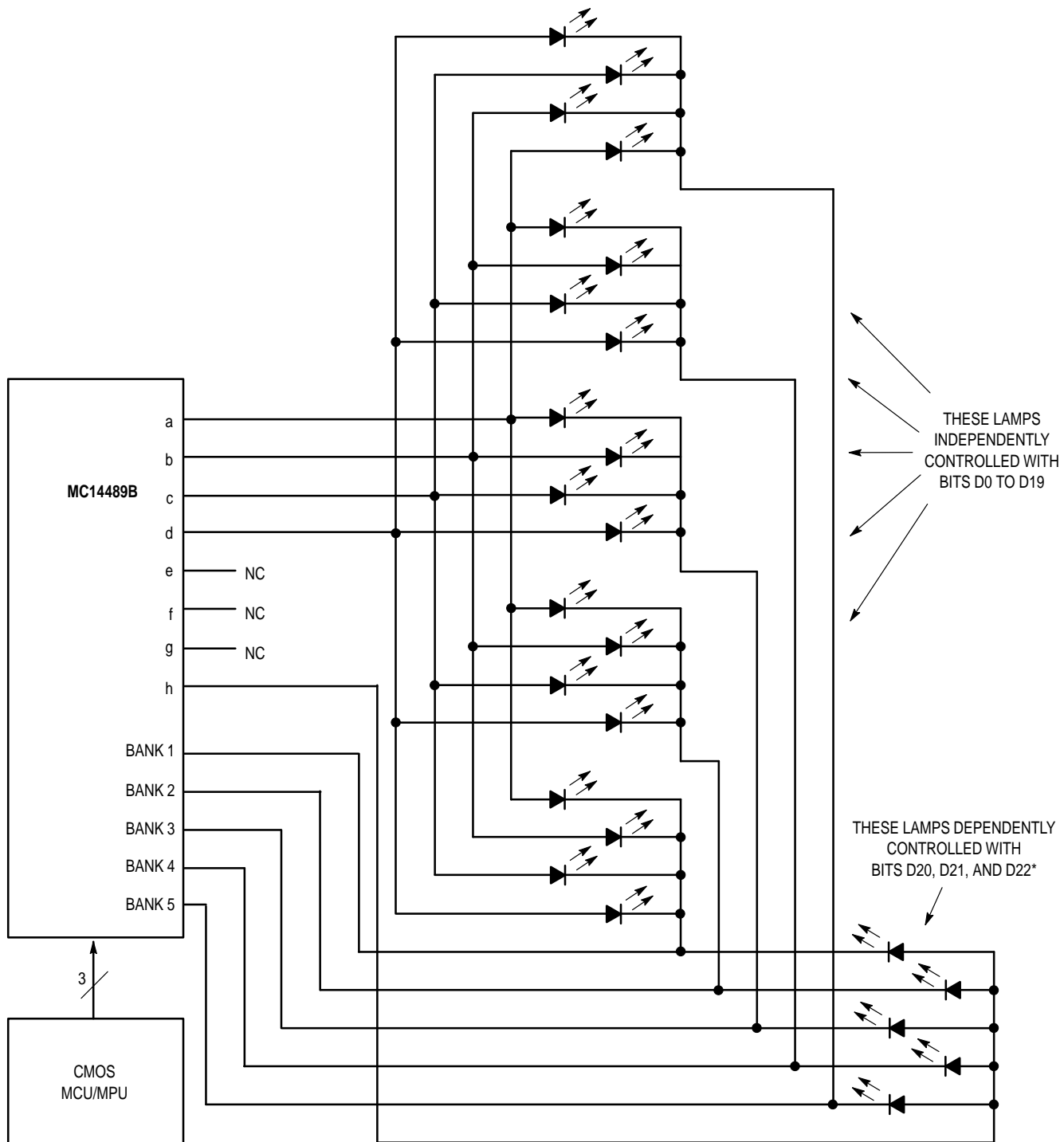
* If required, this group of lamps can be independently controlled. To accomplish independent control, only connect lamps to BANK 1 and
BANK 2 for output h (two lamps). Then, use bits D20, D21, and D22 for control of these two lamps.

**Figure 17. 25–Lamp Application**
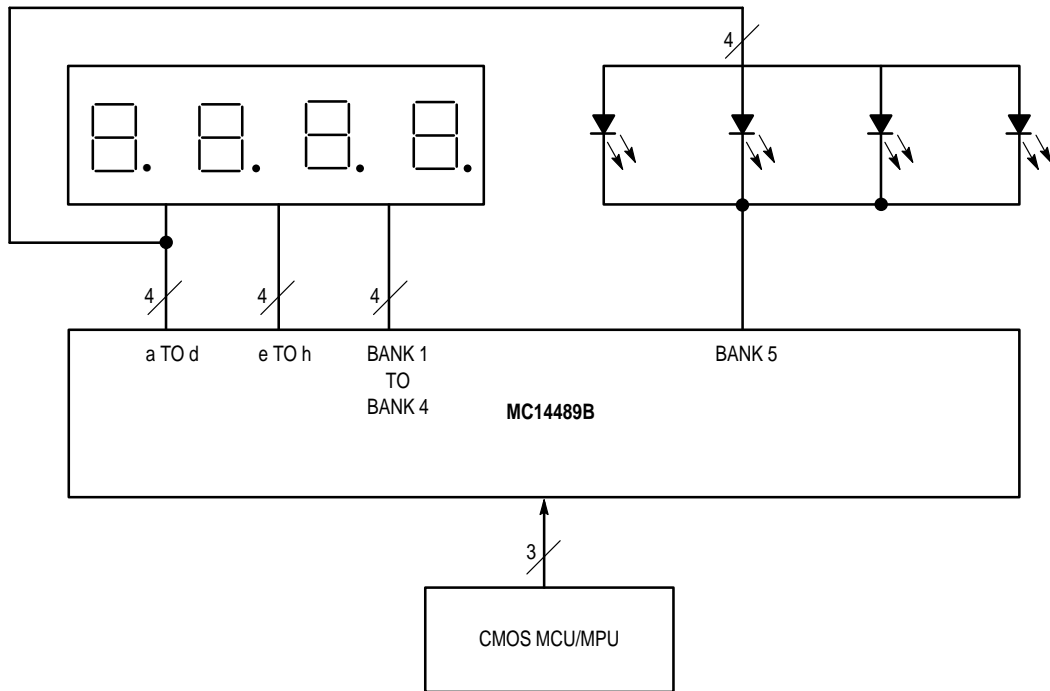
**Figure 18. 4–Digit Display Plus Decimals with Four Annunciators
or 4–1/2–Digit Display Plus Sign**
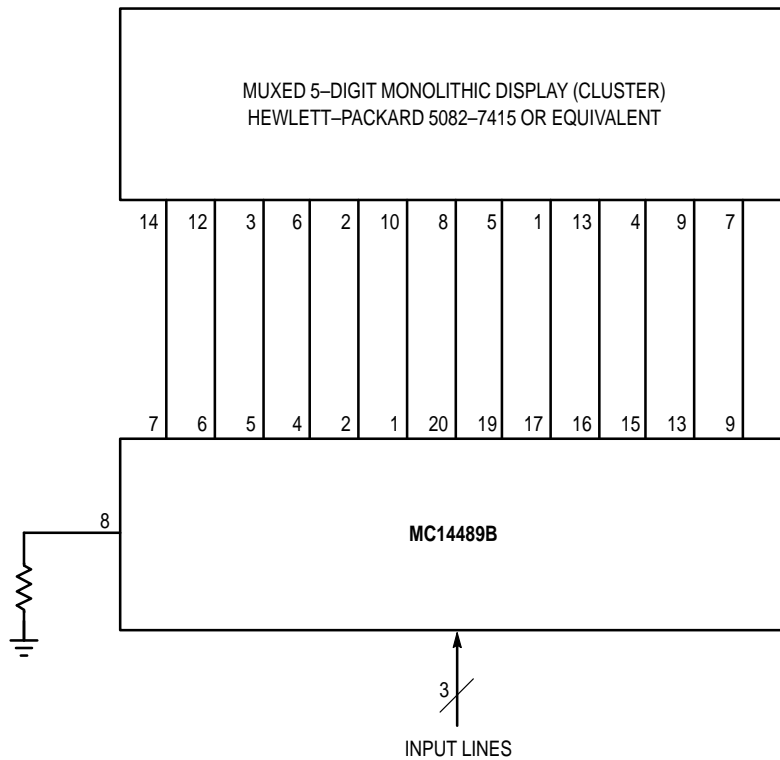


**Figure 19. Compact Display System with Three Components**

# THERMAL CONSIDERATIONS

The MC14489B is designed to operate with a *chip–junction* temperature ($T_J$) ranging from – 40 to 130°C, as indicated in the electrical characteristics tables. The *ambient* operating temperature range ($T_A$) is dependent on $R_{\theta JA}$, the internal chip current, how many anode drivers are used, the number of bank drivers used, the drive current, and how the package is cooled. The maximum ratings table gives the thermal resistance, junction–to–ambient, of the MC14489B mounted on a pc board using natural convection to be 90°C per watt for the plastic DIP. The SOG thermal resistance is 100°C per watt.

The following general equation (1) is used to determine the power dissipated by the MC14489B.

$$P_T = P_D + P_I \qquad (1)$$

where

$P_T$ = Total power dissipation of the MC14489B
$P_D$ = Power dissipated in the driver circuitry (mW)
$P_I$ = Power dissipated by the internal chip circuitry (mW)

The equations for the two terms of the general equation are:

$$P_D = (i_{OH})\,(N)(V_{DD} - V_{LED})(B/5) \qquad (2)$$

$$P_I = (1.5\ mA)(V_{DD}) + I_{Rx}(V_{DD} - I_{Rx}Rx) \qquad (3)$$

where

$i_{OH}$ = Peak anode driver current (mA)
$I_{Rx}$ = $i_{OH}/10$, with $i_{OH}$ = the peak anode driver current (mA) when the dimmer bit is high
$N$ = Number of anode drivers used
$B$ = Number of bank drivers used
$Rx$ = External resistor value (kΩ)
$V_{DD}$ = Maximum supply voltage, referenced to $V_{SS}$ (volts)
$V_{LED}$ = Minimum anticipated voltage drop across the LED
1.5 mA = Operating supply current of the MC14489B

The following two examples show how to calculate the maximum allowable ambient temperature.

**Worst–Case Analysis Example 1:**

5–digit display with decimals (5 banks and 8 anode drivers)
DIP without heat sink on PC board
$\quad i_{OH}$ = 20 mA max
$\quad V_{LED}$ = 1.8 V min
$\quad V_{DD}$ = 5.25 max

$P_D = (20)(8)(5.25 - 1.8)(5/5) = 552\ mW$      Ref. (2)

$P_I = (1.5)(5.25) + 2[5.25 - 2(2)] = 10\ mW$      Ref. (3)

Therefore, $P_T = 552 + 10 = 562\ mW$      Ref. (1)

and $\Delta T_{chip} = R_{\theta JA}P_T = (90°C/W)(0.562) = 51°C$

Finally, the maximum allowable
$\quad T_A = T_Jmax - \Delta T_{chip} = 130 - 51 = 79°C$

That is, if $T_A = 79°C$, the maximum junction temperature is 130°C. The chip's average temperature for this example is lower than 130°C because all segments are usually not illuminated simultaneously for an indefinite period.

**Worst–Case Analysis Example 2:**

16 lamps (4 banks and 4 anode drivers)
SOG without heat sink on PC board
$\quad i_{OH}$ = 30 mA max
$\quad V_{LED}$ = 1.8 V min
$\quad V_{DD}$ = 5.5 max

$P_D = (30)(4)(5.5 - 1.8)(4/5) = 355\ mW$      Ref. (2)

$P_I = (1.5)(5.5) + 3[5.5 - 3(1.0)] = 16\ mW$      Ref. (3)

Therefore, $P_T = 355 + 16 = 371\ mW$      Ref. (1)

and $\Delta T_{chip} = R_{\theta JA}P_T = (100°C/W)(0.371) = 37°C$

Finally, the maximum allowable
$\quad T_A = T_Jmax - \Delta T_{chip} = 130 - 37 = 93°C$

To extend the allowable ambient temperature range or to reduce $T_J$, which extends chip life, a heat sink such as shown in Figure 20 can be used in high–current applications. Alternatively, heat–spreader techniques can be used on the PC board, such as running a wide trace under the MC14489B and using thermal paste. Wide, radial traces from the MC14489B leads also act as heat spreaders.
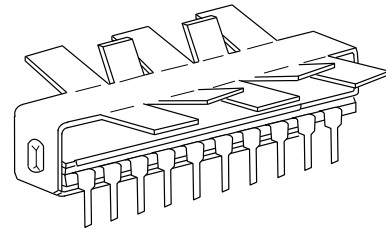


AAVID #5804 or equivalent
(Tel. 603/524–4443, FAX 603/528–1478)
Motorola cannot recommend one supplier over another and in no way suggests that this is the only heat sink supplier.

**Figure 20. Heat Sink**

**Table 3. LED Lamp and Common–Cathode Display Manufacturers**

| Supplier |
| --- |
| QT Optoelectronics |
| Hewlett–Packard (HP), Components Group |
| Industrial Electronic Engineers (IEE), Component Products Div. |
| Purdy Electronics Corp., AND Product Line |

NOTE: Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of LED suppliers.

**P SUFFIX**
**PLASTIC DIP**
**CASE 738–03**
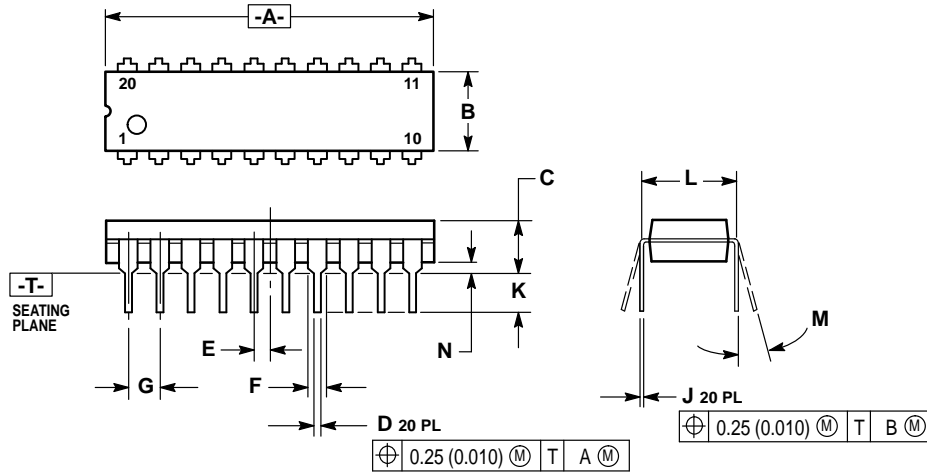


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|-----|-------------|-----|
|     | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**DW SUFFIX**
**SOG PACKAGE**
**CASE 751D–04**
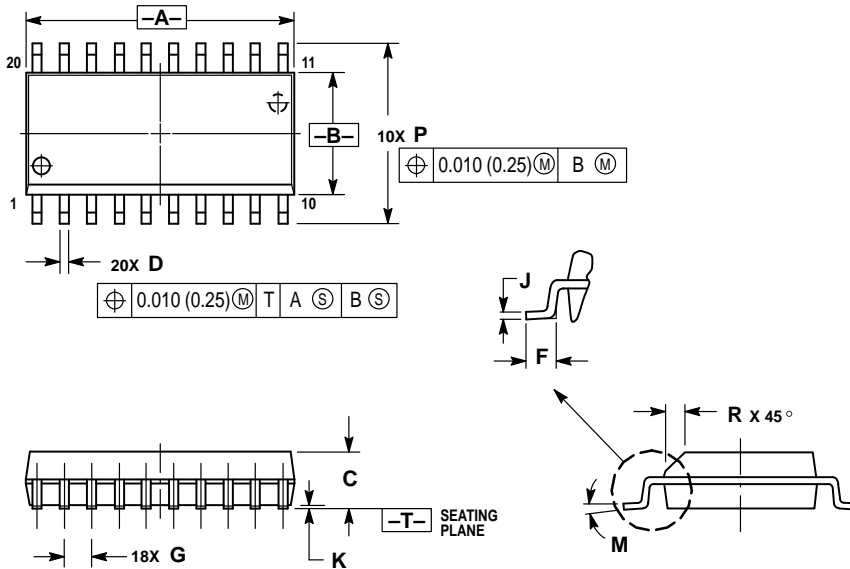


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-----|--------|-----|
|     | MIN | MAX | MIN | MAX |
| A | 12.65 | 12.95 | 0.499 | 0.510 |
| B | 7.40 | 7.60 | 0.292 | 0.299 |
| C | 2.35 | 2.65 | 0.093 | 0.104 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.50 | 0.90 | 0.020 | 0.035 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.25 | 0.32 | 0.010 | 0.012 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 10.05 | 10.55 | 0.395 | 0.415 |
| R | 0.25 | 0.75 | 0.010 | 0.029 |

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MC14489B