

# Low-Voltage CMOS 16-Bit D-Type Flip-Flop With 5V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16374 is a high performance, non-inverting 16-bit D-type flip-flop operating from a 2.7 to 3.6V supply. The device is byte controlled. Each byte has separate Output Enable and Clock Pulse inputs. These control pins can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5V allows MC74LCX16374 inputs to be safely driven from 5V devices.

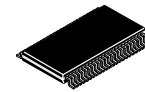
The MC74LCX16374 consists of 16 edge-triggered flip-flops with individual D-type inputs and 5V-tolerant 3-state true outputs. The buffered clocks (CPn) and buffered Output Enables (OEn) are common to all flip-flops within the respective byte. The flip-flops will store the state of individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the OE LOW, the contents of the flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. The OE input level does not affect the operation of the flip-flops.

- Designed for 2.7 to 3.6V  $V_{CC}$  Operation
- 6.2ns Maximum  $t_{pd}$
- 5V Tolerant — Interface Capability With 5V TTL Logic
- Supports Live Insertion and Withdrawal
- I<sub>OFF</sub> Specification Guarantees High Impedance When  $V_{CC} = 0V$
- LVTTTL Compatible
- LVCMOS Compatible
- 24mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V; Machine Model >200V

**MC74LCX16374**

**LCX**

**LOW-VOLTAGE  
CMOS 16-BIT  
D-TYPE FLIP-FLOP**



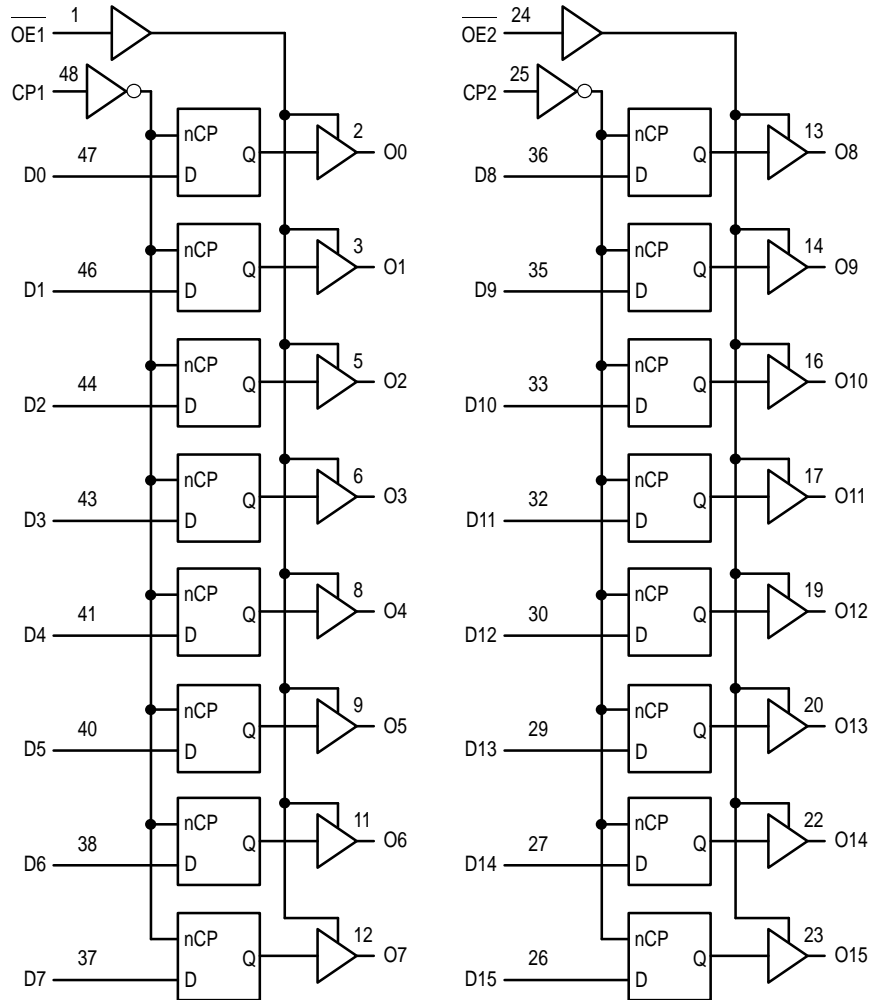
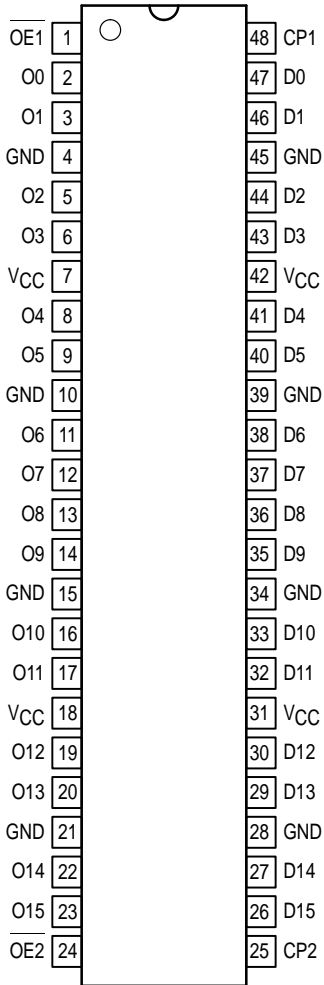
**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 1201-01

**PIN NAMES**

Pins	Function
OEn	Output Enable Inputs
CPn	Clock Pulse Inputs
D0-D15	Inputs
O0-O15	Outputs



LOGIC DIAGRAM



Inputs			Outputs	Inputs			Outputs
CP1	OE1	D0:7	O0:7	CP2	OE2	D8:15	O8:15
↑	L	H	H	↑	L	H	H
↑	L	L	L	↑	L	L	L
L	L	X	O0	L	L	X	O0
X	H	X	Z	X	H	X	Z

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; ↑ = Low-to-High Transition; X = High or Low Voltage Level and Transitions Are Acceptable, for I<sub>CC</sub> reasons, DO NOT FLOAT Inputs

**ABSOLUTE MAXIMUM RATINGS\***

Symbol	Parameter	Value	Condition	Unit
V <sub>CC</sub>	DC Supply Voltage	-0.5 to +7.0		V
V <sub>I</sub>	DC Input Voltage	-0.5 ≤ V <sub>I</sub> ≤ +7.0		V
V <sub>O</sub>	DC Output Voltage	-0.5 ≤ V <sub>O</sub> ≤ +7.0	Output in 3-State	V
		-0.5 ≤ V <sub>O</sub> ≤ V <sub>CC</sub> + 0.5	Note 1.	V
I <sub>IK</sub>	DC Input Diode Current	-50	V <sub>I</sub> < GND	mA
I <sub>OK</sub>	DC Output Diode Current	-50	V <sub>O</sub> < GND	mA
		+50	V <sub>O</sub> > V <sub>CC</sub>	mA
I <sub>O</sub>	DC Output Source/Sink Current	±50		mA
I <sub>CC</sub>	DC Supply Current Per Supply Pin	±100		mA
I <sub>GND</sub>	DC Ground Current Per Ground Pin	±100		mA
T <sub>STG</sub>	Storage Temperature Range	-65 to +150		°C

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

1. Output in HIGH or LOW State. I<sub>O</sub> absolute maximum rating must be observed.

**RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min	Typ	Max	Unit	
V <sub>CC</sub>	Supply Voltage	Operating	2.0	3.3	3.6	V
		Data Retention Only	1.5	3.3	3.6	
V <sub>I</sub>	Input Voltage	0		5.5	V	
V <sub>O</sub>	Output Voltage (HIGH or LOW State) (3-State)	0		V <sub>CC</sub>	V	
		0		5.5		
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			-24	mA	
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 3.0V – 3.6V			24	mA	
I <sub>OH</sub>	HIGH Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			-12	mA	
I <sub>OL</sub>	LOW Level Output Current, V <sub>CC</sub> = 2.7V – 3.0V			12	mA	
T <sub>A</sub>	Operating Free-Air Temperature	-40		+85	°C	
Δt/ΔV	Input Transition Rise or Fall Rate, V <sub>IN</sub> from 0.8V to 2.0V, V <sub>CC</sub> = 3.0V	0		10	ns/V	

**DC ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	Condition	T <sub>A</sub> = -40°C to +85°C		Unit
			Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V	2.0		V
V <sub>IL</sub>	LOW Level Input Voltage (Note 2.)	2.7V ≤ V <sub>CC</sub> ≤ 3.6V		0.8	V
V <sub>OH</sub>	HIGH Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OH</sub> = -100μA	V <sub>CC</sub> - 0.2		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -12mA	2.2		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -18mA	2.4		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -24mA	2.2		
V <sub>OL</sub>	LOW Level Output Voltage	2.7V ≤ V <sub>CC</sub> ≤ 3.6V; I <sub>OL</sub> = 100μA		0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 12mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 24mA		0.55	

2. These values of V<sub>I</sub> are used to test DC electrical characteristics only.

**DC ELECTRICAL CHARACTERISTICS** (continued)

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
$I_I$	Input Leakage Current	$2.7\text{V} \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_I \leq 5.5\text{V}$		$\pm 5.0$	$\mu\text{A}$
$I_{OZ}$	3-State Output Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; 0\text{V} \leq V_O \leq 5.5\text{V}; V_I = V_{IH} \text{ or } V_{IL}$		$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_{CC} = 0\text{V}; V_I \text{ or } V_O = 5.5\text{V}$		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_I = \text{GND or } V_{CC}$		20	$\mu\text{A}$
		$2.7 \leq V_{CC} \leq 3.6\text{V}; 3.6 \leq V_I \text{ or } V_O \leq 5.5\text{V}$		$\pm 20$	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$2.7 \leq V_{CC} \leq 3.6\text{V}; V_{IH} = V_{CC} - 0.6\text{V}$		500	$\mu\text{A}$

**AC CHARACTERISTICS** ( $t_R = t_F = 2.5\text{ns}; C_L = 50\text{pF}; R_L = 500\Omega$ )

Symbol	Parameter	Waveform	Limits				Unit
			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$				
			$V_{CC} = 3.0\text{V to } 3.6\text{V}$		$V_{CC} = 2.7\text{V}$		
			Min	Max	Min	Max	
$f_{\text{max}}$	Clock Pulse Frequency	1	170				MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $O_n$	1	1.5 1.5	6.2 6.2	1.5 1.5	6.5 6.5	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time to HIGH and LOW Levels	2	1.5 1.5	6.1 6.1	1.5 1.5	6.3 6.3	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time from HIGH and LOW Levels	2	1.5 1.5	6.0 6.0	1.5 1.5	6.2 6.2	ns
$t_s$	Setup Time, HIGH or LOW $D_n$ to CP	1	2.5		2.5		ns
$t_h$	Hold Time, HIGH or LOW $D_n$ to CP	1	1.5		1.5		ns
$t_w$	CP Pulse Width, HIGH or LOW	3	3.0		3.0		ns
$t_{\text{OSHL}}$ $t_{\text{OSLH}}$	Output-to-Output Skew (Note 3.)			1.0 1.0			ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{\text{OSHL}}$ ) or LOW-to-HIGH ( $t_{\text{OSLH}}$ ); parameter guaranteed by design.

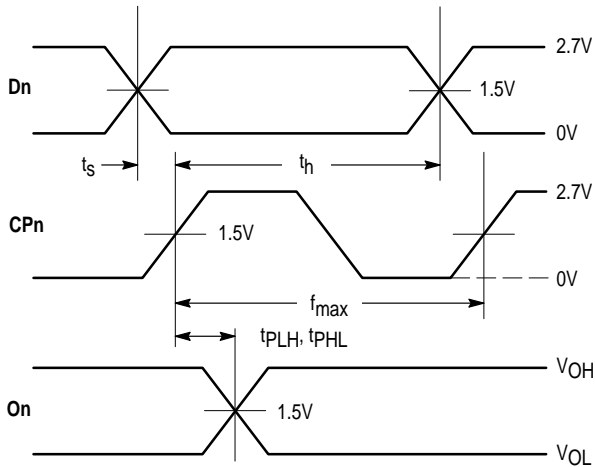
**DYNAMIC SWITCHING CHARACTERISTICS**

Symbol	Characteristic	Condition	$T_A = +25^\circ\text{C}$			Unit
			Min	Typ	Max	
$V_{\text{OLP}}$	Dynamic LOW Peak Voltage (Note 4.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V
$V_{\text{OLV}}$	Dynamic LOW Valley Voltage (Note 4.)	$V_{CC} = 3.3\text{V}, C_L = 50\text{pF}, V_{IH} = 3.3\text{V}, V_{IL} = 0\text{V}$		0.8		V

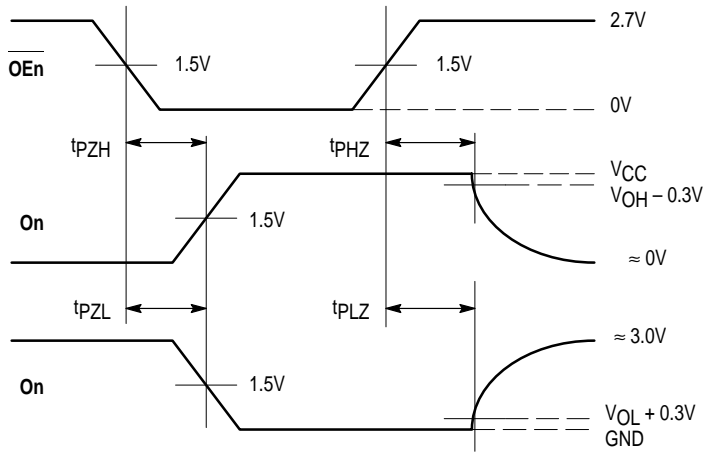
4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

**CAPACITIVE CHARACTERISTICS**

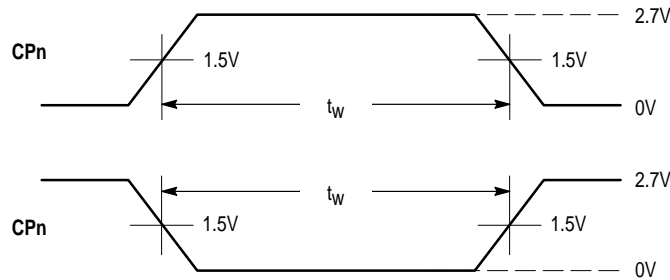
Symbol	Parameter	Condition	Typical	Unit
$C_{\text{IN}}$	Input Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	7	pF
$C_{\text{OUT}}$	Output Capacitance	$V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	8	pF
$C_{\text{PD}}$	Power Dissipation Capacitance	10MHz, $V_{CC} = 3.3\text{V}, V_I = 0\text{V or } V_{CC}$	20	pF



**WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

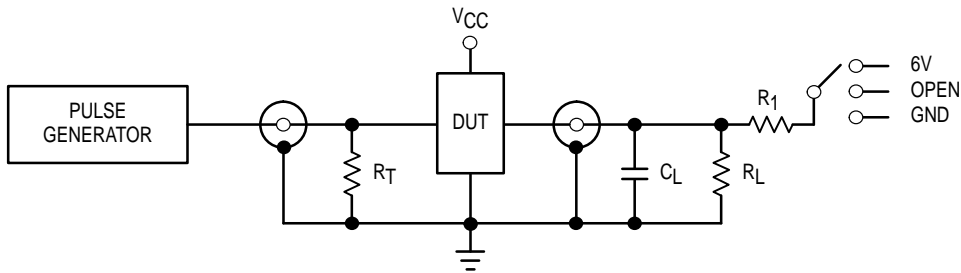


**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 3 – PULSE WIDTH**  
 $t_R = t_F = 2.5\text{ns}$  (or fast as required) from 10% to 90%;  
 Output requirements:  $V_{OL} \leq 0.8\text{V}$ ,  $V_{OH} \geq 2.0\text{V}$

**Figure 1. AC Waveforms**



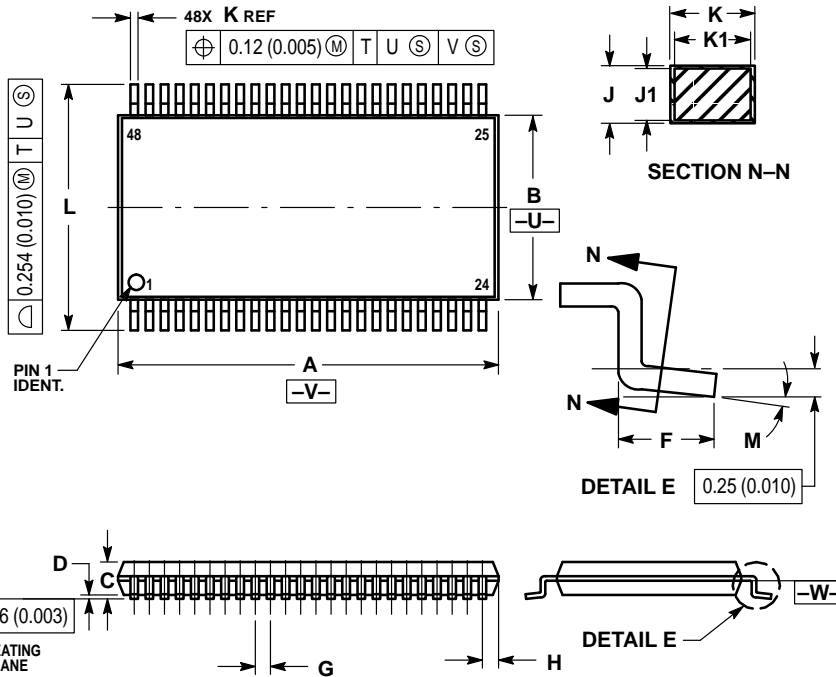
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	6V
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6V
$t_{PZH}$ , $t_{PHZ}$	GND

$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 2. Test Circuit**

OUTLINE DIMENSIONS

DT SUFFIX  
 PLASTIC TSSOP PACKAGE  
 CASE 1201-01  
 ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

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