

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74LCX16373AFT

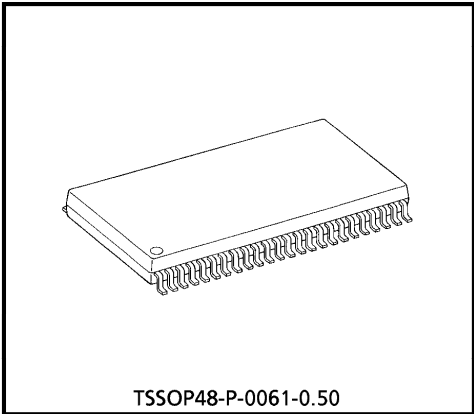
LOW-VOLTAGE 16-BIT D-TYPE LATCH
 WITH 5V TOLERANT INPUTS AND OUTPUTS

The TC74LCX16373AFT is a high performance CMOS 16bit D-TYPE LATCH. Designed for use in 3.3 Volt systems, it achieves high speed operation while maintaining the CMOS low power dissipation.

The device is designed for low-voltage (3.3V) V_{CC} applications, but it could be used to interface to 5V supply environment for both inputs and outputs.

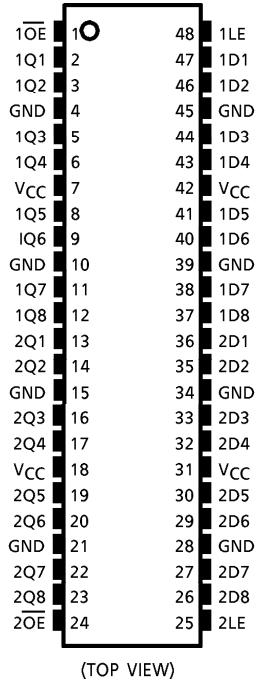
This 16-bit D-type latch is controlled by a latch enable input (LE) and a output enable input ($\overline{OE}$) which are common to each byte. It can be used as two 8-bit latches or one 16-bit latch. When the $\overline{OE}$ input is high, the outputs are in a high impedance state.

All inputs are equipped with protection circuits against static discharge.



Weight : 0.25 g (Typ.)

PIN CONNECTION



961001EBA2

TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

TRUTH TABLE

INPUT			OUTPUT
$1\overline{OE}$	1LE	1D1-1D8	1Q1-1Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

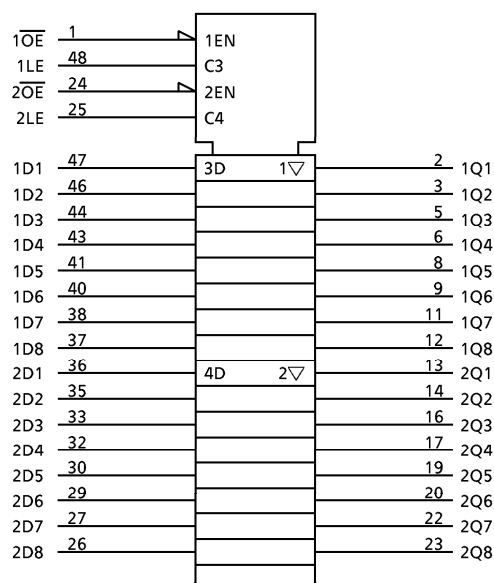
INPUT			OUTPUT
$2\overline{OE}$	2LE	2D1-2D8	2Q1-2Q8
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

X : Don't Care

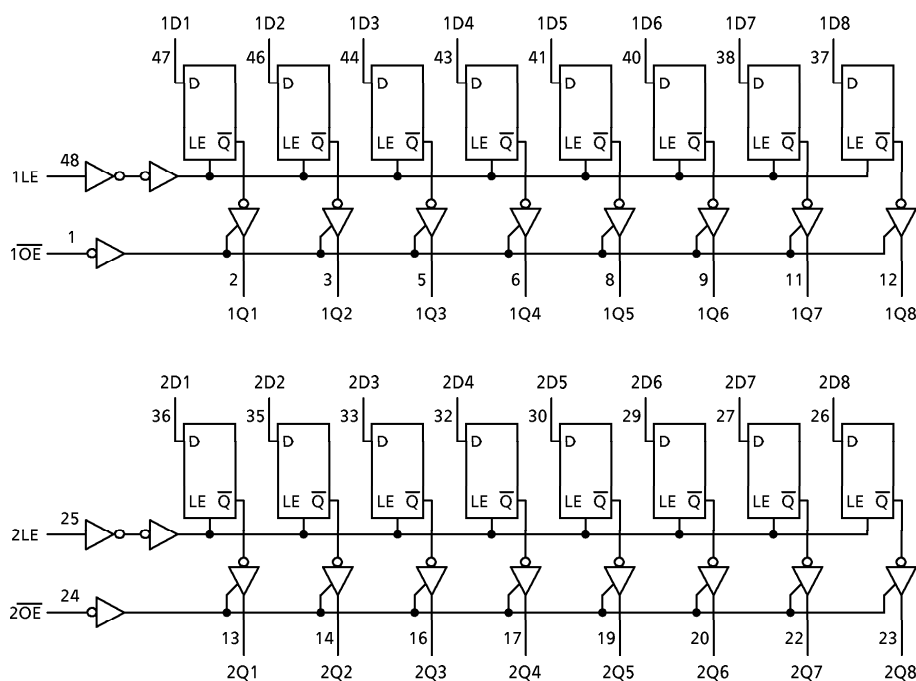
Z : High impedance

Qn : No change

IEC LOGIC SYMBOL



SYSTEM DIAGRAM



961001EBA2'

- The products described in this document are subject to foreign exchange and foreign trade control laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	$-0.5 \sim 7.0$	V
Input Voltage	V_{IN}	$-0.5 \sim 7.0$	V
Output Voltage	V_{OUT}	$-0.5 \sim 7.0$ (Note 1) $-0.5 \sim V_{CC} + 0.5$ (Note 2)	V
Input Diode Current	I_{IK}	-50	mA
Output Diode Current	I_{OK}	± 50 (Note 3)	mA
DC Output Current	I_{OUT}	± 50	mA
Power Dissipation	P_D	400	mW
DC V_{CC} / Ground Current Per Supply Pin	I_{CC} / I_{GND}	± 100	mA
Storage Temperature	T_{stg}	$-65 \sim 150$	$^{\circ}\text{C}$

(Note 1) Output in Off-State

(Note 2) High or Low State. I_{OUT} absolute maximum rating must be observed.(Note 3) $V_{OUT} < \text{GND}$, $V_{OUT} > V_{CC}$

RECOMMENDED OPERATING RANGE

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	$2.0 \sim 3.6$ $1.5 \sim 3.6$ (Note 4)	V
Input Voltage	V_{IN}	$0 \sim 5.5$	V
Output Voltage	V_{OUT}	$0 \sim 5.5$ (Note 5) $0 \sim V_{CC}$ (Note 6)	V
Output Current	I_{OH} / I_{OL}	± 24 (Note 7) ± 12 (Note 8)	mA
Operating Temperature	T_{opr}	$-40 \sim 85$	$^{\circ}\text{C}$
Input Rise And Fall Time	dt / dv	$0 \sim 10$ (Note 9)	ns / V

(Note 4) Data Retention Only

(Note 5) Output in Off-State

(Note 6) High or Low State

(Note 7) $V_{CC} = 3.0 \sim 3.6\text{V}$ (Note 8) $V_{CC} = 2.7 \sim 3.0\text{V}$ (Note 9) $V_{IN} = 0.8 \sim 2.0\text{V}$, $V_{CC} = 3.0\text{V}$

ELECTRICAL CHARACTERISTICS

DC characteristics (Ta = -40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V _{CC} (V)	MIN.	MAX.	UNIT
Input Voltage	"H" Level	V _{IH}			2.7~3.6	2.0	—	V
	"L" Level	V _{IL}			2.7~3.6	—	0.8	V
Output Voltage	"H" Level	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = - 100μA	2.7~3.6	V _{CC} - 0.2	—	V
				I _{OH} = - 12μA	2.7	2.2	—	
				I _{OH} = - 18mA	3.0	2.4	—	
				I _{OH} = - 24mA	3.0	2.2	—	
	"L" Level	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 100μA	2.7~3.6	—	0.2	V
				I _{OL} = 12mA	2.7	—	0.4	
				I _{OL} = 16mA	3.0	—	0.4	
				I _{OL} = 24mA	3.0	—	0.55	
Input Leakage Current		I _{IN}	V _{IN} = 0~5.5V	2.7~3.6	—	± 5.0	μA	
3-State Output Off-State Current		I _{OZ}	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0~5.5V	2.7~3.6	—	± 5.0	μA	
Power Off Leakage Current		I _{OFF}	V _{IN} / V _{OUT} = 5.5V	0	—	10.0	μA	
Quiescent Supply Current	I _{CC}		V _{IN} = V _{CC} or GND	2.7~3.6	—	20.0	μA	
			V _{IN} / V _{OUT} = 3.6~5.5V	2.7~3.6	—	± 20.0		
Increase In I _{CC} Per Input		ΔI _{CC}	V _{IH} = V _{CC} - 0.6V	2.7~3.6	—	500	μA	

AC characteristics (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	MIN.	MAX.	UNIT
Propagation Delay Time (D-Q)	t _{pLH} t _{pHL}	(Fig.1, 2)	2.7	—	8.0	ns
			3.3 ± 0.3	1.5	7.0	
Propagation Delay Time (LE-Q)	t _{pLH} t _{pHL}	(Fig.1, 2)	2.7	—	8.0	ns
			3.3 ± 0.3	1.5	7.0	
3-State Output Enable Time	t _{pZL} t _{pZH}	(Fig.1, 3)	2.7	—	8.2	ns
			3.3 ± 0.3	1.5	7.2	
3-State Output Disable Time	t _{pLZ} t _{pHZ}	(Fig.1, 3)	2.7	—	8.2	ns
			3.3 ± 0.3	1.5	7.2	
Minimum Pulse Width (LE)	t _w (H)	(Fig.1, 2)	2.7	4.0	—	ns
			3.3 ± 0.3	3.0	—	
Minimum Set-up Time	t _s	(Fig.1, 2)	2.7	2.5	—	ns
			3.3 ± 0.3	2.5	—	
Minimum Hold Time	t _h	(Fig.1, 2)	2.7	1.5	—	ns
			3.3 ± 0.3	1.5	—	
Output To Output Skew	t _{osLH} t _{osHL}	(Note 10)	2.7	—	—	ns
			3.3 ± 0.3	—	1.0	

(Note 10) Parameter guaranteed by design.

$$(t_{osLH} = |t_{pLHm} - t_{pLHn}|, t_{osHL} = |t_{pHLm} - t_{pHLn}|)$$

Dynamic switching characteristics

(Ta = 25°C, Input t_r = t_f = 2.5ns, C_L = 50pF, R_L = 500Ω)

PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP	UNIT
Quiet Output Maximum Dynamic V _{OL}	V _{OLP}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V
Quiet Output Minimum Dynamic V _{OL}	V _{OLV}	V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V

Capacitive characteristics (Ta = 25°C)

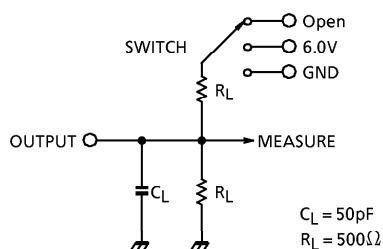
PARAMETER	SYMBOL	TEST CONDITION	V _{CC} (V)	TYP	UNIT
Input Capacitance	C _{IN}	—	3.3	7	pF
Output Capacitance	C _{OUT}		3.3	8	pF
Power Dissipation Capacitance	C _{PD}		3.3	25	pF

(Note 11) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 16. \text{ (Per bit)}$$

Fig.1 Test circuit



PARAMETER	SWITCH
t_{pLH} , t_{pHL}	Open
t_{pLZ} , t_{pZL}	6.0V
t_{pHZ} , t_{pZH}	GND
t_w , t_s , t_h	Open

AC WAVEFORM

Fig.2 t_{pLH} , t_{pHL} , t_w , t_s , t_h

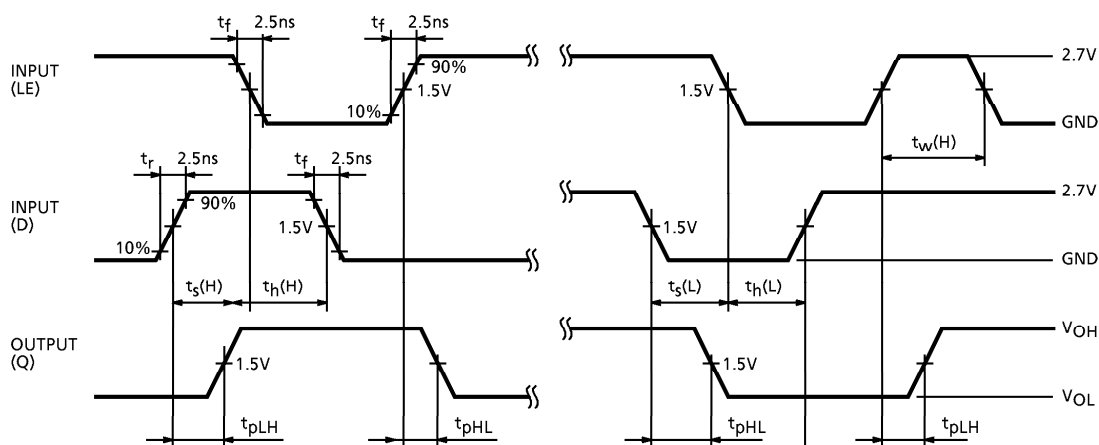
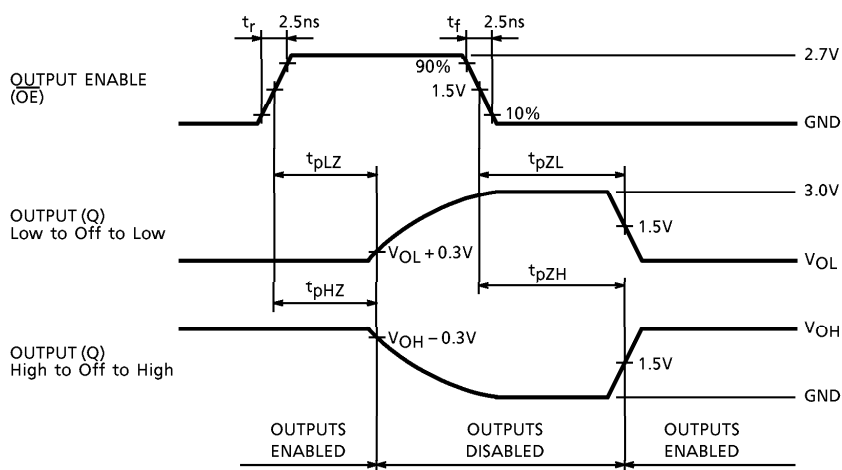


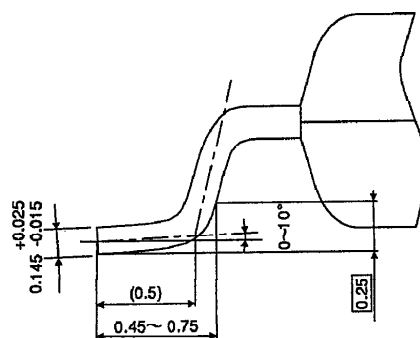
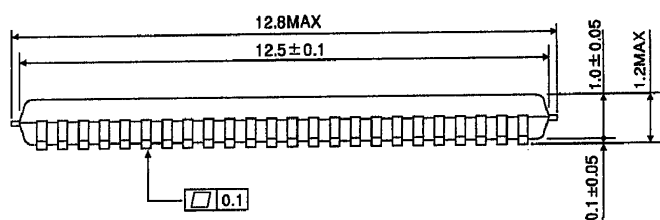
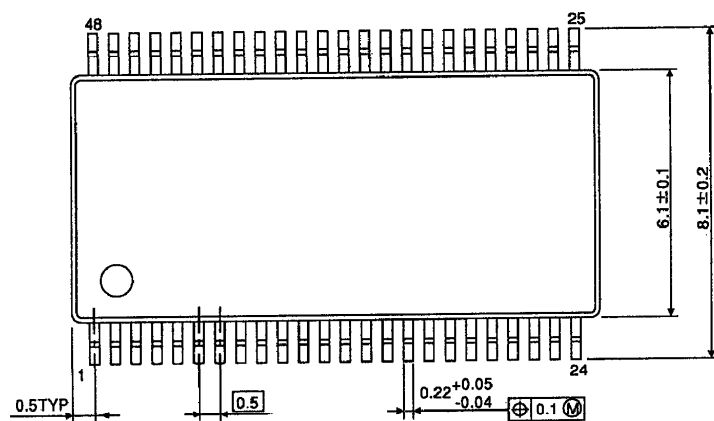
Fig.3 t_{pLZ} , t_{pHZ} , t_{pZL} , t_{pZH}



OUTLINE DRAWING

TSSOP48-P-0061-0.50

Unit : mm



Weight : 0.25g (Typ.)

Copyright Each Manufacturing Company.

All Datasheets cannot be modified without permission.

This datasheet has been download from :

www.AllDataSheet.com

100% Free DataSheet Search Site.

Free Download.

No Register.

Fast Search System.

www.AllDataSheet.com