19-1698; Rev 1; 2/01

MAXIM

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

General Description

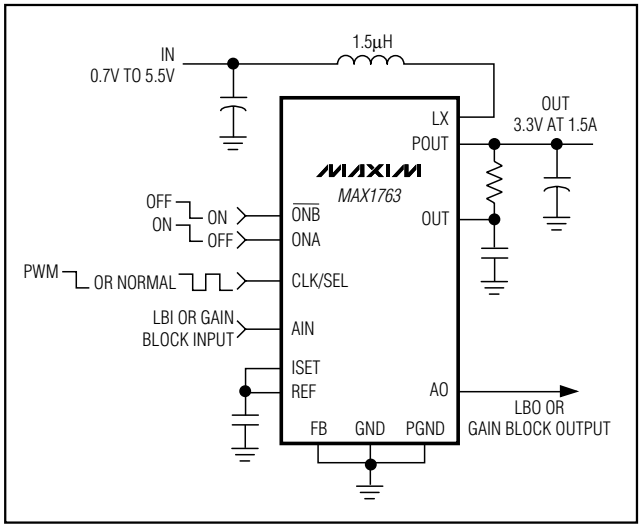
The MAX1763 is a high-efficiency, low-noise, step-up DC-DC converter intended for use in battery-powered wireless applications. This device maintains exceptionally low quiescent supply current (110µA) despite its high 1MHz operating frequency. Small external components and a tiny package make this device an excellent choice for small hand-held applications that require the longest possible battery life.

The MAX1763 uses a synchronous-rectified pulse-width-modulation (PWM) boost topology to generate 2.5V to 5.5V outputs from a wide range of input sources, such as one to three alkaline or NiCd/NiMH cells or a single Lithium-ion (Li+) cell. Maxim's proprietary Idle Mode™ circuitry significantly improves efficiency at light load currents while smoothly transitioning to fixed-frequency PWM operation at higher load currents to maintain excellent full-load efficiency. Low-noise, forced-PWM mode is available for applications that require constant-frequency operation at all load currents. The MAX1763 may also be synchronized to an external clock to protect sensitive frequency bands in communications equipment.

The MAX1763 includes an on-chip linear gain block that can be used to build a high-power external linear regulator or as a low-battery comparator. Soft-start and current limit functions permit optimization of efficiency, external component size, and output voltage ripple.

The MAX1763 is available in a space-saving 16-pin QSOP package or a high-power (1.5W) 16-pin TSSOP-EP package.

Typical Operating Circuit



Features

- ♦ **Up to 94% Efficiency**
- ♦ **+0.7V to +5.5V Input Voltage Range**
- ♦ **1.1V Guaranteed Startup Input Voltage**
- ♦ **Up to 1.5A Output**
- ♦ **Fixed 3.3V Output or Adjustable (2.5V to 5.5V)**
- ♦ **1MHz PWM Synchronous-Rectified Topology**
- ♦ **1µA Logic-Controlled Shutdown**
- ♦ **Analog Gain Block for Linear-Regulator or Low-Battery Comparator**
- ♦ **Adjustable Current Limit and Soft-Start**
- ♦ **1.5W TSSOP Package Available**

Applications

Digital Cordless Phones	Hand-Held Instruments
PCS Phones	Palmtop Computers
Wireless Handsets	Personal Communicators

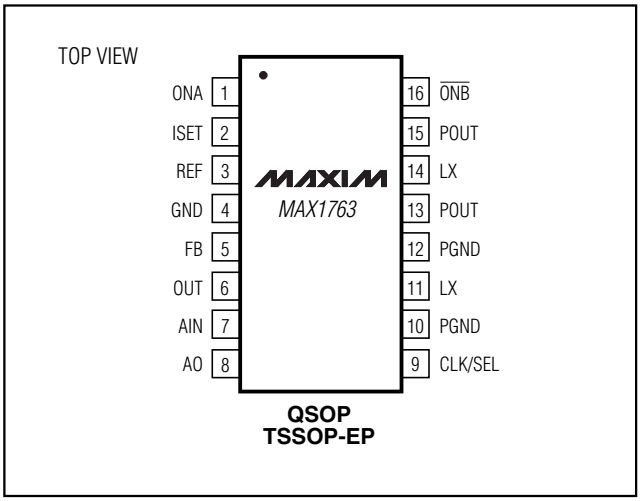
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1763EEE	-40°C to +85°C	16 QSOP
MAX1763EUE	-40°C to +85°C	16 TSSOP-EP*

**EP = Exposed pad*

Idle Mode is a trademark of Maxim Integrated Products.

Pin Configuration



1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

ONA, $\overline{ONB}$, AO, OUT to GND.....0.3V, +6V
PGND to GND.....±0.3V
LX to PGND .....-0.3V to (V_{POUT} + 0.3V)
CLK/SEL, REF, FB, ISET, POUT,
AIN to GND.....-0.3V to (V_{OUT} + 0.3V)
POUT to OUT .....±0.3V

Continuous Power Dissipation
16-Pin QSOP (derate 8.7mW/°C above +70°C).....667mW
16-Pin TSSOP-EP (derate 19mW/°C above +70°C).....1.5W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(CLK/SEL = $\overline{ONB}$ = FB = PGND = GND, ISET = REF, OUT = POUT, V_{ONA} = V_{AIN} = V_{OUT} = 3.6V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC-DC CONVERTER					
Input Voltage Range (Note 1)			0.7	5.5	V
Minimum Startup Voltage (Note 2)	I_{LOAD} < 1mA, T_A = +25°C		0.9	1.1	V
Temperature Coefficient of Startup Voltage	I_{LOAD} < 1mA		-2		mV/°C
Frequency in Startup Mode	V_{OUT} = 1.5V	125	500	1000	kHz
Internal Oscillator Frequency	CLK/SEL = OUT	0.8	1	1.2	MHz
Oscillator Maximum Duty Cycle (Note 3)		80	86	90	%
External Clock Frequency Range		0.5		1.2	MHz
Output Voltage	V_{FB} < 0.1V, CLK/SEL = OUT, includes load regulation for 0 < I_{LX} < 1.1A	3.17	3.3	3.38	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT, includes load regulation for 0 < I_{LX} < 1.1A	1.215	1.245	1.270	V
FB Input Current	V_{FB} = 1.35V		0.01	100	nA
Load Regulation	CLK/SEL = OUT, 0 < I_{LX} < 1.1A		-1.0		%
Output Voltage Adjust Range		2.5		5.5	V
Output Voltage Lockout Threshold (Note 4)	Rising edge	2.00	2.15	2.30	V
ISET Input Leakage Current	V_{ISET} = 1.25V		0.01	50	nA
Supply Current in Shutdown	$V_{\overline{ONB}}$ = 3.6V, V_{ONA} = 0		1	10	µA
No-Load Supply Current, Low-Power Mode (Note 5)	CLK/SEL = GND, AIN = OUT		110	200	µA
No-Load Supply Current, Low-Noise Mode	CLK/SEL = OUT		2.5		mA
Gain Block Supply Current	V_{AIN} < (V_{OUT} - 1.4V), gain block enabled		25	50	µA

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = $\overline{ONB}$ = FB = PGND = GND, ISET = REF, OUT = POUT, V_{ONA} = V_{AIN} = V_{OUT} = 3.6V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC-DC SWITCHES					
POUT Leakage Current	V_{LX} = 0, V_{OUT} = 5.5V		0.1	10	µA
LX Leakage Current	V_{LX} = $V_{\overline{ONB}}$ = V_{OUT} = 5.5V, V_{ONA} = 0		0.1	10	µA
Switch On-Resistance	N channel		0.075	0.13	Ω
	P channel		0.13	0.25	
N-Channel Current Limit		2.0	2.5	3.4	A
P-Channel Turn-Off Current	CLK/SEL = GND	10	120	240	mA
REFERENCE					
Reference Output Voltage	I_{REF} = 0	1.230	1.250	1.270	V
Reference Load Regulation	-1µA < I_{REF} < 50µA		5	15	mV
Reference Supply Rejection	2.5V < V_{OUT} < 5V		0.2	5	mV
GAIN BLOCK					
AIN Reference Voltage	I_{AO} = 20µA	910	938	970	mV
AIN Input Current	V_{AIN} = 1.5V		±0.01	±30	nA
Transconductance	V_{AO} = 1V, 10µA < I_{AO} < 100µA	5	10	16	mS
AO Output Low Voltage	V_{AIN} = 0.5V, I_{AO} = 100µA		0.1	0.4	V
AO Output High Leakage	V_{AIN} = 1.5V, V_{AO} = 5.5V		0.01	1	µA
Gain-Block Enable Threshold (V_{OUT} - V_{AIN}) (Note 6)				1.4	V
Gain-Block Disable Threshold (V_{OUT} - V_{AIN}) (Note 6)		0.2			V
LOGIC INPUTS					
CLK/SEL Input Low Level	2.5V ≤ V_{OUT} ≤ 5.5V			(0.2) V_{OUT}	V
CLK/SEL Input High Level	2.5 V ≤ V_{OUT} ≤ 5.5V	(0.8) V_{OUT}			V
ONA and $\overline{ONB}$ Input Low Level (Note 7)	1.1 V ≤ V_{OUT} ≤ 1.8V			0.2	V
	1.8 V ≤ V_{OUT} ≤ 5.5V			0.4	
ONA and $\overline{ONB}$ Input High Level (Note 7)	1.1 V ≤ V_{OUT} ≤ 1.8V	V_{OUT} - 0.2V			V
	1.8 V ≤ V_{OUT} ≤ 5.5V	1.6			
Input Leakage Current	CLK/SEL, ONA, $\overline{ONB}$		0.01	1	µA
Minimum CLK/SEL Pulse Width			100		ns
Maximum CLK/SEL Rise/Fall Time			100		ns

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

ELECTRICAL CHARACTERISTICS

(CLK/SEL = $\overline{ONB}$ = FB = PGND = GND, ISET = REF, OUT = POUT, V_{ONA} = V_{AIN} = V_{OUT} = 3.6V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 8)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
DC-DC CONVERTER				
Input Voltage Range (Note 1)			5.5	V
Minimum Startup Voltage (Note 2)	I_{LOAD} < 1mA, T_A = +25°C		1.1	V
Frequency in Startup Mode	V_{OUT} = 1.5V	125	1000	kHz
Internal Oscillator Frequency	CLK/SEL = OUT	0.75	1.25	MHz
Oscillator Maximum Duty Cycle (Note 3)		80	91	%
External Clock Frequency Range		0.6	1.2	MHz
Output Voltage	V_{FB} < 0.1V, CLK/SEL = OUT, includes load regulation for 0 < I_{LX} < 1.1A	3.17	3.38	V
FB Regulation Voltage	Adjustable output, CLK/SEL = OUT, includes load regulation for 0 < I_{LX} < 1.1A	1.215	1.270	V
FB Input Current	V_{FB} = 1.35V		100	nA
Output Voltage Adjust Range		2.5	5.5	V
Output Voltage Lockout Threshold (Note 4)	Rising edge	2.00	2.30	V
ISET Input Leakage Current	V_{ISET} = 1.25V		50	nA
Supply Current in Shutdown	$V_{\overline{ONB}}$ = 3.6V, V_{ONA} = 0		10	µA
No-Load Supply Current, Low-Power Mode (Note 5)	CLK/SEL = GND, AIN = OUT		200	µA
Gain Block Supply Current	V_{AIN} < (V_{OUT} - 1.4V), gain block enabled		50	µA
DC-DC SWITCHES				
POUT Leakage Current	V_{LX} = 0, V_{OUT} = 5.5V		10	µA
LX Leakage Current	V_{LX} = $V_{\overline{ONB}}$ = V_{OUT} = 5.5V, V_{ONA} = 0		10	µA
Switch On-Resistance	N-channel		0.13	Ω
	P-channel		0.25	
N-Channel Current Limit		2.0	3.4	A
P-Channel Turn-Off Current	CLK/SEL = GND	10	240	mA
REFERENCE				
Reference Output Voltage	I_{REF} = 0	1.220	1.270	V
Reference Load Regulation	-1µA < I_{REF} < 50µA		15	mV
Reference Supply Rejection	2.5V < V_{OUT} < 5V		5	mV
GAIN BLOCK				
AIN Reference Voltage	I_{AO} = 20µA	910	970	mV
AIN Input Current	V_{AIN} = 1.5V		±30	nA
Transconductance	V_{AO} = 1V, 10µA < I_{AO} < 100µA	5	16	mS
AO Output Low Voltage	V_{AIN} = 0.5V, I_{AO} = 100µA		0.4	V
AO Output High Leakage	V_{AIN} = 1.5V, V_{AO} = 5.5V		1	µA

ELECTRICAL CHARACTERISTICS (continued)

(CLK/SEL = $\overline{ONB}$ = FB = PGND = GND, ISET = REF, OUT = POUT, V_{ONA} = V_{AIN} = V_{OUT} = 3.6V, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 8)

PARAMETER	CONDITIONS	MIN	MAX	UNITS
LOGIC INPUTS				
Gain-Block Enable Threshold (V_{OUT} - V_{AIN}) (Note 6)			1.4	V
Gain-Block Disable Threshold (V_{OUT} - V_{AIN}) (Note 6)		0.2		V
CLK/SEL Input Low Level	2.5 V ≤ V_{OUT} ≤ 5.5V		(0.2) V_{OUT}	V
CLK/SEL Input High Level	2.5 V ≤ V_{OUT} ≤ 5.5V	(0.8) V_{OUT}		V
ONA and $\overline{ONB}$ Input Low Level (Note 7)	1.1 V ≤ V_{OUT} ≤ 1.8V		0.2	V
	1.8 V ≤ V_{OUT} ≤ 5.5V		0.4	
ONA and $\overline{ONB}$ Input High Level (Note 7)	1.1 V ≤ V_{OUT} ≤ 1.8V	V_{OUT} - 0.2V		V
	1.8V ≤ V_{OUT} ≤ 5.5V	1.6		
Input Leakage Current	CLK/SEL, ONA, $\overline{ONB}$		1	µA

Note 1: Operating voltage. Because the regulator is bootstrapped to the output, once started, the MAX1763 will operate down to 0.7V input.

Note 2: Startup is tested with the circuit of Figure 2.

Note 3: Defines low-noise mode maximum step-up ratio.

Note 4: The regulator is in startup mode until this voltage is reached. Do not apply full load current until the output exceeds 2.3V.

Note 5: Supply current from the 3.3V output is measured between the 3.3V output and the OUT pin. This current correlates directly to the actual battery-supply current, but is reduced in value according to the step-up ratio and efficiency. The gain block is disabled.

Note 6: Connect AIN to OUT to disable gain block.

Note 7: ONA and $\overline{ONB}$ have hysteresis of approximately 0.15 × V_{OUT}.

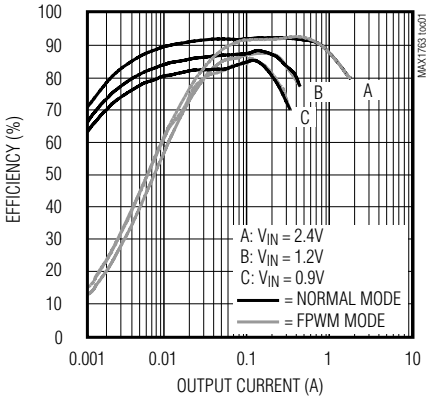
Note 8: Specifications to -40°C are guaranteed by design and not production tested.

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

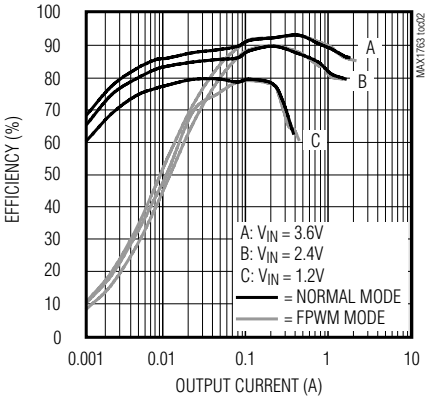
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = +3.6V, V_{OUT} = +5V, T_A = +25°C, unless otherwise noted.)

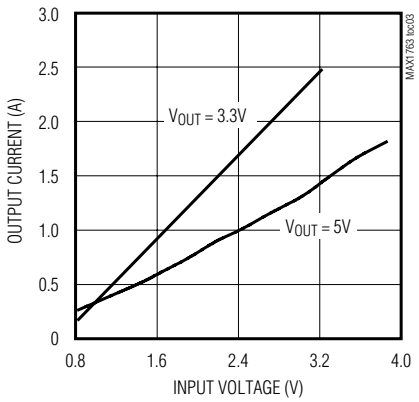
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.3V)



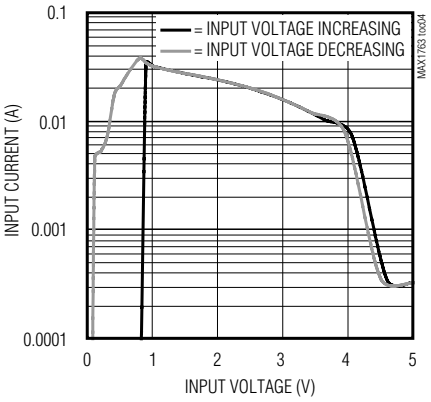
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5V)



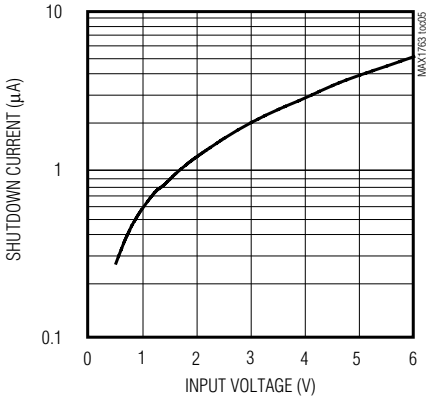
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



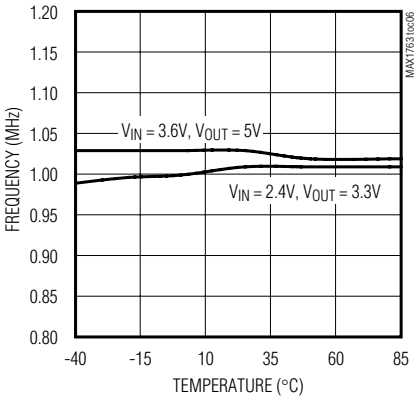
NO-LOAD INPUT vs. INPUT VOLTAGE



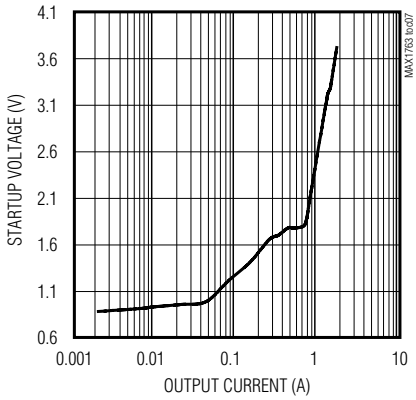
SHUTDOWN CURRENT vs. INPUT VOLTAGE



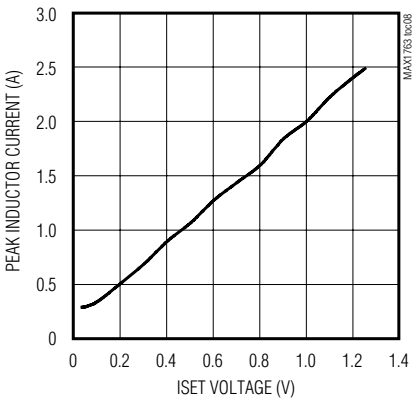
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



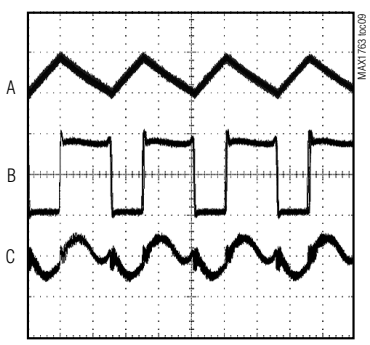
STARTUP VOLTAGE vs. OUTPUT CURRENT



PEAK INDUCTOR CURRENT vs. V_{ISET}



HEAVY-LOAD SWITCHING WAVEFORMS



V_{IN} = 2.4V, V_{OUT} = 3.3V, I_{OUT} = 1.5A
A: INDUCTOR CURRENT, 500mA/div
B: V_{LX}, 2V/div
C: V_{OUT}, 100mV/div, AC COUPLED

Typical Operating Characteristics (continued)

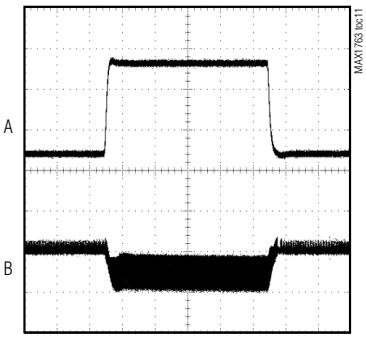
(Circuit of Figure 2, V_{IN} = +3.6V, V_{OUT} = +5V, T_A = +25°C, unless otherwise noted.)

LIGHT-LOAD SWITCHING WAVEFORMS

200ns/div

V_{IN} = 1.1V, V_{OUT} = 3.3V, I_{OUT} = 20mA
A: LX NODE, 5V/div
B: INDUCTOR CURRENT, 0.1A/div, AC COUPLED
C: OUTPUT RIPPLE, 0.1V/div, AC COUPLED

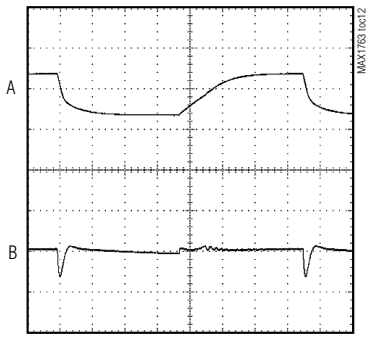
LOAD-TRANSIENT RESPONSE



100µs/div

V_{IN} = 2.4V, V_{OUT} = 3.3V, I_{OUT} = 0.2A TO 1.35A
A: I_{OUT}, 0.5A/div
B: V_{OUT}, 100mV/div, AC-COUPLED

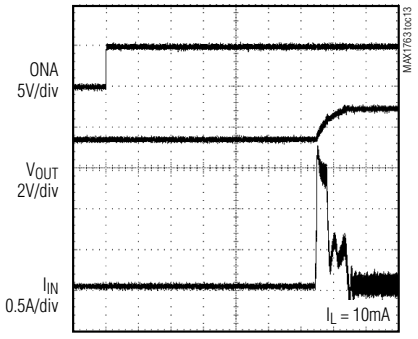
LINE-TRANSIENT RESPONSE



40µs/div

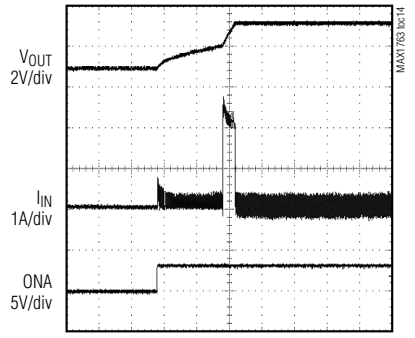
V_{IN} = 2.4V TO 1.4V, I_{OUT} = 70mA
A: V_{IN}, 1V/div
B: V_{OUT}, 5mV/div, AC-COUPLED

POWER-ON DELAY



100µs/div

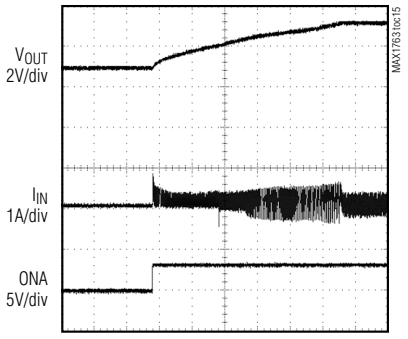
STARTUP WAVEFORMS NO SOFT-START



2ms/div

V_{IN} = 1.2V, V_{OUT} = 3.3V, R_{LOAD} = 3kΩ

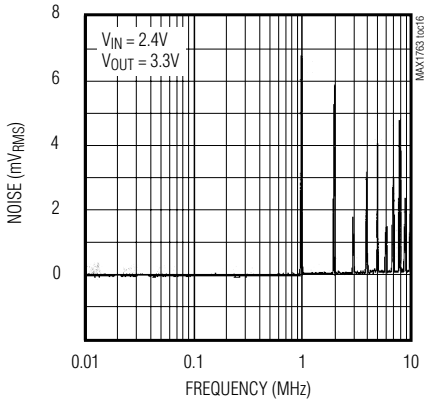
STARTUP WAVEFORMS USING SOFT-START



2ms/div

V_{IN} = 1.2V, V_{OUT} = 3.3V, R_{SS} = 510kΩ, C_{SS} = 0.1µF, R_{LOAD} = 3kΩ

NOISE SPECTRUM



1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

Pin Description

PIN	NAME	FUNCTION
1	ONA	On Control Input. When ONA = high or $\overline{ONB}$ = low, the IC turns on. Connect ONA to OUT for normal operation (Table 3).
2	ISET	N-Channel Current Limit Control. For maximum current limit, connect to REF. To reduce current, supply a voltage between REF and GND by means of a resistive voltage-divider. If soft-start is desired, connect a capacitor from ISET to GND. When ONA = low and $\overline{ONB}$ = high, or V_{REF} < 80% of nominal value, an on-chip switched resistor (100kΩ typ) discharges this pin to GND.
3	REF	1.250V Voltage Reference Bypass Pin. Connect a 0.22µF ceramic bypass capacitor to GND. Up to 50µA of external REF load current is allowed.
4	GND	Ground. Connect to PGND with short trace.
5	FB	DC-DC Converter Feedback Input. To set fixed output voltage of +3.3V, connect FB to ground. For adjustable output of 2.5V to 5.5V, connect to a resistive divider placed from OUT to GND. FB set point is 1.245V (Figure 6).
6	OUT	IC Power, Supplied from the Output. Bypass to GND with a 1.0µF ceramic capacitor, and connect to POUT with a series 4.7Ω resistor (Figure 2).
7	AIN	Gain-Block Input. The nominal transconductance from AIN to AO is 10mS. An external P-channel pass device can be used to build a linear regulator. The gain block can also be used as a low-battery comparator with a threshold of 0.938V. The gain block and its associated quiescent current are disabled by connecting AIN to OUT.
8	AO	Gain-Block Output. This open-drain N-channel output sinks current when V_{AIN} < (0.75)(V_{REF}). AO is high-Z when the device is shut down, or when AIN = OUT.
9	CLK/SEL	Clock Input for the DC-DC Converter. Also serves to program the operating mode of the switcher as follows: **CLK/SEL = LO:** Normal; operates at a fixed frequency, automatically switching to low-power mode if load is minimized. **CLK/SEL = HI:** Forced PWM mode; operates in low-noise, constant-frequency mode at all loads. **CLK/SEL = Clocked:** Forced PWM mode with the internal oscillator synchronized to CLK in 500kHz to 1200kHz range.
10, 12	PGND	Source of N-Channel Power MOSFET Switch. Connect both PGND pins together close to the device.
11, 14	LX	Inductor Connection. Connect the LX pins together close to the device.
13, 15	POUT	Power Output. P-channel synchronous rectifier source.
16	$\overline{ONB}$	Off Control Input. When $\overline{ONB}$ = high and ONA = low, the IC is off. Connect $\overline{ONB}$ to GND for normal operation (Table 3).

Detailed Description

The MAX1763 is a highly-efficient, low-noise power supply for portable RF and hand-held instruments. It combines a boost switching regulator, N-channel power MOSFET, P-channel synchronous rectifier, precision reference, shutdown control, and a versatile gain block (Figure 1).

The DC-DC converter boosts a one-cell to three-cell battery voltage input to a fixed 3.3V or adjustable voltage between 2.5V and 5.5V. An external Schottky diode is required for output voltages greater than 4V. The MAX1763 guarantees startup with an input voltage as low as 1.1V and remains operational down to an input of just 0.7V. It is optimized for use in cellular phones and other applications requiring low noise and low quiescent current for maximum battery life. It features constant-frequency (1MHz), low-noise PWM operation with up to 1.5A output capability. A CLK input allows frequency synchronization to control the output

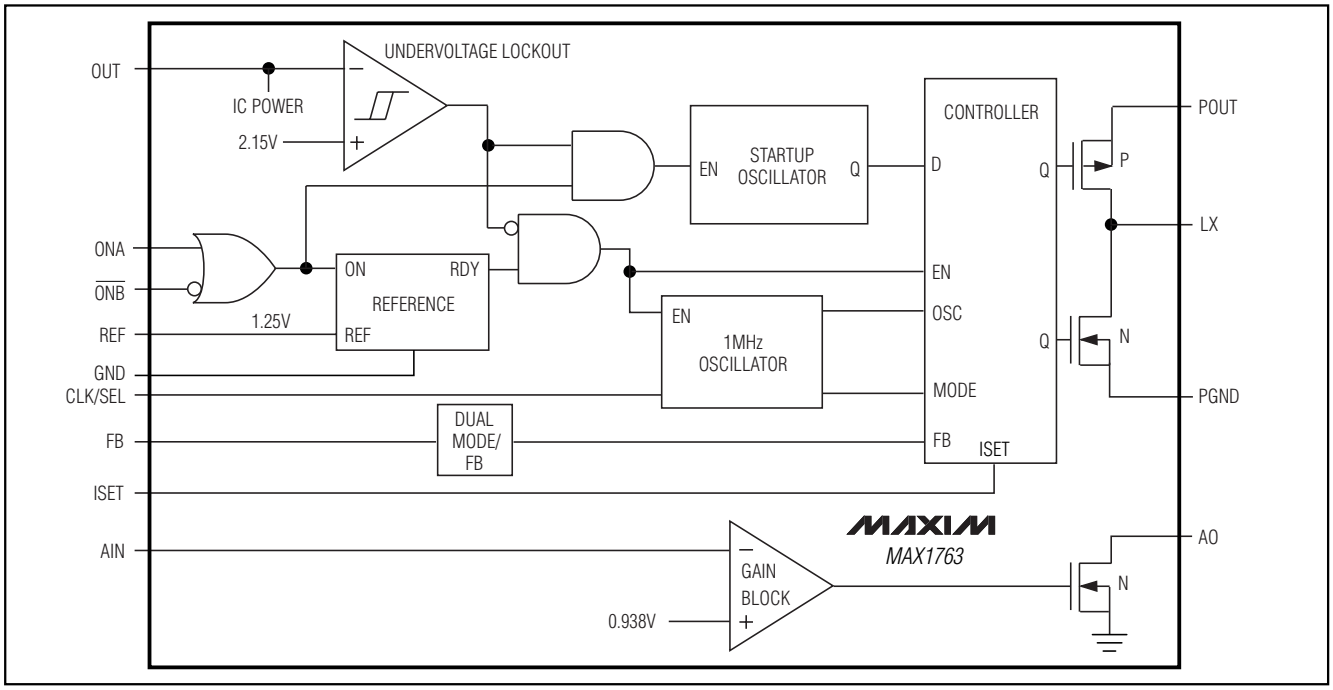


Figure 1. Functional Diagram

Table 1. Typical Available Output Current

NUMBER OF CELLS	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	OUTPUT CURRENT (mA)
1 NiCd/NiMH	1.2	3.3	675
2 NiCd/NiMH	2.4	3.3	1500
	2.4	5.0	950
1 Li+	2.7 (min)	3.3	1300
1 Li+	2.7 (min)	5.0	1100
3 NiCd/NiMH	3.6	5.0	1600

noise spectrum. See Table 1 for typical available output current.

In its normal mode of operation (CLK/SEL = low), the MAX1763 offers fixed-frequency PWM operation through most of its load range. At light loads (less than 25% of full load), the device automatically optimizes efficiency by switching only as needed to supply the load. Shutdown reduces quiescent current to just 1µA. Figure 2 shows the standard application circuit for the MAX1763. (An external Schottky diode is needed for output voltages greater than 4V, or to assist low-voltage startup.)

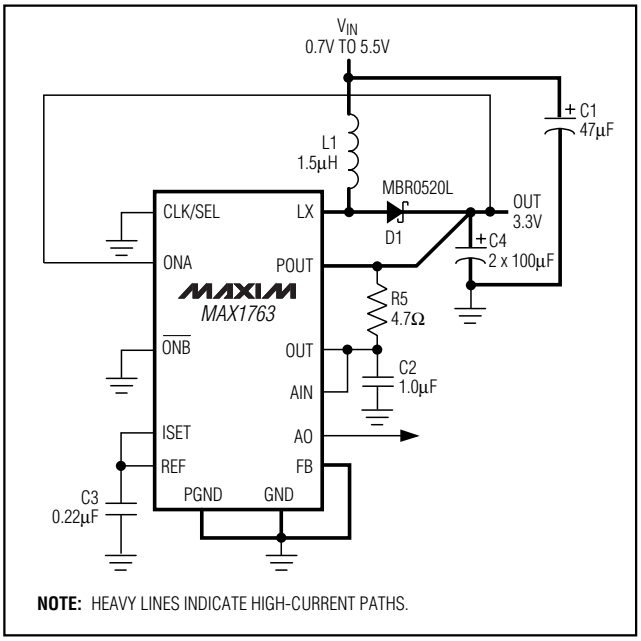


Figure 2. PFM/PWM Automode Connection

Additional features include synchronous rectification for high efficiency and increased battery life, and a gain block that can be used to build a linear regulator using an external P-channel MOSFET pass device. This gain

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

Table 2. Selecting the Operating Mode

CLK/SEL	MODE	FEATURES
0	Normal operation	High efficiency at all loads. Fixed frequency at all but light loads.
1	Forced PWM	Low noise, fixed frequency at all loads.
External clock 500kHz to 1.2MHz	Synchronized PWM	Low noise, fixed frequency at all loads.

block can also function as a voltage-monitoring comparator. The MAX1763 is available in a 16-pin QSOP package or a 1.5W 16-pin TSSOP-EP package for high-temperature or high-dissipation applications.

Step-Up Converter

During DC-DC converter operation, the internal N-channel MOSFET switch turns on for the first part of each cycle, allowing current to ramp up in the inductor and store energy in a magnetic field. During the second part of each cycle, the MOSFET turns off and inductor current flows through the synchronous rectifier to the output filter capacitor and the load. As the energy stored in the inductor is depleted, the current ramps down and the synchronous rectifier turns off, the N-channel FET turns on, and the cycle repeats. At light loads, depending on the CLK/SEL pin setting, output voltage is regulated using either PWM or by switching only as needed to service the load (Table 2).

Normal Operation

Pulling CLK/SEL low selects the MAX1763's normal operating mode. In this mode, the device operates in PWM when driving medium to heavy loads, and at light loads only, switches as needed. This optimizes efficiency over the widest range of load conditions. In normal operation mode, the output voltage regulates 1% higher than in forced-PWM mode. See Efficiency vs. Load Current in the *Typical Operating Characteristics* section.

Forced-PWM Operation

When CLK/SEL is high, the MAX1763 operates in a low-noise forced-PWM mode. During forced-PWM operation, the MAX1763 switches at a constant frequency (1MHz) and modulates the MOSFET switch pulse width to control the power transferred per cycle and regulate the output voltage. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered. See the Noise Spectrum plot in the *Typical Operating Characteristics*.

Synchronized-PWM Operation

In a variation of forced-PWM mode, the MAX1763 can be synchronized to an external frequency by applying a clock signal to CLK/SEL. This allows the user to choose an operating frequency (from 500kHz to 1.2MHz) to avoid interference in sensitive applications. For the most noise-sensitive applications, limit the external synchronization signal duty cycle to less than 10% or greater than 90%. This eliminates the possibility that noise from the power switching will coincide with the synchronization signal. If the synchronization signal edge falls on the power switching edge, a slight frequency jitter may occur.

Synchronous Rectifier

The MAX1763 features an internal 130mΩ P-channel synchronous rectifier to enhance efficiency. Synchronous rectification provides a 5% efficiency improvement over similar boost regulators that rely on diode rectifiers. In PWM mode, the synchronous rectifier is turned on during the second half of each switching cycle. In low-power mode, an internal comparator turns on the synchronous rectifier when the voltage at LX exceeds the boost regulator output and turns it off when the inductor current drops below 120mA. When setting output voltages greater than 4V, an external 0.5A Schottky diode must be connected in parallel with the on-chip synchronous rectifier.

Low-Voltage Startup Oscillator

The MAX1763 uses a CMOS low-voltage startup oscillator for a 1.1V guaranteed minimum startup input voltage. At startup, the low-voltage oscillator switches the N-channel MOSFET until the output voltage reaches 2.15V. Above this level, the normal feedback and control circuitry take over. Once the device is in regulation, it can operate down to 0.7V input because internal power for the IC is derived from the output through the OUT pin. Do not apply full system load until the output exceeds 2.3V.

Shutdown, ONA, $\overline{ONB}$

ONA and $\overline{ONB}$ turn the MAX1763 on or off. When ONA = 1 or $\overline{ONB}$ = 0, the device is on. When ONA = 0 and $\overline{ONB}$ = 1, the device is off (Table 3). Logic high ON control can be implemented by connecting $\overline{ONB}$ high and using ONA for the control input. Momentary one-pushbutton ON/OFF control is described in the *Applications Information* section. Both ONA and $\overline{ONB}$ have approximately $(0.15 \times V_{OUT})$V of hysteresis.

Reference

The MAX1763 has an internal 1.250V reference. Connect a 0.22µF ceramic bypass capacitor to GND

Table 3. On/Off Logic Control

ONA	$\overline{ONB}$	MAX1763
0	0	On
0	1	Off
1	0	On
1	1	On

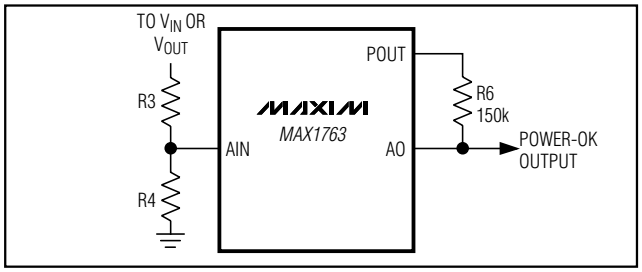


Figure 3. Using the Gain Block as a Power-OK Comparator

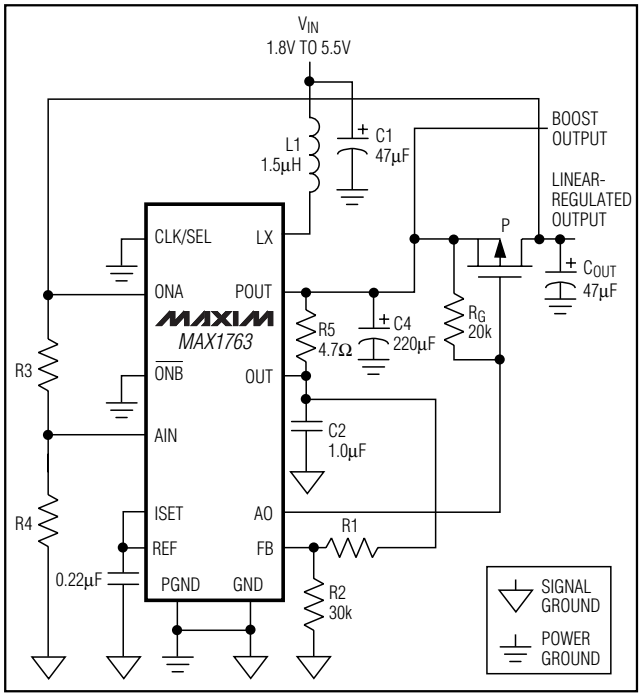


Figure 4. Using the Gain Block as a Linear Regulator from the Boosted Output Voltage

within 0.2in (5mm) of the REF pin. REF can source up to 50µA of external load current.

Gain Block

The MAX1763 gain block can function as a power-OK comparator or can be used to build a linear regulator

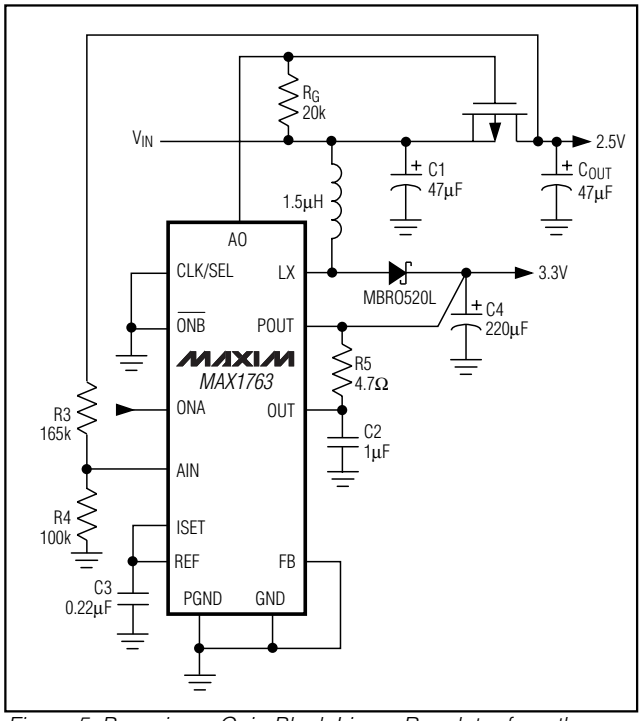


Figure 5. Powering a Gain-Block Linear Regulator from the Input Voltage

using an external P-channel MOSFET pass device. The gain-block output is a single-stage transconductance amplifier that drives an open-drain N-channel MOSFET. The transconductance (G_M) of the entire gain-block stage is 10mS. The internal gain block amplifies the difference between AIN and the internal 0.938V reference.

To provide a power-OK signal, connect the gain-block input, AIN, to an external resistor-divider (Figure 3). The input bias current into AIN is less than 30nA, allowing large-value divider resistors without sacrificing accuracy. Connect the resistor voltage-divider as close to the IC as possible, within 0.2in (5mm) of AIN. Choose an R4 value of 270kΩ or less, then calculate R3 using:

$$R3 = R4((V_{TRIP} / V_{AIN}) - 1)$$

where V_{AIN} is 0.938V.

Figures 4 and 5 show the gain block used in a linear-regulator application. The output of an external P-channel pass element is compared to an internal 0.938V reference. The difference is amplified and drives the gate of the pass element. Use a logic-level PFET, such as Fairchild's NDS336P ($R_{DS(ON)}$ = 270mΩ). When the linear-regulator output voltage is in regulation, the MOSFET will not be full on; thus, the on-resistance will not be important. However, if the linear regulator is used

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

in dropout, the MOSFET on-resistance will determine the dropout voltage ($V_{DROPOUT} = I_{OUT} \times R_{DS(ON)}$). If a lower $R_{DS(ON)}$ PFET is used, increase the linear-regulator output filter capacitance to maintain stability.

The output capacitance can be determined by the function:

$$C_{OUT} \geq [(V_{REF} / V_{OUT}) \times G_M \times G_{FS} \times C_G \times (R_G \times 2)]$$

and

$$C_{OUT} \geq 10 \times [(V_{REF} / [V_{OUT} \times GBP]) \times G_M \times G_{FS} \times R_G]$$

where V_{REF} is the 0.983V reference voltage, G_M is the 10mS internal amplifier transconductance, G_{FS} is the external MOSFET transconductance, R_G is the gate-source resistor, and GBP is the gain-bandwidth product of the internal gain block, 63Mrad/s.

Design Procedure

Setting the Output Voltage

For a fixed 3.3V output, connect FB to GND. To set the output voltage between 2.5V and 5.5V, connect a resistor voltage-divider to FB from OUT to GND (Figure 6). The input bias current into FB is less than 100nA, allowing large-value divider resistors without sacrificing accuracy. Connect the resistor voltage-divider as close to the IC as possible, within 0.2in (5mm) of FB. Choose R2 of 30kΩ or less, then calculate R1 using:

$$R1 = R2((V_{OUT} / V_{FB}) - 1)$$

where V_{FB}, the boost-regulator feedback set point, is 1.245V.

Setting the Switch Current Limit and Soft-Start

The ISET pin adjusts the inductor peak current and can also be used to implement soft-start. With ISET connected to REF, the inductor current limits at 2.5A. With ISET connected to a resistive divider set from REF to GND, the current limit is reduced according to:

$$I_{LIM} = 2.5(V_{ISET} / 1.25) [A]$$

Implement soft-start by placing a resistor from ISET to REF (>300kΩ) and a capacitor from ISET to GND. In shutdown, ISET is discharged to GND through an internal 100kΩ resistor. As the capacitor voltage rises, the output current is allowed to increase, and the output voltage rises. The speed at which the output rises is determined by the soft-start time constant:

$$t_{SS} = R_{SS} C_{SS}$$

where $R_{SS} \geq 300k$.

Both features may be implemented simultaneously by placing a capacitor across the lower resistor of the current-limiting resistive divider (Figures 7 and 8).

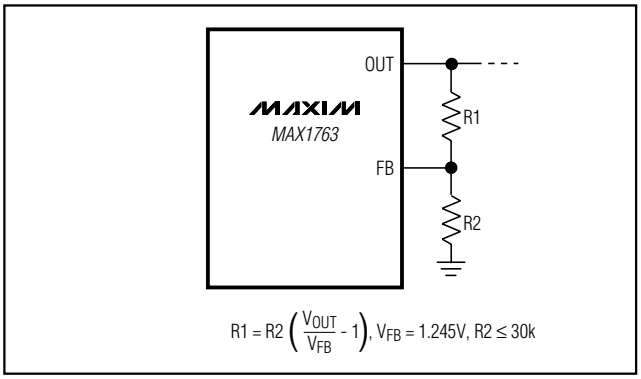


Figure 6. Connecting Resistors for External Feedback

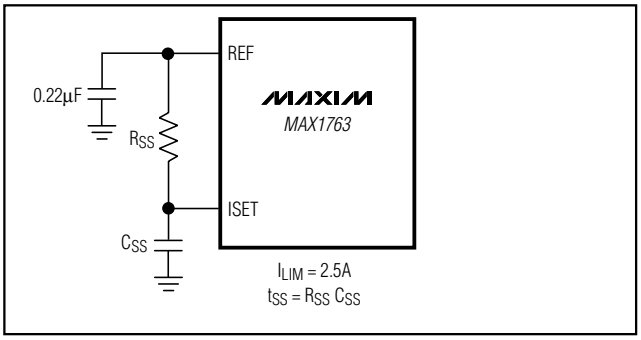


Figure 7. Soft-Start with Maximum Switch Limit Current

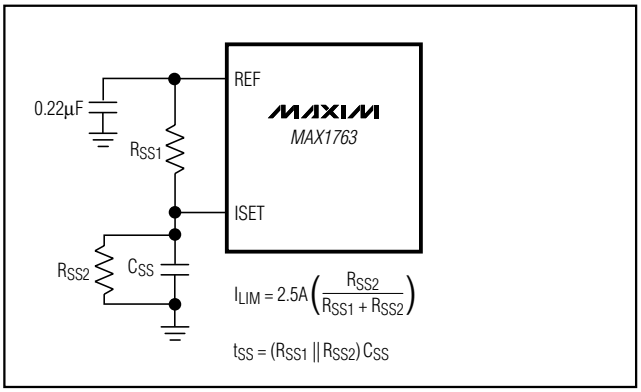


Figure 8. Soft-Start with Reduced Switch Limit Current

Package Selection

The MAX1763 is available in two packages, a 16-pin QSOP and a 16-pin TSSOP-EP. Since the MAX1763 has excellent efficiency, most applications are well served by the QSOP package. If the application requires high power dissipation, or operation in a high ambient temperature, choose the TSSOP-EP package. The TSSOP-EP is equipped with an exposed metal pad on its underside for soldering to grounded circuit board copper. This reduces the junction-to-case thermal

Table 4. Component Selection Guide

INDUCTORS	CAPACITORS	DIODES
Coilcraft LPT3305	AVX TPS series	Motorola MBR0520L
	Kemet T510 series	
	Sanyo POSCAP series	
Sumida	Panasonic SP/CB	Nihon EP10QY03

resistance of the package from +115°C/W for QSOP to +53°C/W for the TSSOP-EP.

At an ambient temperature of +70°C, continuous power dissipation for the QSSOP package is 667mW, while the TSSOP-EP can dissipate 1.5W. A first-order estimate of power dissipation can be determined by calculating the output power delivered to the load (e.g., 3.3V × 1A = 3.3W). At the input voltage used, find the efficiency from the *Typical Operating Characteristics* graphs (e.g., 87%). The estimated power dissipation in the MAX1763 is then: (100% - %Efficiency) × Output Power. The example would have: 13% × 3.3W = 0.43W, allowing the QSOP package (667mW) to be used. For higher ambient temperature, higher output power, or a lower-efficiency operating point, the TSSOP-EP package (1.5W) may be necessary. For detailed package mechanical information, see the package outline drawings at the end of this data sheet.

Inductor Selection

The MAX1763's high switching frequency allows the use of a small 1.5µH surface-mount inductor. The chosen inductor should generally have a saturation current rating exceeding the N-channel switch current limit; however, it is acceptable to bias the inductor current into saturation by as much as 20% if a slight reduction in efficiency is acceptable. Inductors rated for lower peak current may be used if ISET is employed to reduce the peak inductor current (see *Setting the Switch Current Limit and Soft-Start*). For high efficiency, choose an inductor with a high-frequency ferrite core material to reduce core losses. To minimize radiated noise, use a toroid or shielded inductor. See Table 4 for suggested components and Table 5 for a list of component suppliers. Connect the inductor from the battery to the LX pins as close to the IC as possible.

External Diode

For output voltages greater than 4V, an external Schottky diode must be connected from LX to POUT, in parallel with the on-chip synchronous rectifier (Figure 2). The diode should be rated for 0.5A. Representative devices are Motorola MBR0520L, Nihon EP05Q03L, or generic 1N5817. This external diode is also recommended for applications that must start with input voltages at or below 1.8V. The Schottky diode carries current during both startup and after the synchronous rectifier turns off. Thus, its current rating only needs to be 500mA even if the inductor current is higher. Connect the diode as close to the IC as possible. Do not use ordinary rectifier diodes; their slow switching speeds and long reverse-recovery times render them unacceptable. For circuits that do not require startup with inputs below 1.8V, and have an output of 4V or less, no external diode is needed.

Table 5. Component Suppliers

SUPPLIER	PHONE
AVX	USA: 843-448-9411
Coilcraft	USA: 847-639-6400
Kemet	USA: 810-287-2536
Motorola	USA: 408-629-4789 Japan: 81-45-474-7030
Sumida	USA: 847-956-0666 Japan: 011-81-3-3667-3302

Note: *Please indicate that you are using the MAX1763 when contacting these component suppliers.*

Input and Output Capacitors

Choose input and output capacitors that will service the input and output peak currents with acceptable voltage ripple. Choose input capacitors with working voltage ratings over the maximum input voltage, and output capacitors with working voltage ratings higher than the output. A 220µF, low equivalent-series-resistance (ESR) (less than 100mΩ) capacitor is recommended for most applications. Alternatively, two 100µF capacitors in parallel will reduce the effective ESR for even better performance.

The input capacitor reduces peak currents drawn from the input source and also reduces input switching noise. The input voltage source impedance determines the required size of the input capacitor. When operating directly from one or two NiMH cells placed close to the MAX1763, use a single 47µF low-ESR input filter capacitor. With higher impedance batteries, such as alkaline and Li+, a higher value input capacitor may improve efficiency.

Sanyo POSCAP, Panasonic SP/CB, and Kemet T510 are good low-ESR capacitors (Tables 4 and 5). Low-ESR tantalum capacitors offer a good trade-off between price and performance. Do not exceed the ripple current ratings of tantalum capacitors. Avoid aluminum

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

electrolytic capacitors; their high ESR typically results in higher output ripple voltage.

Bypass Components

A few ceramic bypass capacitors are required for proper operation. Bypass REF to GND with 0.22µF. Also, bypass OUT to GND with a 1µF ceramic capacitor, and connect OUT to POUT with a 4.7Ω resistor. Each of these components should be placed as close to their respective IC pins as possible, within 0.2in (5mm). Table 5 lists suggested suppliers.

Layout Considerations

High switching frequencies and large peak currents make PC board layout a critical part of design. Poor design will cause excessive EMI and ground bounce, both of which can cause instability or regulation errors by corrupting the voltage and current feedback signals.

Power components, such as the inductor, converter IC, and filter capacitors, should be placed as close together as possible, and their traces should be kept short, direct, and wide. Keep the voltage feedback network very close to the IC, within 0.2in (5mm) of the FB pins. Keep noisy traces, such as those from the LX pin, away from the voltage feedback networks and guarded from them using grounded copper. If an external rectifier is used, its traces must be kept especially short and use an absolute minimum of copper area to avoid excess capacitance that can slow the operation of the on-chip synchronous rectifier and actually reduce efficiency. Refer to the MAX1763 EV kit for a full PC board example.

The MAX1763 TSSOP-EP package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a direct thermal heat path from the die to the PC board. Additionally, the ground pin (GND) also channels heat. Connect the exposed thermal pad and GND to circuit ground by using a large pad or multiple vias to the ground plane.

Step-Up/Step-Down Applications

In some battery-powered applications, the battery voltage range overlaps the output voltage. In this case, depending on the battery voltage, the regulator will have to step the voltage up or down. To make a step-up/step-down regulator, use the gain block to make a linear regulator that follows the step-up converter. In this case, if the battery voltage is low, then the circuit will step up, and when the battery voltage is high, the linear regulator will drop the voltage. See the *Gain Block* section on how to use the gain block to make a linear regulator. When the output voltage is greater than the regulation voltage, then the synchronous rectifier will be held on, reducing the dropout, and thus increasing the efficiency when the battery voltage is close to, but slightly above, the regulation voltage.

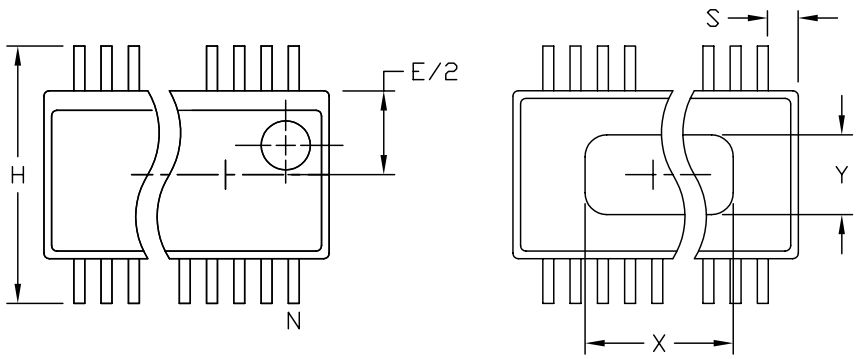
Chip Information

TRANSISTOR COUNT: 1530

SUBSTRATE CONNECTED TO GND

Package Information

QSOP.EPS



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.102	0.249
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.191	0.249
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
X	SEE VARIATIONS			
Y	.071	.087	1.803	2.209
α	0°	8°	0°	8°

VARIATIONS:

	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
X	.107	.123	2.72	3.12		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.270	1.397		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.635	0.762		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.635	0.762		
X	.271	.287	6.88	7.29		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006" PER SIDE.
3. HEAT SLUG DIMENSIONS X AND Y APPLY ONLY TO 16 AND 28 LEAD POWER-QSOP PACKAGES.
4. CONTROLLING DIMENSIONS: INCHES.
5. MEETS JEDEC MO137.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, QSOP, .150", .025" LEAD PITCH

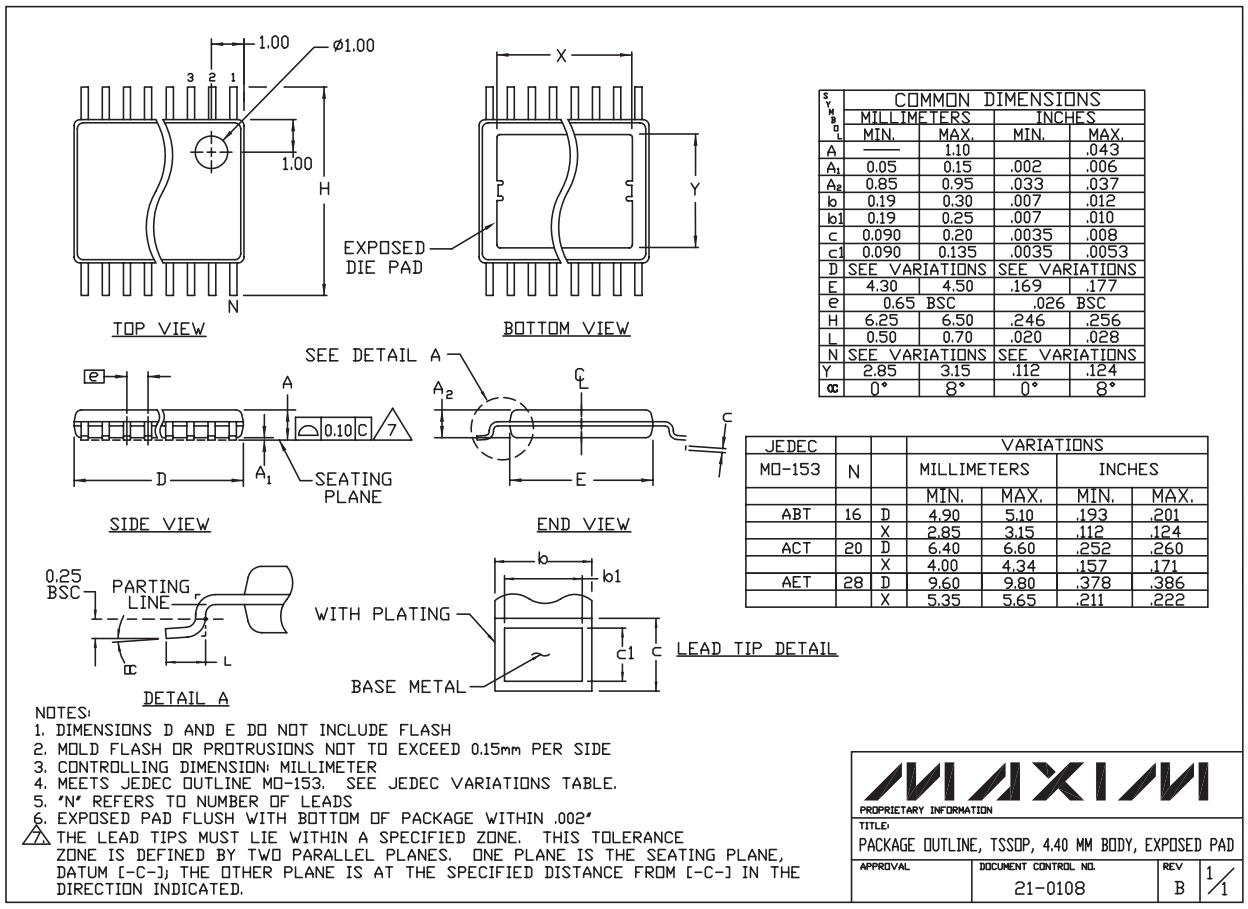
APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0055	C	1/1

Note: *The MAX1763EEE is a 16-pin QSOP and does not have a heat slug. Use the MAX1763EUE for higher power dissipation.*

1.5A, Low-Noise, 1MHz, Step-Up DC-DC Converter

Package Information (continued)

TSSOP, 4.0,EXP PADS.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
ACT	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AET	28	D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002"
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0108	B	1/1

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.