



Direct-Conversion Tuner IC for Digital DBS Applications

MAX2104

General Description

The MAX2104 low-cost direct-conversion tuner IC is designed for use in digital direct-broadcast satellite (DBS) television set-top box units. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures. The MAX2104 directly converts L-band signals to baseband signals using a broadband I/Q downconverter. The operating frequency range extends from 925MHz to 2175MHz.

The IC includes an LNA gain control, I and Q downconverting mixers, lowpass filters with gain control and frequency control, a local oscillator (LO) buffer with a 90° quadrature network, and a charge-pump based PLL for frequency control. The MAX2104 also has an on-chip LO, requiring only an external varactor-tuned LC tank for operation. The output of the LO drives the internal quadrature generator and dual modulus prescaler. An on-chip crystal amplifier drives a reference divider as well as a buffer amplifier to drive off-chip circuitry. The MAX2104 is offered in a 48-pin TQFP-EP package.

Applications

- DirecTV, PrimeStar, EchoStar DBS Tuners
- DVB-Compliant DBS Tuners
- Broadband Systems
- LMDS

Features

- ◆ Low-Cost Architecture
- ◆ Operates from Single 5V Supply
- ◆ 925MHz to 2175MHz Input Frequency Range
- ◆ On-Chip Quadrature Generator, Dual-Modulus Prescaler (/32, /33)
- ◆ On-Chip Crystal Amplifier
- ◆ PLL Mixer with Gain-Controlled Charge Pump
- ◆ Input Levels: -25dBm to -65dBm per Carrier
- ◆ Over 40dB Gain Control Range
- ◆ Noise Figure = 11.5dB; IIP3 = 7dBm (at 1550MHz)
- ◆ Automatic Baseband Offset Correction
- ◆ Loophrough Replaces External Splitter
- ◆ Crystal Output Buffer

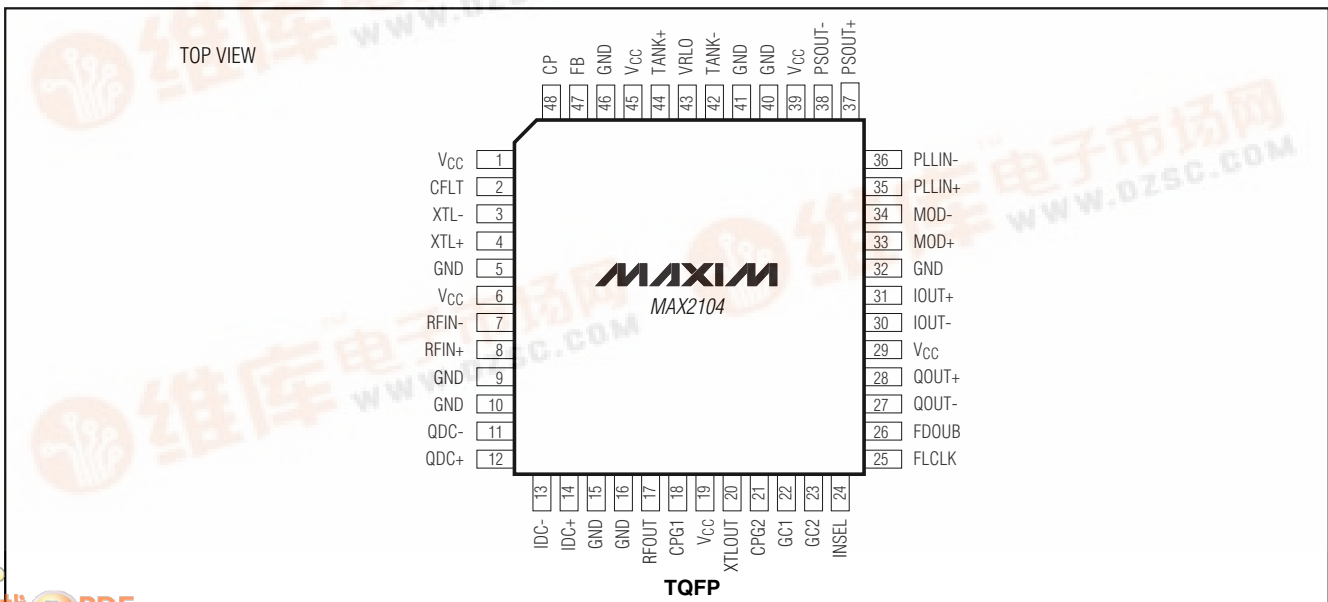
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2104CCM*	0°C to +70°C	48 TQFP-EP

*Contact factory for availability.

Functional Diagram appears at end of data sheet.

Pin Configuration



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ABSOLUTE MAXIMUM RATINGS

V _{CC} to GND	-0.5V to +7V
All Other Pins to GND	-0.3V to (V _{CC} + 0.3V)
RF1+ to RF1-, RF2+ to RF2-, TANK+ to TANK-, IDC+ to IDC-, QDC+ to QDC-	±2V
IOU _T -, QOU _T - to GND Short-Circuit Duration	10s
PSOU _T +, PSOU _T - to GND Short-Circuit Duration	10s
Continuous Current (any pin)	20mA

Continuous Power Dissipation (T _A = +70°C) (derate 27mW/°C above +70°C)	1.5W
Operating Temperature Range	0°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, V_{FB} = 2.4V, C_{IOU_T} = C_{QOU_T} = 10pF, f_{FLCLK} = 2MHz, RF_{IN} = floating, RI_{OU_T} = RQ_{OU_T} = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V _{CC}		4.75		5.25	V
Operating Supply Current	I _{CC}			190	275	mA
STANDARD DIGITAL INPUTS (FDOUB, INSEL, CPG1, CPG2)						
Digital Input Voltage High	V _{IH}		2.4			V
Digital Input Voltage Low	V _{IL}				0.5	V
Digital Input Current	I _{IN}		-15		+10	μA
SLEW-RATE-LIMITED DIGITAL INPUTS						
FLCLK Input Voltage High			1.85			V
FLCLK Input Voltage Low					1.45	V
FLCLK Input Current (Note 1)		R _{SOURCE} = 50kΩ, V _{FLCLK} = 1.65V	-1		+1	μA
DIFFERENTIAL DIGITAL INPUTS (MOD+, MOD-, PLLIN+, PLLIN-)						
Common-Mode Input Voltage	V _{CM1}		1.08	1.2	1.32	V
Input Voltage Low (Note 2)		Referenced to V _{CM1}			-100	mV
Input Voltage High (Note 2)		Referenced to V _{CM1}	100			mV
Input Current (Note 1)			-5		5	μA
DIFFERENTIAL DIGITAL OUTPUTS (PSOUT+, PSOUT-)						
Common-Mode Output Voltage	V _{CMO}		2.16	2.4	2.64	V
Output Voltage Low (Note 3)		Referenced to V _{CMO}		-215	-150	mV
Output Voltage High (Note 3)		Referenced to V _{CMO}	150	215		mV
FREQUENCY SYNTHESIZER						
Prescaler Ratio		(V _{MOD+} - V _{MOD-}) = 200mV	32		32	
		(V _{MOD+} - V _{MOD-}) = -200mV	33		33	
Reference Divider Ratio			8		8	
Charge-Pump Output High Measured at FB		V _{CPG1} = V _{CPG2} = 0.5V	0.08	0.1	0.12	mA
		V _{CPG1} = 0.5V, V _{CPG2} = 2.4V	0.24	0.3	0.36	
		V _{CPG1} = 2.4V, V _{CPG2} = 0.5V	0.48	0.6	0.72	
		V _{CPG1} = V _{CPG2} = 2.4V	1.44	1.8	2.16	

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DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, V_{FB} = 2.4V, C_{IOUT_} = C_{QOUT_} = 10pF, f_{FLCLK} = 2MHz, R_{FIN_} = floating, R_{IOUT_} = R_{QOUT_} = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge-Pump Output Low Measured at FB		V _{CPG1} = V _{CPG2} = 0.5V	-0.12	-0.1	-0.08	mA
		V _{CPG1} = 0.5V, V _{CPG2} = 2.4V	-0.36	-0.3	-0.24	
		V _{CPG1} = 2.4V, V _{CPG2} = 0.5V	-0.72	-0.6	-0.48	
		V _{CPG1} = V _{CPG2} = 2.4V	-2.16	-1.8	-1.44	
Charge-Pump Output Current Matching Positive to Negative		Measured at FB	-5		5	%
Charge-Pump Output Leakage		Measured at FB	-25		25	nA
Charge-Pump Output Current Drive (Note 1)		Measured at CP	100			μA
ANALOG CONTROL INPUTS (GC_)						
Analog Control Input Current	I _{GC_}	V _{GC_} = 1V to 4V	-50		+50	μA
BASEBAND OUTPUTS (IOUT+, IOUT-, QOUT+, QOUT-)						
Differential Output Voltage Swing		R _L = 2kΩ differential	1			V _{P-P}
Common-Mode Output Voltage (Note 1)			0.65		0.85	V
Offset Voltage (Note 1)			-50		+50	mV

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75V to 5.25V, V_{IOUT_} = V_{QOUT_} = 0.59V_{P-P}, C_{IOUT_} = C_{QOUT_} = 10pF, f_{FLCLK} = 2MHz, R_{IOUT_} = R_{QOUT_} = 10kΩ, V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
RF FRONT END							
R _{FIN_} Input Frequency Range	f _{RFIN}		925		2175	MHz	
R _{FIN_} Input Power for 0.59V _{P-P} Baseband Levels		Single carrier	V _{GC1} = V _{GC2} = +4V (min gain)		-20	dBm	
			V _{GC1} = V _{GC2} = +1V (max gain)		-68 -65		
R _{FIN_} Input Third-Order Intercept (Note 4)	IP _{3RFIN_}	PR _{FIN_} = -25dBm per tone	f _{LO} = 2175MHz	5		dBm	
			f _{LO} = 1550MHz	7			
			f _{LO} = 950MHz	8			
R _{FIN_} Input Second-Order Intercept (Note 5)	IP _{2RFIN_}	PR _{FIN_} = -25dBm per tone, f _{LO} = 951MHz		15.5		dBm	
Output-Referred 1dB Compression Point (Note 6)	P _{1dBOUT_}	PR _{FIN_} = -40dBm, signals within filter bandwidth		2		dBV	
Noise Figure	NF	PR _{FIN_} = -65dBm, f _{RFIN_} = 1550MHz, V _{GC1} = 1V, V _{GC2} adjusted 0.59V _{P-P} baseband level		11.5		dB	
R _{FIN_} Return Loss (Note 7)		f _{RFIN_} = 925MHz	10		dB		
		f _{RFIN_} = 2175MHz	10				
LO 2nd Harmonic Rejection (Note 8)		Average level of V _{IOUT_} , V _{QOUT_}	27			dBc	
LO Half Harmonic Rejection (Note 9)		Average level of V _{IOUT_} , V _{QOUT_}	31	38			dBc

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AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75V to 5.25V, V_{IOUT_} = V_{QOUT_} = 0.59V_{P-P}, C_{IOUT_} = C_{QOUT_} = 10pF, f_{FLCLK} = 2MHz, R_{IOUT_} = R_{QOUT_} = 10k Ω , V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V, V_{PLLIN+} = V_{MOD+} = 1.3V, V_{PLLIN-} = V_{MOD-} = 1.1V, T_A = +25°C. Typical values are at V_{CC} = 5.0V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LO Leakage Power (Notes 7, 10)		Measured at RFIN_		-66		dBm
RFOUT PORT (LOOPTHROUGH)						
RFIN_ to RFOUT Gain (Note 11)		f = 925MHz		0.5		dB
		f = 1550MHz		1.8		
		f = 2175MHz		2.5		
RFOUT Output Third-Order Intercept Point (Note 11)		f = 925MHz		9		dBm
		f = 1550MHz		7		
		f = 2175MHz		4		
RFOUT Noise Figure (Note 11)		f = 925MHz		15		dB
		f = 1550MHz		12		
		f = 2175MHz		11.5		
RFOUT Return Loss (Notes 1, 11)		925MHz < f < 2175MHz			8	dB
BASEBAND CIRCUITS						
Output Real Impedance (Note 1)		IOUT_, QOUT_			50	Ω
Baseband Highpass Frequency (Note 1)		C _{IDC_} = C _{QDC_} = 0.22 μ F			750	Hz
LPF -3dB Cutoff-Frequency Range (Note 1)		Controlled by FLCLK signal	8		33	MHz
Baseband Frequency Response (Note 1)		Deviation from ideal 7th order, Butterworth, up to 0.7 x f _C	-0.5		+0.5	dB
LPF -3dB Cutoff-Frequency Accuracy (Note 1)		f _{FLCLK} = 0.5MHz, f _C = 8MHz	-5.5		+5.5	%
		f _{FLCLK} = 1.25MHz, f _C = 19.3MHz	-10		+10	
		f _{FLCLK} = 2.0625MHz, f _C = 31.4MHz	-10		+10	
Ratio of In-Filter-Band to Out-of-Filter-Band Noise		f _{IN_BAND} = 100Hz to 22.5MHz, f _{OUT_BAND} = 67.5MHz to 112.5MHz		19		dB
Quadrature Gain Error		Includes effects from baseband filters, measured at 125kHz baseband			1.2	dB
Quadrature Phase Error		Includes effects from baseband filters, measured at 125kHz baseband			4	degrees

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AC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 4.75V$ to $5.25V$, $V_{IOUT_} = V_{QOUT_} = 0.59V_{P-P}$, $C_{IOUT_} = C_{QOUT_} = 10pF$, $f_{FLCLK} = 2MHz$, $R_{IOUT_} = R_{QOUT_} = 10k\Omega$, $V_{FDOUB} = V_{INSEL} = V_{CPG1} = V_{CPG2} = 2.4V$, $V_{PLLIN+} = V_{MOD+} = 1.3V$, $V_{PLLIN-} = V_{MOD-} = 1.1V$, $T_A = +25^{\circ}C$. Typical values are at $V_{CC} = 5.0V$ and $T_A = +25^{\circ}C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYNTHESIZER						
XTLOUT Output Voltage Swing		Load = 10pF 10kΩ, $f_{XTLOUT} = 6MHz$	0.75	1	1.5	V_{P-P}
XTLOUT Output Voltage DC				2		V
Crystal Frequency Range (Note 1)			4		7.26	MHz
MOD+, MOD- Setup Time (Note 1)	t_{SUM}	Figure 1	7			ns
MOD+, MOD- Hold Time (Note 1)	t_{HM}	Figure 1	0			ns
LOCAL OSCILLATOR						
LO Tuning Range (Note 1)			590		1180	MHz
LO Phase Noise (Notes 7, 12)		At 1kHz offset, $f_{LO} = 2175MHz$		-55		dBc/Hz
		At 10kHz offset, $f_{LO} = 2175MHz$		-75		
		At 100kHz offset, $f_{LO} = 2175MHz$		-95		
RFIN_ to LO Input Isolation (Note 10)		$f_{RFIN_} = 2150MHz$		57		dB

Note 1: Minimum and maximum values are guaranteed by design and characterization over supply voltage.

Note 2: With external 100Ω termination resistor.

Note 3: Driving differential load of 10kΩ || 15pF.

Note 4: Two signals are applied to RFIN_ at $f_{LO} - 100MHz$ and $f_{LO} - 199MHz$. $V_{GC2} = 1V$; V_{GC1} is set such that the baseband outputs are at 590mV_{P-P}. IM products are measured at baseband outputs but are referred to RF inputs.

Note 5: Two signals are applied to RFIN_ at 1200MHz and 2150MHz. $V_{GC2} = 1V$, V_{GC1} is set such that the baseband outputs are at 590mV_{P-P}. IM products are measured at baseband outputs but are referred to RF inputs.

Note 6: $P_{RFIN_} = -40dBm$ so that front end IM contributions are minimized.

Note 7: Using L64733/L64734 demo board from LSI Logic.

Note 8: Downconverted level, in dBc, of carrier present at $f_{LO} \times 2$, $f_{LO} = 1180MHz$, $f_{VCO} = 590MHz$, $V_{FDOUB} = 2.4V$.

Note 9: Downconverted level, in dBc, of carrier present at $f_O / 2$, $f_{LO} = 2175MHz$, $f_{VCO} = 1087.5MHz$, $V_{FDOUB} = 2.4V$.

Note 10: Leakage is dominated by board parasitics.

Note 11: $V_{CPG1} = V_{CPG2} = V_{FDOUB} = V_{INSEL} = 0.5V$, $f_{FLCLK} = 0.5MHz$.

Note 12: Measured at tuned frequency with PLL locked. All phase noise measurements assume tank components have a $Q > 50$.

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Pin Description

PIN	NAME	FUNCTION
1, 6, 19, 29, 39, 45	V _{CC}	V _{CC} Power-Supply Input. Connect each pin to a +5V ±5% low-noise supply. Bypass each V _{CC} pin to the nearest GND with a ceramic chip capacitor.
2	CFLT	External Bypass for Internal Bias. Bypass this pin with a 0.1µF ceramic chip capacitor to GND.
3	XTL-	Inverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.
4	XTL+	Noninverting Input to Crystal Oscillator. Consult crystal manufacturer for circuit loading requirements.
5, 9, 10, 15, 16, 32, 40, 41, 46	GND	Ground. Connect each of these pins to a solid ground plane. Use multiple vias to reduce inductance where possible.
7	RFIN-	RF Inverting Input. Bypass RFIN- with 47pF capacitor in series with a 75Ω resistor to GND.
8	RFIN+	RF Noninverting Input. Connect to 75Ω source with a 47pF ceramic chip capacitor.
11	QDC-	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from QDC- to QDC+ (pin 12).
12	QDC+	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from QDC+ to QDC- (pin 11).
13	IDC-	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from IDC- to IDC+ (pin 14).
14	IDC+	Baseband Offset Correction. Connect a 0.22µF ceramic chip capacitor from IDC+ to IDC- (pin 13).
17	RFOUT	Buffered RF Output. Enabled when INSEL is low.
18	CPG1	Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See the <i>DC Electrical Characteristics</i> section for available gain settings.
20	XTLOUT	Buffered Crystal Oscillator Output
21	CPG2	Charge-Pump Gain Select. High-impedance digital input. Sets the charge-pump output scaling. See the <i>DC Electrical Characteristics</i> section for available gain settings.
22	GC1	Gain Control Input for RF Front End. High-impedance analog input, with an input range of 1V to 4V. See the <i>AC Electrical Characteristics</i> section for transfer function.
23	GC2	Gain Control Input for Baseband Signals. High-impedance analog input, with an input range of 1V to 4V. See the <i>AC Electrical Characteristics</i> section for transfer function.
24	INSEL	Loophrough Mode Enable. High-impedance digital input. Drive low to enable the RFOUT buffer and disable the internal downconverters. Connect to V _{CC} for normal tuner operation.
25	FLCLK	Baseband Filter Cutoff Adjust. Connect to a slew-rate-limited clock source. See the <i>AC Electrical Characteristics</i> section for transfer function.
26	FDOUB	LO Frequency Doubler. High-impedance digital input. Drive high to enable the LO frequency doubler. Drive low to disable the doubling function.
27	QOUT-	Baseband Quadrature Output. Connect to inverting input of high-speed ADC.
28	QOUT+	Baseband Quadrature Output. Connect to noninverting input of high-speed ADC.
30	IOUT-	Baseband In-Phase Output. Connect to inverting input of high-speed ADC.
31	IOUT+	Baseband In-Phase Output. Connect to noninverting input of high-speed ADC.
33	MOD+	PECL Modulus Control. A PECL high on MOD+ sets the dual-modulus prescaler to divide by 32. A PECL logic low sets the divide ratio to 33. Drive with a differential PECL signal with MOD- (pin 34).

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Pin Description (continued)

PIN	NAME	FUNCTION
34	MOD-	PECL Modulus Control. A PECL low on MOD- sets the dual-modulus prescaler to divide by 32. A PECL logic high sets the divide ratio to 33. Drive with a differential PECL signal with MOD+ (pin 33).
35	PLLIN+	PECL Phase-Locked Loop Input. Drive with a differential PECL signal with PLLIN- (pin 36).
36	PLLIN-	PECL Phase-Locked Loop Input. Drive with a differential PECL signal with PLLIN+ (pin 35).
37	PSOUT+	PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used with PSOUT- (pin 38). Requires PECL-compatible termination.
38	PSOUT-	PECL Prescaler Output. Differential output of the dual-modulus prescaler. Used with PSOUT+ (pin 37). Requires PECL-compatible termination.
42	TANK-	LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.
43	VRLO	LO Internal Regulator. Bypass with a 100pF ceramic chip capacitor to GND.
44	TANK+	LO Tank Oscillator Input. Connect to an external LC tank with varactor tuning.
47	FB	Feedback Output. Control of external charge-pump transistor.
48	CP	Voltage Drive Output. Control of external charge-pump transistor.

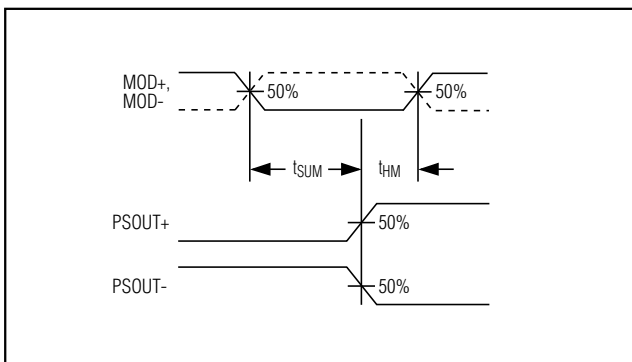
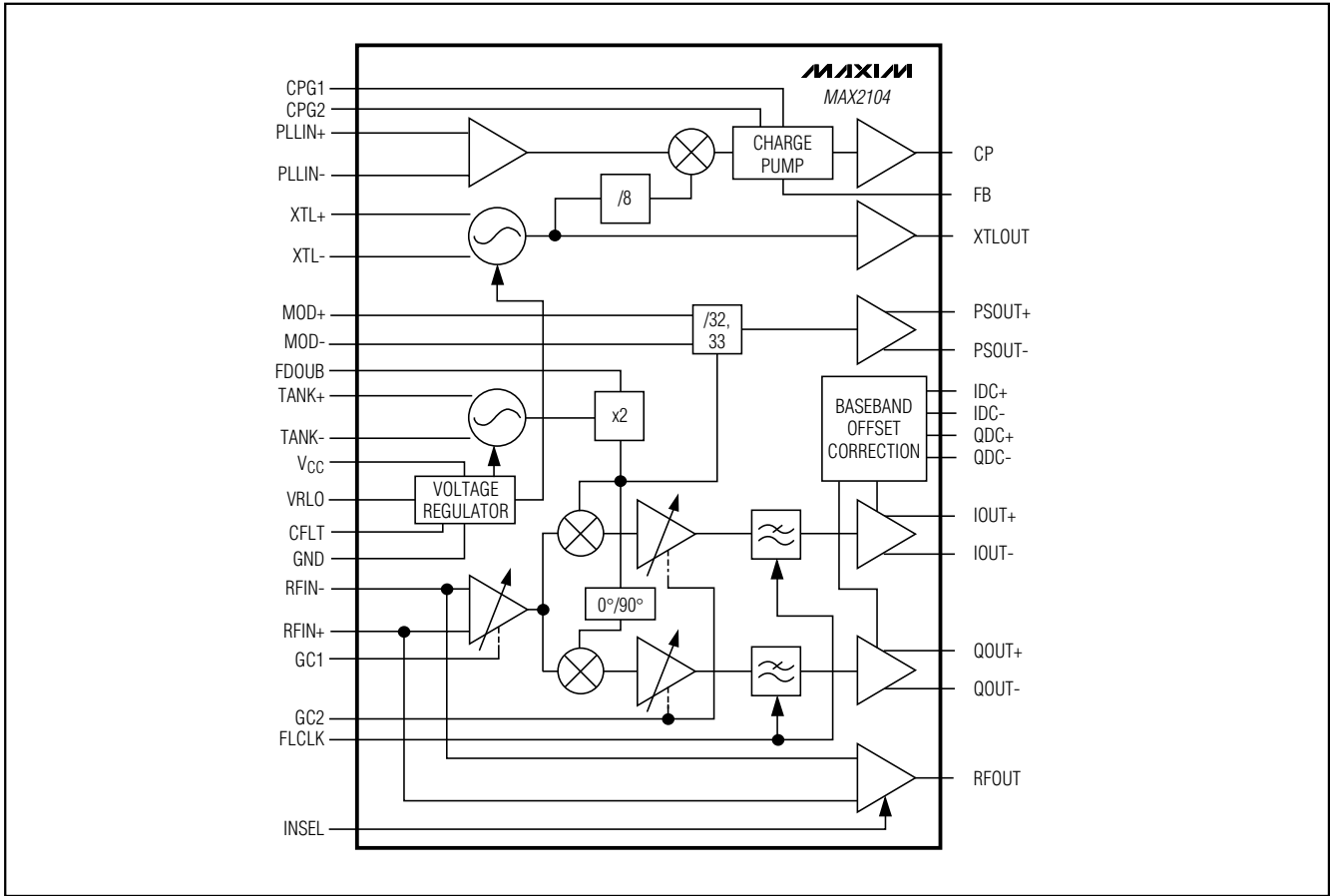


Figure 1. Timing Diagram

Direct-Conversion Tuner IC for Digital DBS Applications

Functional Diagram

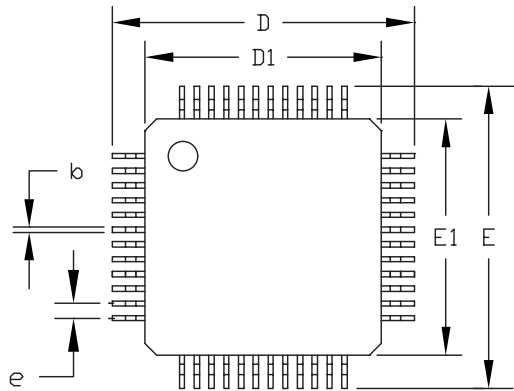


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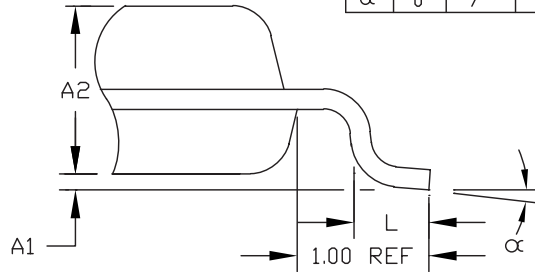
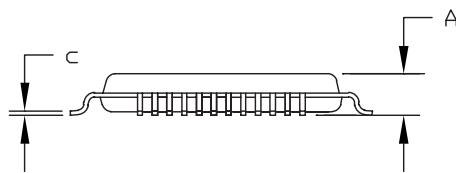
Package Information

MAX2104

32L/48L_TQFP.EPS



	JEDEC VARIATION			
	BC		BE	
	32 LEAD	48 LEAD	32 LEAD	48 LEAD
	MIN.	MAX.	MIN.	MAX.
A	---	1.60	---	1.60
A ₁	0.05	0.15	0.05	0.15
A ₂	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10
D ₁	7.00	BSC.	7.00	BSC.
E	8.90	9.10	8.90	9.10
E ₁	7.00	BSC.	7.00	BSC.
e	0.8	BSC.	0.5	BSC.
L	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27
c	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°



NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MD-136, VARIATIONS BC AND BE.
4. LEADS SHALL BE COPLANAR WITHIN .004 INCH.

MAXIM		
<small>PROPRIETARY INFORMATION</small>		
TITLE: PACKAGE OUTLINE, 32/48L, 7x7x1.4 MM TQFP		
APPROVAL	DOCUMENT CONTROL NO. 21-0054	REV D 1/1

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