19-3386; Rev 0; 8/04

MAXIM

Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

General Description

The MAX3746 multirate limiting amplifier functions as a data quantizer for SONET, Fibre-Channel, and Gigabit Ethernet optical receivers. The amplifier accepts a wide range of input voltages and provides selectable-level, current-mode logic (CML) output voltages with controlled edge speeds. A received-signal-strength indicator (RSSI) is available when the MAX3746 is DC-coupled to the MAX3744/MAX3724 SFP transimpedance amplifier (TIA). A receiver consisting of the MAX3744/MAX3724 and the MAX3746 can provide up to 19dB RSSI dynamic range. Additional features include a programmable loss-of-signal (LOS) detect, an optional disable function (DISABLE), and an output-signal polarity reversal (OUTPOL). Output disable can be used to implement squelch.

The combination of the MAX3746 and the MAX3744/MAX3724 allows for the implementation of all the small-form-factor SFF-8472 digital diagnostic specifications using a standard 4-pin TO-46 header.

The MAX3746 is pin-for-pin compatible with the MAX3748A limiting amplifier and consumes 30% less power. The MAX3746 is packaged in a 3mm x 3mm, 16-pin QFN package.

Applications

Gigabit Ethernet SFF/SFP Transceiver Modules

Fibre-Channel SFF/SFP Transceiver Modules

Multirate OC-12 to OC48-FEC SFF/SFP Transceiver Modules

Features

- ♦ SFP Reference Design Available
- ♦ Low 115mW Power Consumption
- ♦ 16-Pin QFN Package with 3mm x 3mm Footprint
- ♦ 70ps Rise and Fall Time
- ♦ Loss-of-Signal with Programmable Threshold
- ♦ RSSI Interface (with MAX3744/MAX3724 TIA)
- ♦ Output Disable
- ♦ Polarity Select
- ♦ 8.4ps$_{P-P}$ Deterministic Jitter (3.2Gbps)
- ♦ Improved EMI Performance
- ♦ Selectable CML Output levels
- ♦ Pin Compatible with MAX3748A

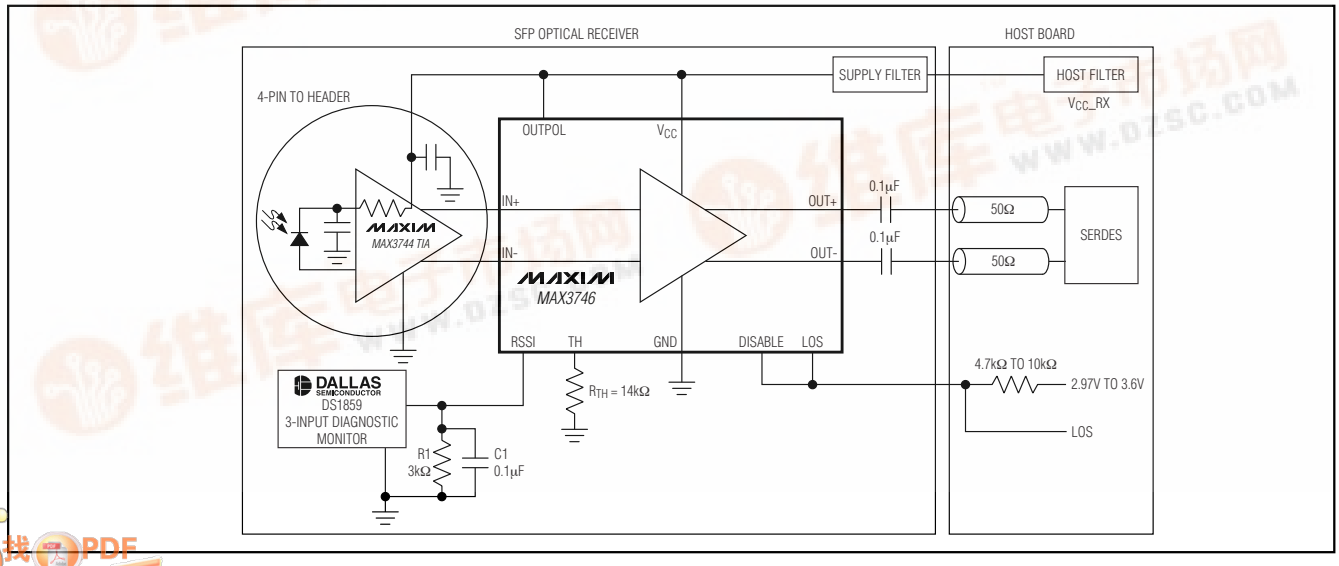
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX3746ETE	-40°C to +85°C	16 QFN	T1633F-3

Pin Configuration appears at end of data sheet.

Typical Operating Circuits continued at end of data sheet.

Typical Operating Circuits



Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC}) .....-0.5V to +4.5V
Voltage at IN+, IN- .....(V_{CC} - 2.4V) to (V_{CC} + 0.5V)
Voltage at DISABLE, OUTPOL, RSSI, LOS, TH .....-0.5V to (V_{CC} + 0.5V)
Current into LOS.....1mA to +9mA
Differential Input Voltage (IN+ - IN-) 2.5V
Continuous Current at CML Outputs (OUT+, OUT-) .....-25mA to +25mA
Continuous Power Dissipation (T_A = + 70°C)
16-Pin QFN (derate 17.7mW above +70°C) 1.4W
Operating Junction Temperature Range (T_J)....-55°C to +150°C
Storage Ambient Temperature Range (Ts) .....-55°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, CML output load is 50Ω to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified. The data input transition time is controlled by 4th-order Bessel filter with f_{-3dB} = 0.75 x 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 x 3.2GHz for a data rate of 3.2Gbps.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Single-Ended Input Resistance	R_{IN}	Single ended to V_{CC}	42	50	58	Ω
Input Return Loss	se S_{11}	Single ended, f < 3GHz, DUT is powered on		14		dB
	diff S_{11}	Differential, f < 3GHz, DUT is powered on		15		
Input Sensitivity	V_{IN-MIN}	(Note 1)		2	4	mV_{P-P}
Input Overload	V_{IN-MAX}	(Note 1)	1200			mV_{P-P}
Single-Ended Output Resistance	R_{OUT}	Single ended to V_{CC}	42	50	58	Ω
Output Return Loss	diff S_{22}	Differential, f < 3GHz, DUT is powered on		20		dB
CML Differential Output Voltage		$4mV_{P-P} < V_{IN} < 1200mV_{P-P}$, OUTPOL connected to V_{CC} or GND	600	800	1000	mV_{P-P}
		$4mV_{P-P} < V_{IN} < 1200mV_{P-P}$, OUTPOL open or connected to 30kΩ	400	500	600	
Differential Output Signal when Disabled		Outputs AC-coupled, V_{IN-MAX} applied to input (Note 2)			10	mV_{P-P}
Deterministic Jitter (Note 3)	DJ	K28.5 pattern at 3.2Gbps (Note 2)		8.4	18	ps_{P-P}
		K28.5 pattern at 3.2Gbps at T_A = +100°C		10.2		
		2^{23} - 1 PRBS equivalent at 2.7Gbps (Note 2)		11.6	23	
		2^{23} - 1 PRBS equivalent pattern at 2.7Gbps at T_A = +100°C		13.1		
		K28.5 pattern at 2.1Gbps		8	20	
		K28.5 pattern at 2.1Gbps at T_A = +100°C		9.7		
		2^{23} - 1 PRBS equivalent pattern at 622Mbps (Note 2)		42.5	69	
		2^{23} - 1 PRBS equivalent pattern at 622Mbps at T_A = +100°C		47.8		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, CML output load is 50Ω to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise specified. The data input transition time is controlled by 4th-order Bessel filter with f_{-3dB} = 0.75 x 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 x 3.2GHz for a data rate of 3.2Gbps.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Random Jitter		Input = 4mV$_{P-P}$ (Notes 2, 4)		3	7	ps$_{RMS}$
Data Output Transition Time		4mV$_{P-P}$ < V$_{INP-P}$ < 1200mV$_{P-P}$, 20% to 80% (Note 2)		70	114	ps
Input-ReferredNoise		(Note 2)			150	µV$_{RMS}$
Low-Frequency Cutoff				20		kHz
Power-Supply Current	I_{CC}	Includes the CML output current; OUTPOL connected to V_{CC} or GND		35	41.5	mA
		Includes the CML output current; OUTPOL open or connected to 30kΩ to GND		29	35	
		Excludes the CML output current and the CM_RSSI circuitry; OUTPOL connected to V_{CC} or GND (Note 5)		20	25	
Power-Supply Noise Rejection	PSNR	f < 2MHz		40		dB
LOSS-OF-SIGNAL (Notes 2, 6)						
LOS Hysteresis		10 log ($V_{DEASSERT}$ / V_{ASSERT})	1.25	2.2		dB
LOS Assert/Deassert Time		(Note 7)	2.3		50	µs
Low LOS Assert Level		R_{TH} = 2kΩ	2.6	4	6.4	mV$_{P-P}$
Low LOS Deassert Level		R_{TH} = 2kΩ		6	9.6	mV$_{P-P}$
Medium LOS Assert Level		R_{TH} = 14kΩ	19.6	28	31.8	mV$_{P-P}$
Medium LOS Deassert Level		R_{TH} = 14kΩ		42	54.7	mV$_{P-P}$
High LOS Assert Level		R_{TH} = 25kΩ	36	50	54.3	mV$_{P-P}$
High LOS Deassert Level		R_{TH} = 25kΩ		84	114	mV$_{P-P}$
CM_RSSI SPECIFICATION						
RSSI Current Gain	A_{RSSI}	I_{RSSI} / I_{CM_RSSI} (Note 8)		0.031		
V_{CM} to I_{RSSI} 3dB Bandwidth				40		kHz
Input-Referred RSSI Current Stability	$\frac{I_{RSSI}}{A_{RSSI}}$	Input < 6.6mA, 0V ≤ V_{RSSI} ≤ 2.5V (Note 9)	-40		+36	µA
RSSI Output Compliance Voltage	V_{RSSI}		0		2.0	V
TTL/CMOS I/O						
LOS Output High Voltage	V_{OH}	R_{LOS} = 4.7kΩ to 10kΩ to Vcc_host (3V)	2.4			V
LOS Output Low Voltage	V_{OL}	R_{LOS} = 4.7kΩ to 10kΩ to Vcc_host (3.6V)			0.4	V

Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, CML output load is 50Ω to V_{CC}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C, unless otherwise specified. The data input transition time is controlled by 4th-order Bessel filter with f_{-3dB} = 0.75 x 2.667GHz for all data rates of 2.667Gbps and below, and with f_{-3dB} = 0.75 x 3.2GHz for a data rate of 3.2Gbps.)

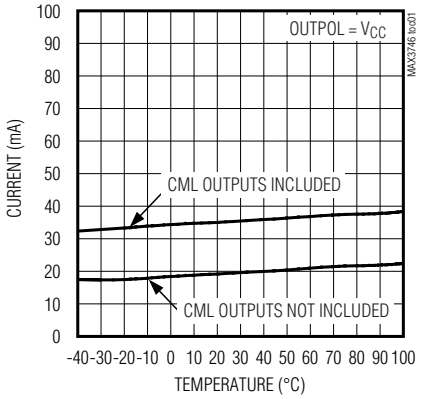
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DISABLE Input High	V_{IH}		2.0			V
DISABLE Input Low	V_{IL}				0.8	V
DISABLE Input Current		R_{LOS} = 4.7kΩ to 10kΩ to Vcc_host			10	µA

Note 1: Between sensitivity and overload, all AC specifications are met.
Note 2: Guaranteed by design and characterization.
Note 3: The deterministic jitter caused by the filter is not included in the DJ generation specification.
Note 4: Random jitter was measured without using a filter at the input.
Note 5: The supply current measurement excludes the CML output currents by connecting the CML outputs to a separate V_{CC}. (See Figure 1.)
Note 6: Hysteresis is calculated as 10 log ($V_{DEASSERT}$ / V_{ASSERT}). Unless otherwise specified, the data rate for all LOS detect specifications varies from 622Mbps up to 3.2Gbps, and the patterns are 1010 or 2^{23} - 1 PRBS.
Note 7: The signal is switched between two amplitudes, Signal_On and Signal _Off as shown in Figure 2.
Note 8: I_{CM_RSSI} is the input common-mode current. I_{RSSI} is the current at the RSSI output.
Note 9: Stability is defined as the variation over temperature and power supply with respect to the typical gain of the part.

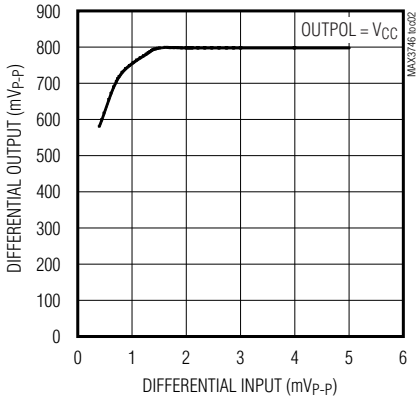
Typical Operating Characteristics

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

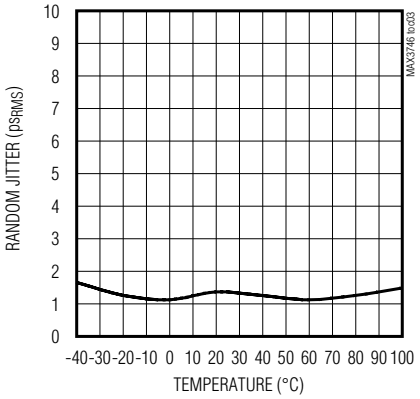
SUPPLY CURRENT vs. TEMPERATURE



TRANSFER FUNCTION



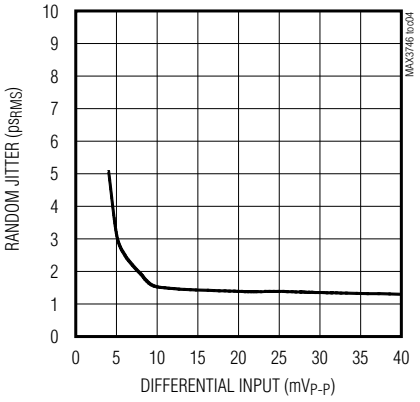
RANDOM JITTER vs. TEMPERATURE (INPUT LEVEL 10mVP-P)



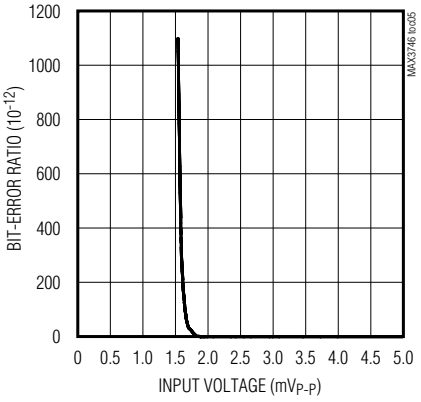
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

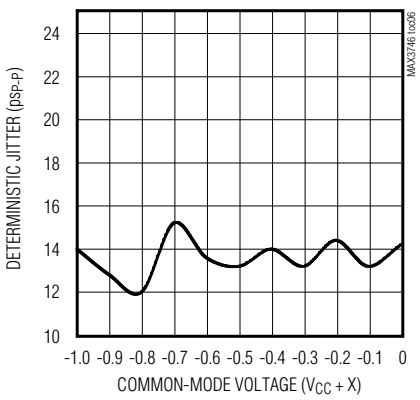
RANDOM JITTER vs. INPUT AMPLITUDE



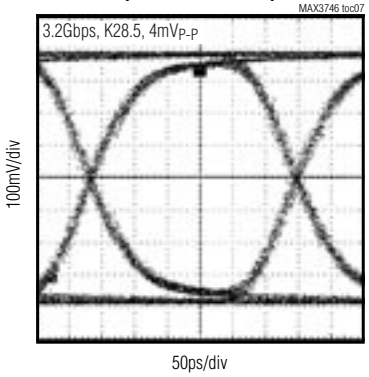
BIT-ERROR RATIO vs. INPUT VOLTAGE



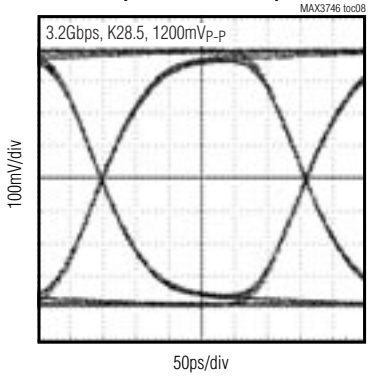
DETERMINISTIC JITTER vs. INPUT COMMON-MODE VOLTAGE (2.7Gbps, K28.5)



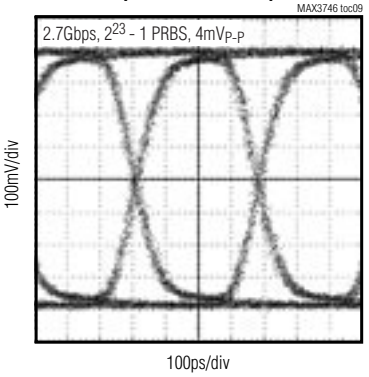
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



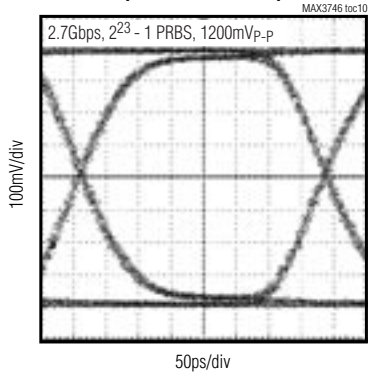
OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



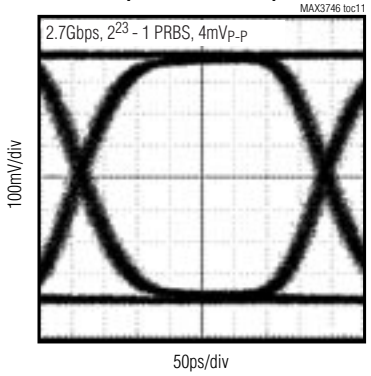
OUTPUT EYE DIAGRAM (MINIMUM INPUT)



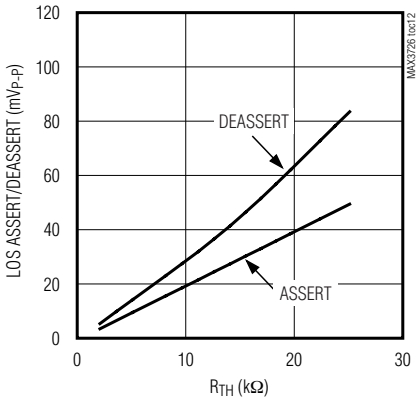
OUTPUT EYE DIAGRAM (MAXIMUM INPUT)



OUTPUT EYE DIAGRAM AT +100°C (MINIMUM INPUT)



ASSERT/DEASSERT LEVELS vs. R_{TH}

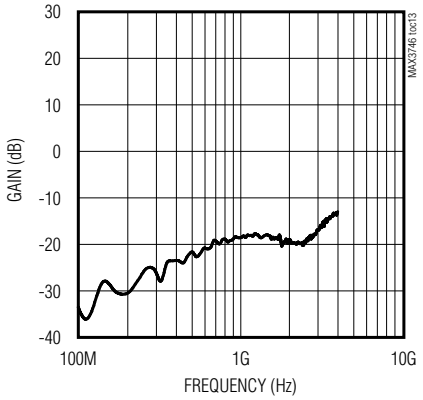


Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

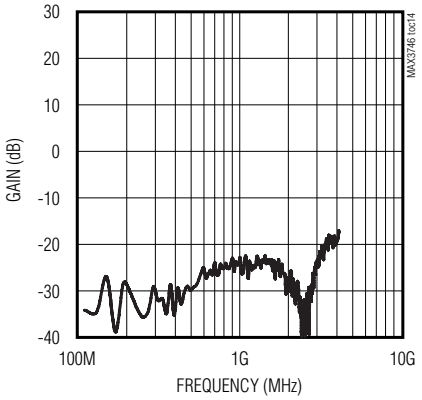
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, T_A = +25°C, unless otherwise noted.)

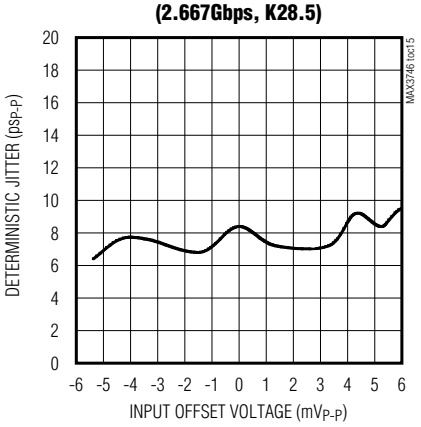
**INPUT RETURN GAIN (SDD11)
(INPUT SIGNAL LEVEL = -50dBm)
(OUTPUT DISABLED)**



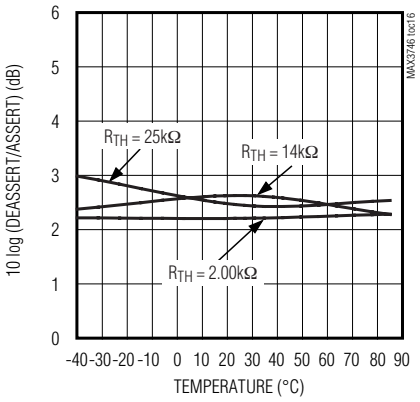
**OUTPUT RETURN GAIN (SDD22)
(INPUT SIGNAL LEVEL = -50dBm)
(WITH INPUT DC OFFSET)**



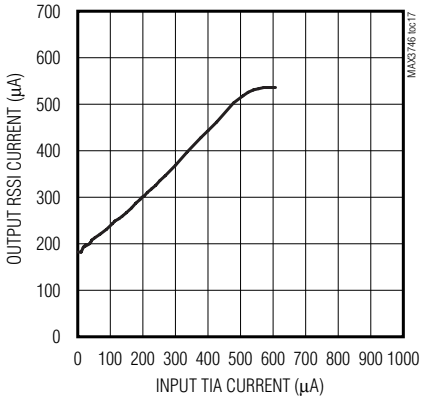
**DETERMINISTIC JITTER
vs. INPUT OFFSET VOLTAGE
(2.667Gbps, K28.5)**



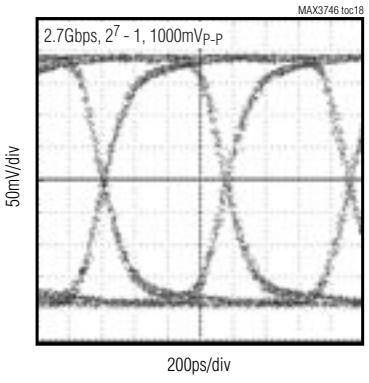
**LOS HYSTERESIS
vs. TEMPERATURE
(2.667Gbps, 2^{23} - 1 PRBS)**



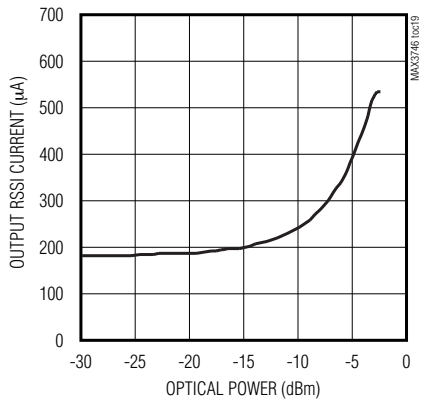
**RSSI CURRENT vs. INPUT TIA CURRENT
(MAX3744 and MAX3746)**



**SINGLE-ENDED
OUTPUT SIGNAL**



**RSSI CURRENT vs. OPTICAL POWER
(MAX3744 and MAX3746)**



Pin Description

PIN	NAME	FUNCTION
1, 4	V_{CC1}	Supply Voltage
2	IN+	Noninverted Input Signal, CML
3	IN-	Inverted Input Signal, CML
5	TH	Loss-of-Signal Threshold Pin. Resistor to ground (R_{TH}) sets the LOS threshold. Connecting this pin to V_{CC} disables the LOS circuitry and reduces power consumption.
6	DISABLE	Disable Input, CMOS/TTL. The data outputs are held static when this pin is asserted high. The LOS function remains active when the outputs are disabled.
7	LOS	Noninverted Loss-of-Signal Output. LOS is asserted high when the signal drops below the assert threshold set by the TH input. The output is open collector.
8, 16	GND	Supply Ground
9	OUTPOL	Output Polarity Control. Connect to GND for an inversion of polarity through the limiting amplifier and connect to V_{CC} for normal operation. See Table 1 for all settings.
10	OUT-	Inverted Data Output, CML
11	OUT+	Noninverted Data Output, CML
12	V_{CC2}	Output Supply
13	RSSI	Received-Signal-Strength Indicator. This current output can be used to obtain a ground-referenced voltage proportional to the photodiode current with the MAX3744 by connecting an external resistor between this pin and GND.
14,15	N.C.	No Connection. Leave open.
EP	EXPOSED PAD	Connect the exposed pad to board ground for optimal electrical and thermal performance.

Detailed Description

The MAX3746 limiting amplifier consists of an input buffer, a multistage amplifier, offset-correction circuitry, an output buffer, power-detection circuitry, and signal-detect circuitry (see the *Functional Diagram*).

Input Buffer

The input buffer is shown in Figure 3. It provides 50Ω termination for each input signal IN+ and IN-. The MAX3746 can be DC- or AC-coupled to a TIA (TIA output offset degrades receiver performance if DC-coupled). The CML input buffer is optimized for the MAX3744/MAX3724 TIA.

Gain Stage

The high-bandwidth multistage amplifier provides approximately 60dB of gain.

Offset Correction Loop

The MAX3746 is susceptible to DC offsets in the signal path because it has high gain. In communication systems using NRZ data with a 50% duty cycle, pulse-width distortion present in the signal, or generated in the transimpedance amplifier, appears as an input offset and is reduced by the offset correction loop.

CML Output Buffer

The MAX3746 limiting amplifier's CML output provides high tolerance to impedance mismatches and inductive connectors. The OUTPOL setting programs the output current. Connecting the DISABLE pin to V_{CC} disables the output. If the LOS pin is connected to the DISABLE pin, the outputs OUT+ and OUT- are at a static voltage (squelch) whenever the input signal level drops below the LOS threshold. The output common mode remains constant when the part is disabled. The output buffer can be AC- or DC-coupled to the load (Figure 4).

Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

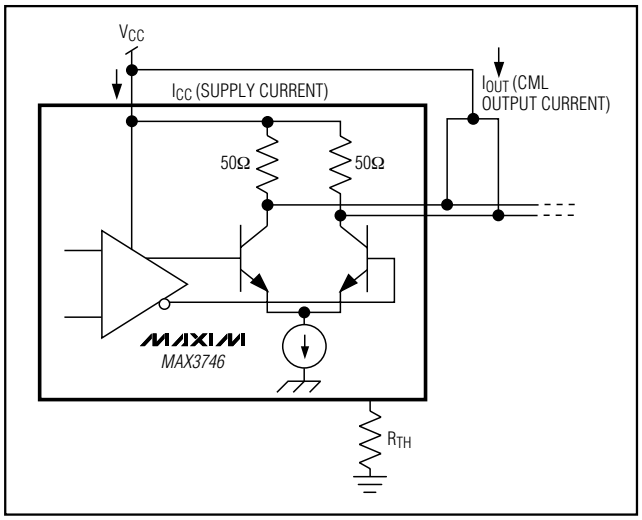


Figure 1. Power-Supply Current Measurement

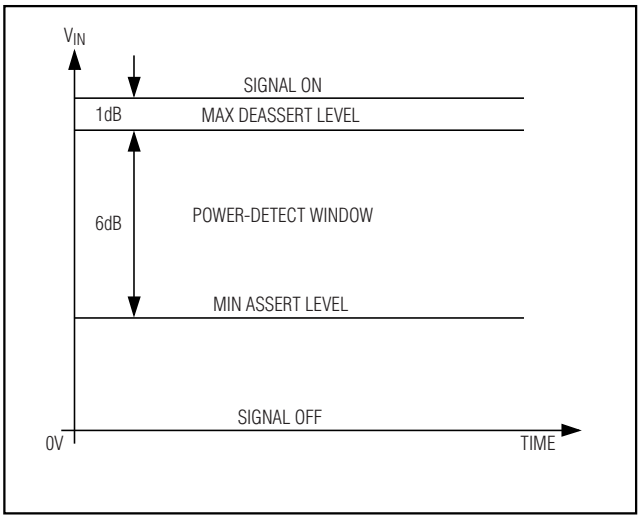


Figure 2. LOS Assert Threshold Set 1dB Below the Minimum by Receiver Sensitivity for Selected R_{TH}

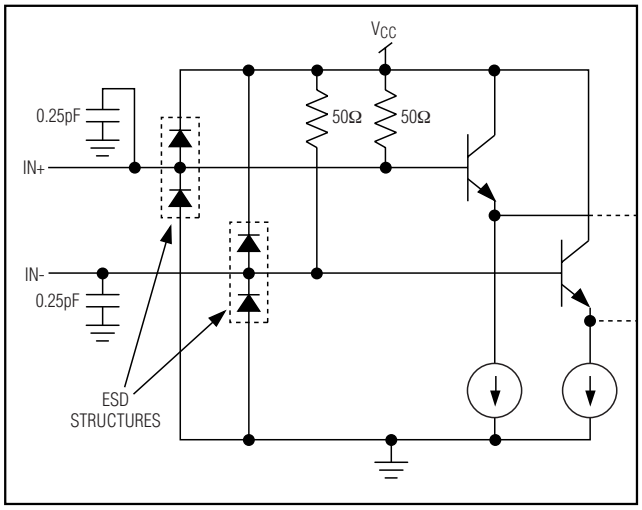


Figure 3. CML Input Buffer

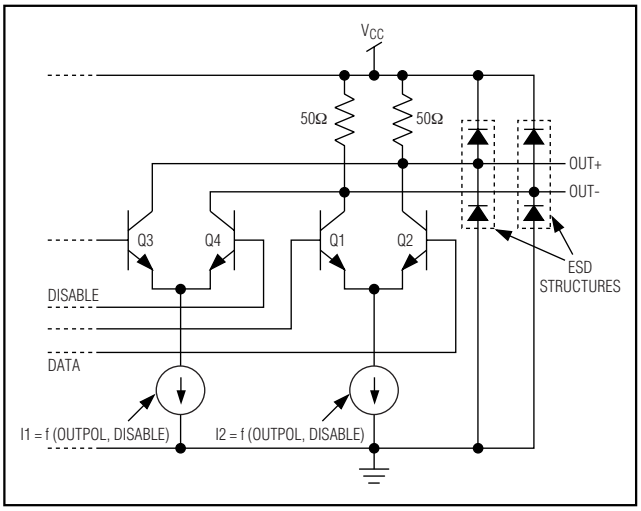


Figure 4. CML Output Buffer

Power Detect and Loss-of-Signal Indicator

The MAX3746 is equipped with multirate LOS circuitry that indicates when the input signal is below a programmable threshold, set by resistor R_{TH} at the TH pin (see the *Typical Operating Characteristics* for appropriate resistor sizing). An averaging RMS power detector compares the input signal amplitude with this threshold and feeds the signal-detect information to the open-collector LOS output.

To prevent LOS chatter in the region of the programmed threshold, approximately 2dB of hysteresis is built into the LOS assert/deassert function. Once asserted, the LOS is not deasserted until the input amplitude rises to the required level ($V_{DEASSERT}$). (See Figures 2 and 5.)

Design Procedure

Program the LOS Assert Threshold

External resistor, R_{TH}, programs the loss-of-signal threshold. See the LOS Threshold vs. R_{TH} graph in the *Typical Operating Characteristics* to select the appropriate resistor.

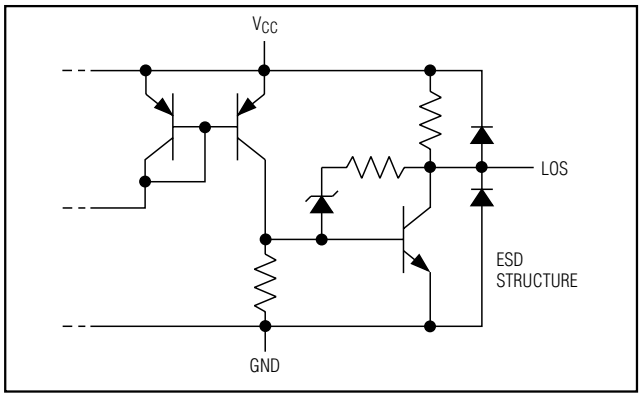


Figure 5. LOS Output Circuit

Select the Coupling Capacitor

When AC coupling is desired, coupling capacitors C_{IN} and C_{OUT} should be selected to minimize the receiver's deterministic jitter. Jitter is decreased as the input low-frequency cutoff (f_{IN}) is decreased.

$$f_{IN} = 1 / [2\pi(50)(C_{IN})]$$

For ATM/SONET or other applications using scrambled NRZ data, select (C_{IN}, C_{OUT}) ≥ 0.1µF, which provides f_{IN} < 32kHz. For Fibre Channel, Gigabit Ethernet, or other applications using 8B/10B data coding, select (C_{IN}, C_{OUT}) ≥ 0.01µF, which provides f_{IN} < 320kHz. Refer to Application Note HFAN-1.1, *Choosing AC-Coupling Capacitors*.

RSSI Implementation

The SFF-8472 Digital Diagnostic specification requires monitoring of input receive power. The MAX3746 and MAX3744 receiver chipset allows for the monitoring of the average receive power by measuring the average DC current of the photodiode.

The MAX3744/MAX3724 preamp measures the average photodiode current and provides the information to the output common mode. The MAX3746 RSSI detect block senses the common-mode DC level of input signals. IN+ and IN- provide a ground-referenced output signal (RSSI) proportional to the photodiode current. The advantage of this implementation is that it allows the TIA to be packaged in a low-cost, conventional 4-pin TO-46 header.

The MAX3746 RSSI output is connected to an analog input channel of the DS1858/DS1859 SFP controller to convert the analog information into a 16-bit word. The DS1858/DS1859 provide the receive-power information to the host board of the optical receiver through a 2-wire interface. The DS1859 allows for internal calibration of the receive power monitor.

The MAX3744/MAX3724 and the MAX3746 have been optimized to achieve RSSI stability of 2.5dB within the 6µA to 500µA range of average input photodiode current. To achieve the best accuracy, MAXIM recommends receive-power calibration at the low end (6µA) and the high end (500µA) of the required range. See the RSSI Current Gain graph in the *Typical Operating Characteristics*.

Connecting to the Dallas DS1858/DS1859

For best use of the RSSI monitor, capacitor C1 and resistor R1 shown in the first *Typical Application Circuit* need to be placed as close as possible to the Dallas diagnostic monitor with the ground of C1 and R1 the same as the DS1858/DS1859 ground. Capacitor C1 suppresses system noise on the RSSI signal. R1 = 3kΩ and C1 = 0.1µF is recommended.

EMI Performance

The MAX3746 has been designed for better EMI performance. To help reduce EMI, special care has been taken to produce symmetrical signal outputs. See the eye diagram of the single-ended output in the *Typical Operating Characteristics*.

Table 1. Logic Table for Polarity and CML Output-Level Settings

OUTPOL	DESCRIPTION
V_{CC}	Noninverting output with full CML output level
Open	Noninverting output with reduced CML output level
30kΩ to GND	Inverting output with reduced CML output level
GND	Inverting output with full CML output level

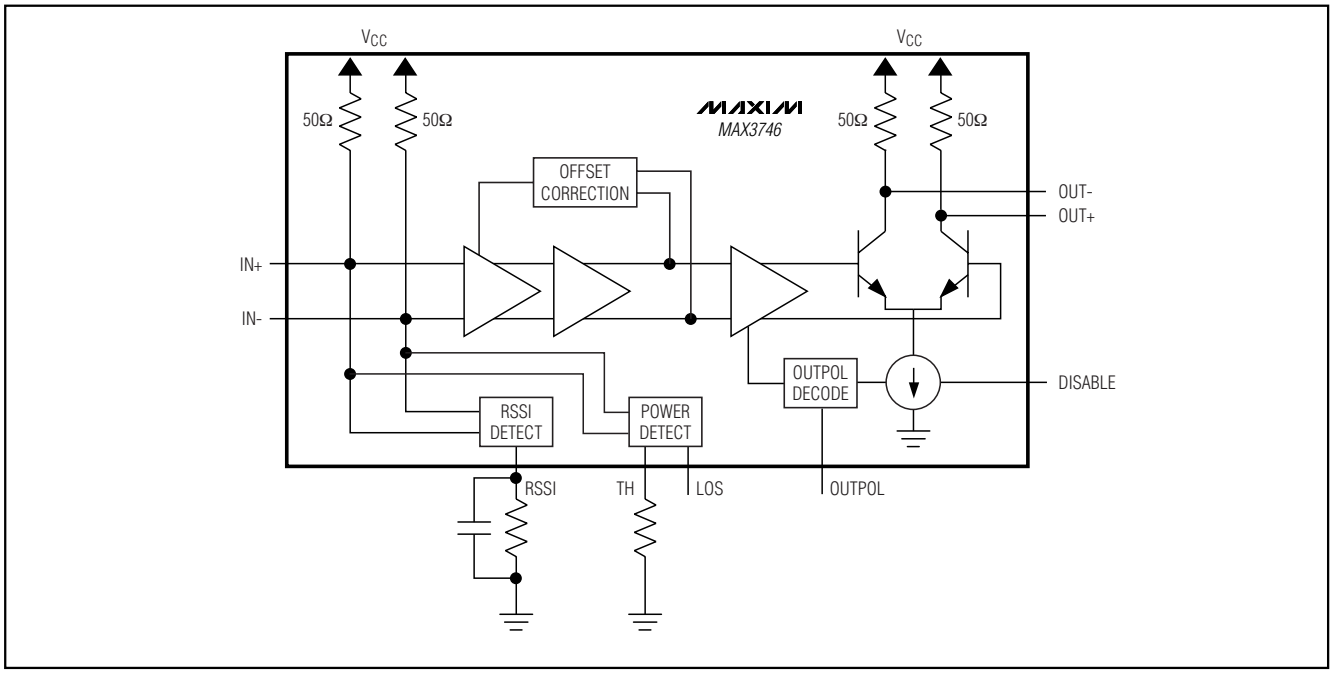
Chip Information

TRANSISTOR COUNT: 1385

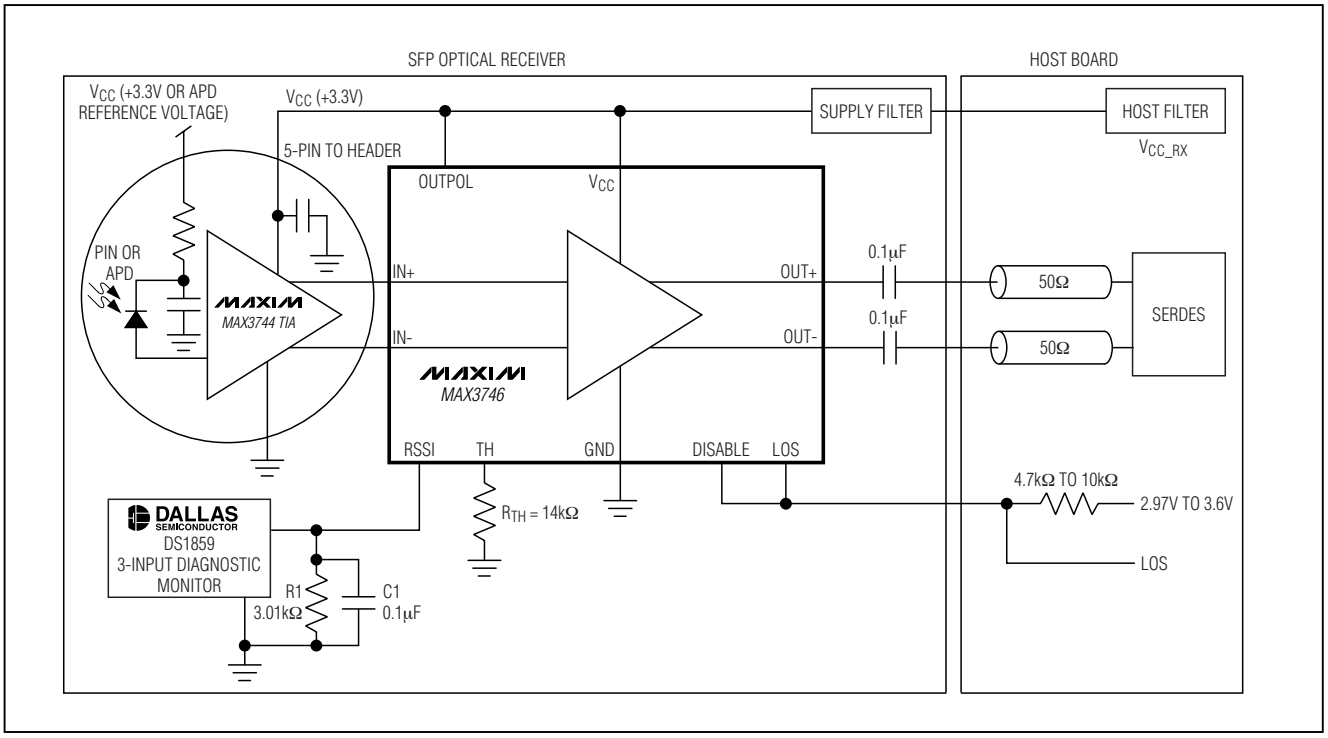
PROCESS: SiGe Bipolar

Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

Functional Diagram

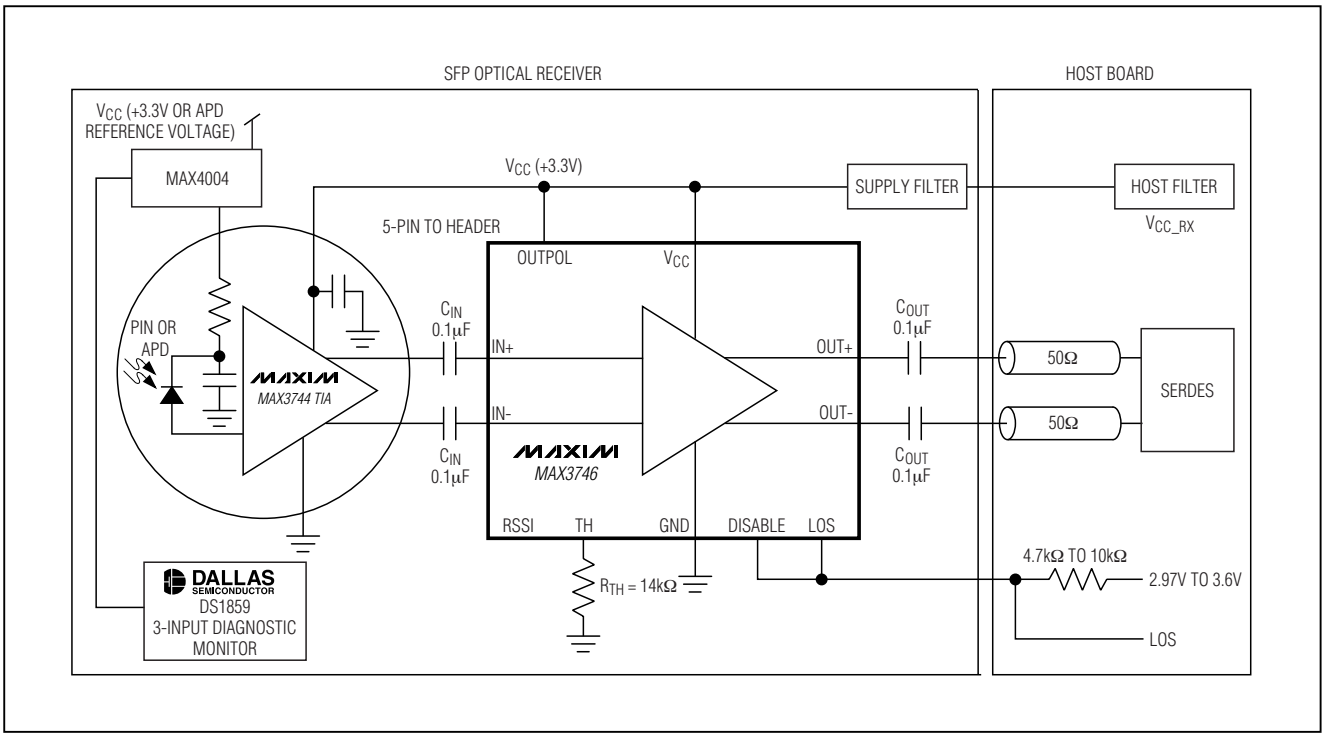


Typical Operating Circuits (continued)

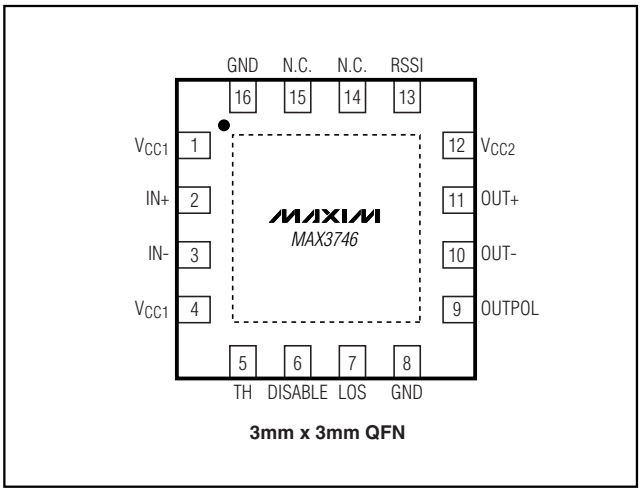


Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

Typical Operating Circuits (continued)



Pin Configuration



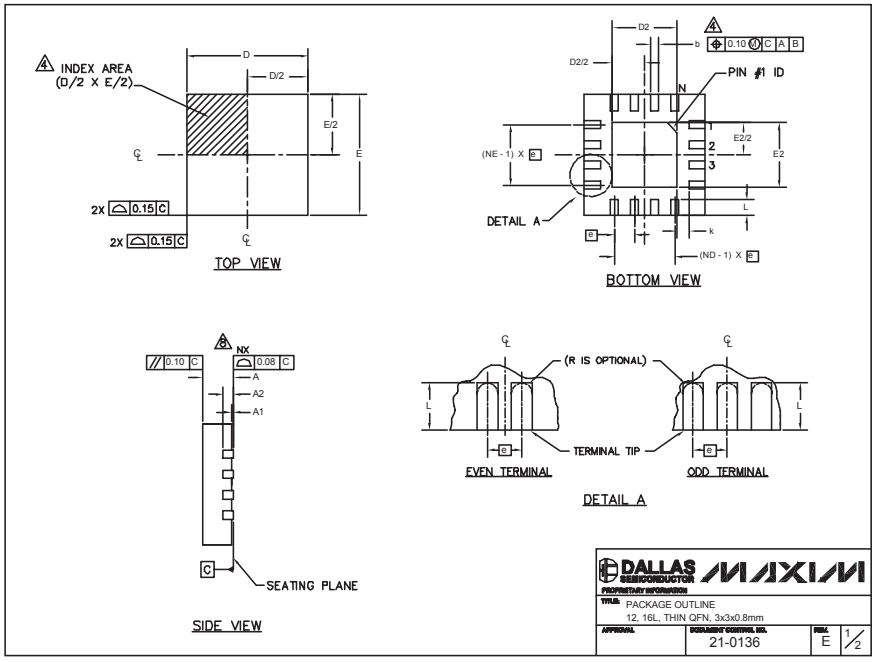
3mm x 3mm QFN

Low-Power, 622Mbps to 3.2Gbps Limiting Amplifier

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

12x16L QFN THIN.EPS



DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12, 16L, THIN QFN, 3x3x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. E | 1/2

PKG	12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80
b	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10
e	0.50 BSC.			0.50 BSC.		
L	0.45	0.55	0.65	0.30	0.40	0.50
N	12			16		
ND	3			4		
NE	3			4		
A1	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2			PIN ID	JEDEC	DOWN BONDS ALLOWED
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.			
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	NO
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1	YES
T1633-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	YES
T1633F-3	0.55	0.80	0.95	0.55	0.80	0.95	0.225 x 45°	WEED-2	N/A
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2	NO

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE 12, 16L, THIN QFN, 3x3x0.8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0136 | REV. E | 2/2

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